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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347ecvvagdb

1 Overview

This section provides a high-level overview of the MPC8347E features. Figure 1 shows the major functional units within the MPC8347E.

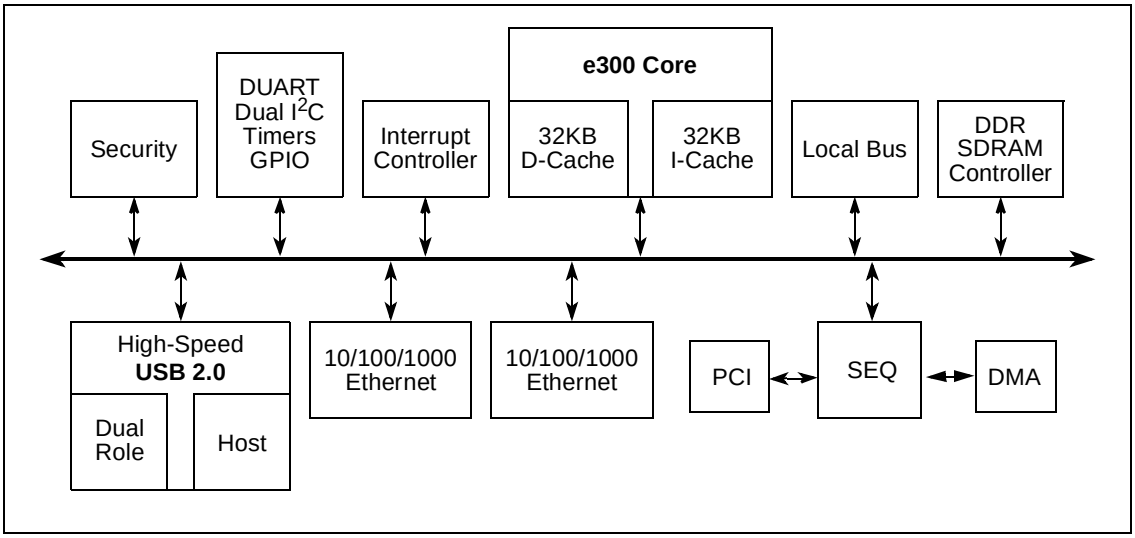


Figure 1. MPC8347E Block Diagram

Major features of the MPC8347E are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR SDRAM memory controller
  - Programmable timing for DDR-1 SDRAM
  - 32- or 64-bit data interface, up to 333-MHz data rate for TBGA, 266 MHz for PBGA
  - Four banks of memory, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbit to 1 Gbit with x8/x16 data ports
  - Full error checking and correction (ECC) support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep mode for self-refresh SDRAM
  - Auto refresh

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8347E. The MPC8347E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.32	V	
PLL supply voltage		AV_{DD}	–0.3 to 1.32	V	
DDR DRAM I/O voltage		GV_{DD}	–0.3 to 3.63	V	
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63	V	
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8347E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

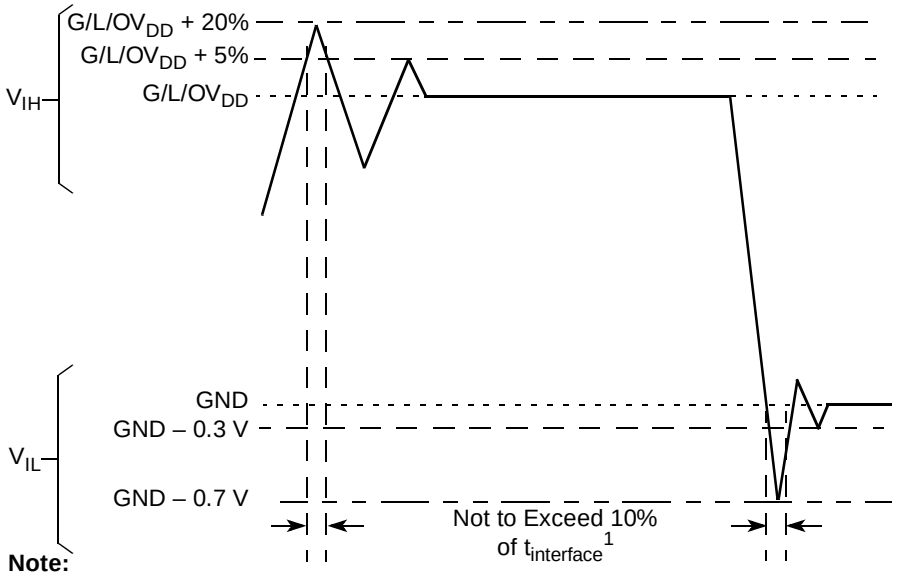
Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR DRAM I/O supply voltage	GV_{DD}	2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	LV_{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	LV_{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	3.3 V ± 330 mV	V	

Note:

1 GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8347E.



Note:

1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

Table 5 shows the estimated typical I/O power dissipation for MPC8347E.

Table 5. MPC8347E Typical I/O Power Dissipation

Interface	Parameter	DDR2 GV_{DD} (1.8 V)	DDR1 GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V Rs = 20 Ω Rt = 50 Ω 2 pair of clocks	200 MHz, 32 bits	—	0.42	—	—	—	W	—
	200 MHz, 64 bits	—	0.55	—	—	—	W	—
	266 MHz, 32 bits	—	0.5	—	—	—	W	—
	266 MHz, 64 bits	—	0.66	—	—	—	W	—
	300 MHz,[1] 32 bits	—	0.54	—	—	—	W	—
	300 MHz,[1] 64 bits	—	0.7	—	—	—	W	—
	333 MHz,[1] 32 bits	—	0.58	—	—	—	W	—
	333 MHz,[1] 64 bits	—	0.76	—	—	—	W	—
	400 MHz,[1] 32 bits	—	—	—	—	—		—
	400 MHz,[1] 64 bits	—	—	—	—	—		—
PCI I/O load = 30 pF	33 MHz, 32 bits	—	—	0.04	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
Local bus I/O load = 25 pF	167 MHz, 32 bits	—	—	0.34	—	—	W	—
	133 MHz, 32 bits	—	—	0.27	—	—	W	—
	83 MHz, 32 bits	—	—	0.17	—	—	W	—
	66 MHz, 32 bits	—	—	0.14	—	—	W	—
	50 MHz, 32 bits	—	—	0.11	—	—	W	—
TSEC I/O load = 25 pF	MII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.06	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
USB	12 MHz	—	—	0.01	—	—	W	Multiply by 2 if using 2 ports.
	480 MHz	—	—	0.2	—	—	W	
Other I/O		—	—	0.01	—	—	W	—

[1] TBGA package only.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKLME}	-0.9	0.3	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{\text{MCK}}$ can be shifted in 1/4 applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*, for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8347E.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8347E. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 5 shows the DDR SDRAM output timing for address skew with respect to any MCK.

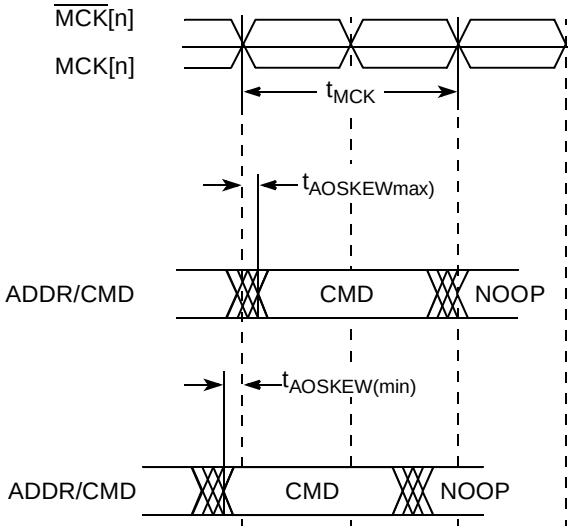


Figure 5. Timing Diagram for t_{AOSKEW} Measurement

Figure 6 provides the AC test load for the DDR bus.

Table 16. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8347E.

7.1 DUART DC Electrical Characteristics

Table 17 provides the DC electrical characteristics for the DUART interface of the MPC8347E.

Table 17. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (0.8 V ≤ V_{IN} ≤ 2 V)	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 18 provides the AC timing parameters for the DUART interface of the MPC8347E.

Table 18. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

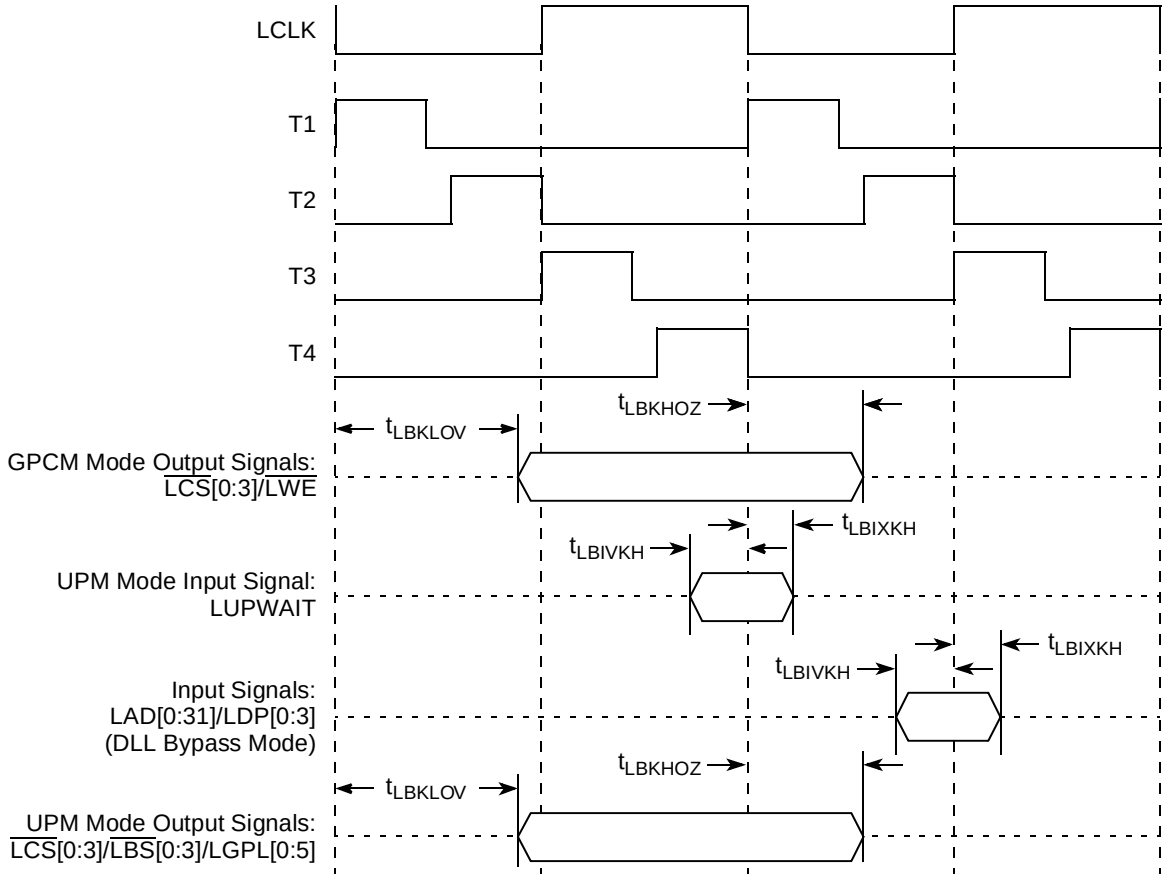


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

Figure 34 shows the PCI input AC timing diagram.

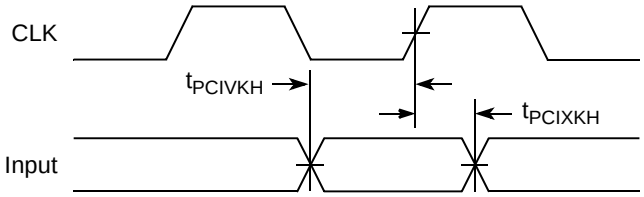


Figure 34. PCI Input AC Timing Diagram

Figure 35 shows the PCI output AC timing diagram.

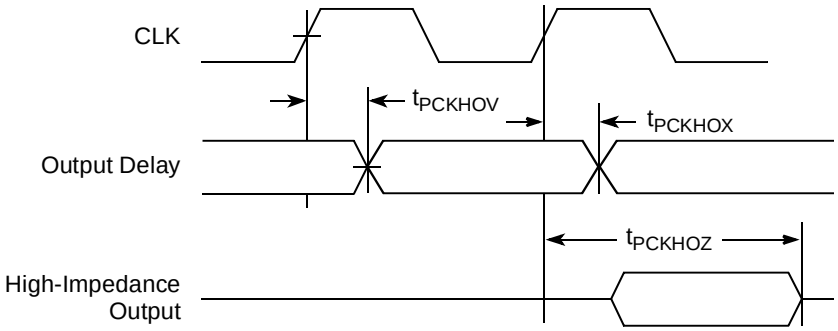


Figure 35. PCI Output AC Timing Diagram

18.5 Pinout Listings

Table 51 provides the pinout listing for the MPC8347E, 672 TBGA package.

Table 51. MPC8347E (TBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_INTA/IRQ_OUT	B34	O	OV_{DD}	2
PCI_RESET_OUT	C33	O	OV_{DD}	
PCI_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV_{DD}	
PCI_C/BE[3:0]	J30, M31, P33, T34	I/O	OV_{DD}	
PCI_PAR	P32	I/O	OV_{DD}	
PCI_FRAME	M32	I/O	OV_{DD}	5
PCI_TRDY	N29	I/O	OV_{DD}	5
PCI_IRDY	M34	I/O	OV_{DD}	5
PCI_STOP	N31	I/O	OV_{DD}	5
PCI_DEVSEL	N30	I/O	OV_{DD}	5
PCI_IDSEL	J31	I	OV_{DD}	
PCI_SERR	N34	I/O	OV_{DD}	5
PCI_PERR	N33	I/O	OV_{DD}	5
PCI_REQ[0]	D32	I/O	OV_{DD}	
PCI_REQ[1]/CPCI1_HS_ES	D34	I	OV_{DD}	
PCI_REQ[2:4]	E34, F32, G29	I	OV_{DD}	
PCI_GNT0	C34	I/O	OV_{DD}	
PCI_GNT1/CPCI1_HS_LED	D33	O	OV_{DD}	
PCI_GNT2/CPCI1_HS_ENUM	E33	O	OV_{DD}	
PCI_GNT[3:4]	F31, F33	O	OV_{DD}	
M66EN	A19	I	OV_{DD}	
DDR SDRAM Memory Interface				
MDQ[0:63]	D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8	I/O	GV_{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV_{DD}	
MECC[5]/MDVAL	U1	I/O	GV_{DD}	
MECC[6:7]	Y1, Y6	I/O	GV_{DD}	
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	O	GV_{DD}	
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV_{DD}	
MBA[0:1]	AD1, AA5	O	GV_{DD}	
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	O	GV_{DD}	
$\overline{\text{MWE}}$	AF1	O	GV_{DD}	
$\overline{\text{MRAS}}$	AF4	O	GV_{DD}	
$\overline{\text{MCAS}}$	AG3	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	AG2, AG1, AK1, AL4	O	GV_{DD}	
MCKE[0:1]	H3, G1	O	GV_{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	U3, E3, AN2, V4, E1, AM4	O	GV_{DD}	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
MODT[0:3]	AH3, AJ5, AH1, AJ4	—	—	
MBA[2]	H4	—	—	
SPARE1	AA1	—	—	8
SPARE2	AB1	—	—	6
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV_{DD}	
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	AM21	I/O	OV_{DD}	
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	AP22	I/O	OV_{DD}	
LDP[2]	AN22	I/O	OV_{DD}	
LDP[3]	AM22	I/O	OV_{DD}	
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV_{DD}	
$\overline{\text{LCS}}$[0:3]	AN24, AL23, AP25, AN25	O	OV_{DD}	
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	AK23, AP26, AL24, AM25	O	OV_{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LBCTL	AN26	O	OV_{DD}	
LALE	AK24	O	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV_{DD}	
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	AL25	I/O	OV_{DD}	
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	AJ24	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	AN27	I/O	OV_{DD}	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	AP28	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AL26	I/O	OV_{DD}	
LCKE	AM27	O	OV_{DD}	
LCLK[0:2]	AN28, AK26, AP29	O	OV_{DD}	
LSYNC_OUT	AM12	O	OV_{DD}	
LSYNC_IN	AJ10	I	OV_{DD}	
General Purpose I/O Timers				
GPIO1[0]/GTM1_TIN1/GTM2_TIN2	F24	I/O	OV_{DD}	
GPIO1[1]/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	E24	I/O	OV_{DD}	
GPIO1[2]/$\overline{\text{GTM1\_TOUT1}}$	B25	I/O	OV_{DD}	
GPIO1[3]/GTM1_TIN2/GTM2_TIN1	D24	I/O	OV_{DD}	
GPIO1[4]/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	A25	I/O	OV_{DD}	
GPIO1[5]/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	B24	I/O	OV_{DD}	
GPIO1[6]/GTM1_TIN3/GTM2_TIN4	A24	I/O	OV_{DD}	
GPIO1[7]/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	D23	I/O	OV_{DD}	
GPIO1[8]/$\overline{\text{GTM1\_TOUT3}}$	B23	I/O	OV_{DD}	
GPIO1[9]/GTM1_TIN4/GTM2_TIN3	A23	I/O	OV_{DD}	
GPIO1[10]/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	F22	I/O	OV_{DD}	
GPIO1[11]/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	E22	I/O	OV_{DD}	
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	A26	I/O	OV_{DD}	
MPH1_D1_SER_TXD/DR_D1_SER_TXD	B26	I/O	OV_{DD}	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	D25	I/O	OV_{DD}	
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV_{DD}	
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV_{DD}	
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV_{DD}	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	D26	I/O	OV_{DD}	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	E26	I/O	OV_{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	O	OV_{DD}	
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV_{DD}	
$\overline{\text{UART\_CTS}}$[1]/MSRCID4/LSRCID4	AP30	I/O	OV_{DD}	
$\overline{\text{UART\_CTS}}$[2]/MDVAL/ LDVAL	AN30	I/O	OV_{DD}	
$\overline{\text{UART\_RTS}}$[1:2]	AP31, AM30	O	OV_{DD}	
I^2C interface				
IIC1_SDA	AK29	I/O	OV_{DD}	2
IIC1_SCL	AP32	I/O	OV_{DD}	2
IIC2_SDA	AN31	I/O	OV_{DD}	2
IIC2_SCL	AM31	I/O	OV_{DD}	2
SPI				
SPIMOSI	AN32	I/O	OV_{DD}	
SPIMISO	AP33	I/O	OV_{DD}	
SPICLK	AK30	I/O	OV_{DD}	
SPISEL	AL31	I	OV_{DD}	
Clocks				
PCI_CLK_OUT[0:4]	AN9, AP9, AM10, AN10, AJ11	O	OV_{DD}	
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV_{DD}	
PCI_SYNC_OUT	AP11	O	OV_{DD}	3
RTC/PIT_CLOCK	AM32	I	OV_{DD}	
CLKIN	AM9	I	OV_{DD}	
JTAG				
TCK	E20	I	OV_{DD}	
TDI	F20	I	OV_{DD}	4
TDO	B20	O	OV_{DD}	3
TMS	A20	I	OV_{DD}	4
$\overline{\text{TRST}}$	B19	I	OV_{DD}	4
Test				
TEST	D22	I	OV_{DD}	6
TEST_SEL	AL13	I	OV_{DD}	7
PMC				
$\overline{\text{QUIESCE}}$	A18	O	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCAS}}$	AG6	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	AE7, AH7, AH4, AF2	O	GV_{DD}	
MCKE[0:1]	AG23, AH23	O	GV_{DD}	3
MCK[0:5]	AH15, AE24, AE2, AF14, AE23, AD3	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	AG15, AD23, AE3, AG14, AF24, AD2	O	GV_{DD}	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
MODT[0:3]	AG5, AD4, AH6, AF4	—	—	
MBA[2]	AD22			
SPARE1	AF12	—	—	7
SPARE2	AG11	—	—	6
Local Bus Controller Interface				
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV_{DD}	
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	H1	I/O	OV_{DD}	
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	K5	I/O	OV_{DD}	
LDP[2]	H2	I/O	OV_{DD}	
LDP[3]	G1	I/O	OV_{DD}	
LA[27:31]	J4, H3, G2, F1, G3	O	OV_{DD}	
$\overline{\text{LCS}}$[0:3]	J5, H4, F2, E1	O	OV_{DD}	
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	F3, G4, D1, E2	O	OV_{DD}	
LBCTL	H5	O	OV_{DD}	
LALE	E3	O	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	F4	I/O	OV_{DD}	
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	D2	I/O	OV_{DD}	
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	C1	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	C2	I/O	OV_{DD}	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	B3	I/O	OV_{DD}	
LCKE	E4	O	OV_{DD}	
LCLK[0:2]	D4, A3, C4	O	OV_{DD}	
LSYNC_OUT	U3	O	OV_{DD}	
LSYNC_IN	Y2	I	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
General Purpose I/O Timers				
GPIO1[0]/GTM1_TIN1/GTM2_TIN2	D27	I/O	OV_{DD}	
GPIO1[1]/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	E26	I/O	OV_{DD}	
GPIO1[2]/$\overline{\text{GTM1\_TOUT1}}$	D28	I/O	OV_{DD}	
GPIO1[3]/GTM1_TIN2/GTM2_TIN1	G25	I/O	OV_{DD}	
GPIO1[4]/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	J24	I/O	OV_{DD}	
GPIO1[5]/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	F26	I/O	OV_{DD}	
GPIO1[6]/GTM1_TIN3/GTM2_TIN4	E27	I/O	OV_{DD}	
GPIO1[7]/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	E28	I/O	OV_{DD}	
GPIO1[8]/$\overline{\text{GTM1\_TOUT3}}$	H25	I/O	OV_{DD}	
GPIO1[9]/GTM1_TIN4/GTM2_TIN3	F27	I/O	OV_{DD}	
GPIO1[10]/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	K24	I/O	OV_{DD}	
GPIO1[11]/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	G26	I/O	OV_{DD}	
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	C28	I/O	OV_{DD}	
MPH1_D1_SER_TXD/DR_D1_SER_TXD	F25	I/O	OV_{DD}	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	B28	I/O	OV_{DD}	
MPH1_D3_SPEED/DR_D3_SPEED	C27	I/O	OV_{DD}	
MPH1_D4_DP/DR_D4_DP	D26	I/O	OV_{DD}	
MPH1_D5_DM/DR_D5_DM	E25	I/O	OV_{DD}	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	C26	I/O	OV_{DD}	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	D25	I/O	OV_{DD}	
MPH1_NXT/DR_SESS_VLD_NXT	B26	I	OV_{DD}	
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	E24	I/O	OV_{DD}	
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	A27	O	OV_{DD}	
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	C25	I	OV_{DD}	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A26	O	OV_{DD}	
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	B25	O	OV_{DD}	
MPH1_CLK/DR_CLK	A25	I	OV_{DD}	
USB Port 0				
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	D24	I/O	OV_{DD}	
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	C24	I/O	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV_{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV_{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV_{DD}	
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV_{DD}	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV_{DD}	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV_{DD}	
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV_{DD}	
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV_{DD}	
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV_{DD}	
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV_{DD}	
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV_{DD}	
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV_{DD}	
MPH0_CLK/DR_RX_VALID	C21	I	OV_{DD}	
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E8	O	OV_{DD}	2
$\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12]	J28	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV_{DD}	
Ethernet Management Interface				
EC_MDC	Y24	O	LV_{DD1}	
EC_MDIO	Y25	I/O	LV_{DD1}	2
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV_{DD1}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV_{DD}	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV_{DD1}	
TSEC1_GTX_CLK	V24	O	LV_{DD1}	3
TSEC1_RX_CLK	U26	I	LV_{DD1}	
TSEC1_RX_DV	U24	I	LV_{DD1}	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV_{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV_{DD}	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV_{DD1}	
TSEC1_TX_CLK	N25	I	OV_{DD}	

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 56 shows the multiplication factor encodings for the system PLL.

Table 56. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

As described in Section 19, “Clocking,” the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 57 and Table 58 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 60. Suggested PLL Configurations

Ref No.[1]	RCWL		400 MHz Device			533 MHz Device			667 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
33 MHz CLKIN/PCI_CLK Options											
922	**1001**	**0100010**	—	—	—	—	—	f300	33	300	300
723	**0111**	**0100011**	33	233	350	33	233	350	33	233	350
604	**0110**	**0000100**	33	200	400	33	200	400	33	200	400
624	**0110**	**0100100**	33	200	400	33	200	400	33	200	400
803	**1000**	**0000011**	33	266	400	33	266	400	33	266	400
823	**1000**	**0100011**	33	266	400	33	266	400	33	266	400
903	**1001**	**0000011**	—			33	300	450	33	300	450
923	**1001**	**0100011**	—			33	300	450	33	300	450
704	**0111**	**0000011**	—			33	233	466	33	233	466
724	**0111**	**0100011**	—			33	233	466	33	233	466
A03	**1010**	**0000011**	—			33	333	500	33	333	500
804	**1000**	**0000100**	—			33	266	533	33	266	533
705	**0111**	**0000101**	—			—			33	233	583
606	**0110**	**0000110**	—			—			33	200	600
904	**1001**	**0000100**	—			—			33	300	600
805	**1000**	**0000101**	—			—			33	266	667
A04	**1010**	**0000100**	—			—			33	333	667
66 MHz CLKIN/PCI_CLK Options											
304	**0011**	**0000100**	66	200	400	66	200	400	66	200	400
324	**0011**	**0100100**	66	200	400	66	200	400	66	200	400
403	**0100**	**0000011**	66	266	400	66	266	400	66	266	400
423	**0100**	**0100011**	66	266	400	66	266	400	66	266	400
305	**0011**	**0000101**	—			66	200	500	66	200	500
503	**0101**	**0000011**	—			66	333	500	66	333	500
404	**0100**	**0000100**	—			66	266	533	66	266	533
306	**0011**	**0000110**	—			—			66	200	600
405	**0100**	**0000101**	—			—			66	266	667
504	**0101**	**0000100**	—			—			66	333	667

1 The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

2 The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

Table 68. SVR Settings (continued)

MPC8347E	PBGA	8054_0010
MPC8347	PBGA	8055_0010

23.2 Part Marking

Parts are marked as in the example shown in Figure 44.

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA or PBGA Devices

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