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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347eczqagd

Email: info@E-XFL.COM

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1 Overview

This section provides a high-level overview of the MPC8347E features. Figure 1 shows the major functional units within the MPC8347E.



Figure 1. MPC8347E Block Diagram

Major features of the MPC8347E are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR SDRAM memory controller
 - Programmable timing for DDR-1 SDRAM
 - 32- or 64-bit data interface, up to 333-MHz data rate for TBGA, 266 MHz for PBGA
 - Four banks of memory, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbit to 1 Gbit with x8/x16 data ports
 - Full error checking and correction (ECC) support
 - Page mode support (up to 16 simultaneous open pages)
 - Contiguous or discontiguous memory mapping
 - Read-modify-write support
 - Sleep mode for self-refresh SDRAM
 - Auto refresh

- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3[®], 802.3^w, 802.3^w, 802.3^w, 802.3^w, 802.3^w
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- PCI interface
 - Designed to comply with PCI Specification Revision 2.2
 - Data bus width:
 - 32-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities
 - PCI agent mode on PCI interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration supporting five masters on PCI
 - Accesses to all PCI address spaces
 - Parity supported
 - Selectable hardware-enforced coherency
 - Address translation units for address mapping between host and peripheral
 - Dual address cycle for target
 - Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i[®], iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms

- Programmable field size up to 2048 bits
- Elliptic curve cryptography
- F2m and F(p) modes
- Programmable field size up to 511 bits
- Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
- ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality
 - Complies with USB specification Rev. 2.0
 - Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints
 - Can operate as a stand-alone USB host controller
 - USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
 - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
 - Can operate as a stand-alone USB host controller
 - USB root hub with one or two downstream-facing ports

3 Power Characteristics

The estimated typical power dissipation for the MPC8347E device is shown in Table 4.

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T _J = 65	Typical ^{2,3}	Maximum ⁴	Unit
PBGA	266	266	1.3	1.6	1.8	W
		133	1.1	1.4	1.6	W
	400	266	1.5	1.9	2.1	W
		133	1.4	1.7	1.9	W
	400	200	1.5	1.8	2.0	W
		100	1.3	1.7	1.9	W
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W

Table 4. MPC8347E Power Dissipation¹

¹ The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.

² Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.

³ Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.

⁴ Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

Parameter/Condition	Min	Мах	Unit	Notes
Input hold time for POR configuration signals with respect to negation of HRESET	0	_	ns	
Time for the MPC8347E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8347E to turn on POR configuration signals with respect to the negation of HRESET	1	_	^t PCI_SYNC_IN	1, 3

Table 9. RESET Initialization Timing Specifications (continued)

Notes:

1. t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*.

- 2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual.
- 3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 lists the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8347E.

NOTE

The information in this document is accurate for revision 1.1 silicon and earlier. For information on revision 3.0 silicon and earlier versions see the *MPC8347EA PowerQUICCTM II Pro Integrated Host Processor Hardware Specifications*. See Section 23.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8347E.

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	
Output leakage current	I _{OZ}	-10	10	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{OH}	-15.2	—	mA	
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	—	mA	
MV _{REF} input leakage current	I _{VREF}	—	5	μA	

Table 11. DDR SDRAM DC Electrical Characteristics

Notes:

1. ${\rm GV}_{\rm DD}$ is expected to be within 50 mV of the DRAM ${\rm GV}_{\rm DD}$ at all times.

 MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 12 provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}		0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t _{AOSKEW}	1000 1100 1200	200 300 400	ps	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHAS}	2.8 3.45 4.6	_	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHAX	2.0 2.65 3.8	_	ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHCS	2.8 3.45 4.6	_	ns	4
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHCX	2.0 2.65 3.8	_	ns	4
MCK to MDQS 333 MHz 266 MHz 200 MHz	^t DDKHMH	-0.9 -1.1 -1.2	0.3 0.5 0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	^t DDKHDS, ^t DDKLDS	900 900 1200	_	ps	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	^t ddkhdx, ^t ddkldx	900 900 1200	_	ps	6
MDQS preamble start	t _{DDKHMP}	$-0.25 \times t_{MCK} - 0.9$	$-0.25 \times t_{\text{MCK}} + 0.3$	ns	7

Ethernet: Three-Speed Ethernet, MII Management

Figure 8 shows the GMII transmit AC timing diagram.



Figure 8. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 22 provides the GMII receive AC timing specifications.

Table 22. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock period	t _{GRX}	_	8.0	—	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise, V _{IL} (min) to V _{IH} (max)	t _{GRXR}		—	1.0	ns
RX_CLK clock fall time, $V_{IH}(max)$ to $V_{IL}(min)$	t _{GRXF}			1.0	ns

Note:

1. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Ethernet: Three-Speed Ethernet, MII Management

Figure 10 shows the MII transmit AC timing diagram.



Figure 10. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock period 10 Mbps	t _{MRX}	_	400	—	ns
RX_CLK clock period 100 Mbps	t _{MRX}	_	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V _{IL} (min) to V _{IH} (max)	t _{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V _{IH} (max) to V _{IL} (min)	t _{MRXF}	1.0	_	4.0	ns

Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular functionI. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 11 provides the AC test load for TSEC.



Figure 14 shows the TBI receive AC timing diagram.



Figure 14. TBI Receive AC Timing Diagram

8.2.4 RGMII and RTBI AC Timing Specifications

Table 27 presents the RGMII and RTBI AC timing specifications.

Table 27. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
Data to clock output skew (at transmitter)	t _{SKRGT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ²	t _{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t _{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t _{RGTH} /t _{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t _{RGTH} /t _{RGT}	40	50	60	%
Rise time (20%–80%)	t _{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t _{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t _{G12} 6	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	47	—	53	%

Notes:

 In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).

2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.

- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.
- 5. Duty cycle reference is $LV_{DD}/2$.

6. This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention.

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8347E.

9.1 USB DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the USB interface.

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current	I _{IN}	—	±5	μΑ
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} – 0.2	-	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

Table 31. USB DC Electrical Characteristics

9.2 USB AC Electrical Specifications

Table 32 describes the general timing parameters of the USB interface of the MPC8347E.

Table 32.	USB C	General	Timing	Parameters	(ULPI	Mode	Only)
					\-		

Parameter	Symbol ¹	Min	Мах	Unit	Notes
USB clock cycle time	t _{USCK}	15	-	ns	2–5
Input setup to USB clock—all inputs	t _{USIVKH}	4	-	ns	2–5
Input hold to USB clock—all inputs	t _{USIXKH}	1	-	ns	2–5
USB clock to output valid—all outputs	t _{USKHOV}	—	7	ns	2–5
Output hold from USB clock—all outputs	t _{USKHOX}	2		ns	2–5

Notes:

 The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

2. All timings are in reference to USB clock.

- 3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Local Bus

Figure 20 through Figure 25 show the local bus signals.



Figure 20. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)



Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)



Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8347E is available in two packages—a tape ball grid array (TBGA) and a plastic ball grid array (PBGA). See Section 18.1, "Package Parameters for the MPC8347E TBGA," Section 18.2, "Mechanical Dimensions for the MPC8347E TBGA, Section 18.3, "Package Parameters for the MPC8347E PBGA," and Section 18.4, "Mechanical Dimensions for the MPC8347E PBGA."

18.1 Package Parameters for the MPC8347E TBGA

The package parameters are provided in the following list. The package type is $35 \text{ mm} \times 35 \text{ mm}$, 672 tape ball grid array (TBGA).

Package outline	$35 \text{ mm} \times 35 \text{ mm}$
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm

Package and Pin Listings

18.4 Mechanical Dimensions for the MPC8347E PBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 620-PBGA package.



Notes:

1.All dimensions are in millimeters.

2.Dimensioning and tolerancing per ASME Y14. 5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E PBGA

Clocking

19 Clocking

Figure 41 shows the internal distribution of the clocks.



Figure 41. MPC8347E Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8347E is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICD*n*] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUT n signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8347E to function. When the MPC8347E is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

Table 60.	Suggested	PLL	Configurations
-----------	-----------	-----	----------------

Ref No. ¹	RC	WL	400	400 MHz Device 533 MHz Device		667 MHz Device					
	SPMF	CORE PLL	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)
				33 M	Hz CLKIN	PCI_CLK	Options				
922	1001	0100010	_	—		—	—	f300	33	300	300
723	0111	0100011	33	233	350	33	233	350	33	233	350
604	0110	0000100	33	200	400	33	200	400	33	200	400
624	0110	0100100	33	200	400	33	200	400	33	200	400
803	1000	0000011	33	266	400	33	266	400	33	266	400
823	1000	0100011	33	266	400	33	266	400	33	266	400
903	1001	0000011		_		33	300	450	33	300	450
923	1001	0100011		_		33	300	450	33	300	450
704	0111	0000011		_		33	233	466	33	233	466
724	0111	0100011	—		33	233	466	33	233	466	
A03	1010	0000011	_		33	333	500	33	333	500	
804	1000	0000100	_		33	266	533	33	266	533	
705	0111	0000101	—			_		33	233	583	
606	0110	0000110	_			_		33	200	600	
904	1001	0000100	_			—		33	300	600	
805	1000	0000101				_			266	667	
A04	1010	0000100		—			_		33	333	667
	66 MHz CLKIN/PCI_CLK Options										
304	0011	0000100	66	200	400	66	200	400	66	200	400
324	0011	0100100	66	200	400	66	200	400	66	200	400
403	0100	0000011	66	266	400	66	266	400	66	266	400
423	0100	0100011	66	266	400	66	266	400	66	266	400
305	0011	0000101				66	200	500	66	200	500
503	0101	0000011	—		66	333	500	66	333	500	
404	0100	0000100				66	266	533	66	266	533
306	0011	0000110							66	200	600
405	0100	0000101		—			_		66	266	667
504	0101	0000100	_						66	333	667

¹ The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

² The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

Tyco Electronics Chip Coolers [™] P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102
Interface material vendors include the following:	
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally

Revision	Date	Substantive Change(s)
1	4/2005	Table 1: Addition of note 1Table 48: Addition of Therm0 (K32)Table 49: Addition of Therm0 (B15)
0	4/2005	Initial release.

Table 66. Document Revision History (continued)



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