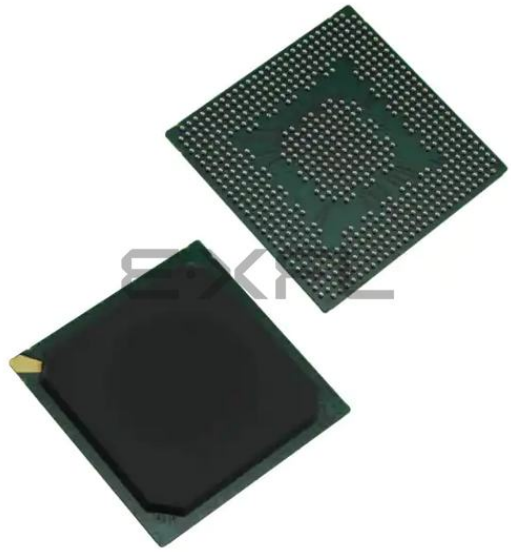

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | Security; SEC |
| RAM Controllers | DDR |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 620-BBGA Exposed Pad |
| Supplier Device Package | 620-HBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347eczqagdb |

  - Programmable field size up to 2048 bits
  - Elliptic curve cryptography
  - F2m and F(p) modes
  - Programmable field size up to 511 bits
- Data encryption standard (DES) execution unit (DEU)
  - DES and 3DES algorithms
  - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
  - ECB and CBC modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rijndael symmetric-key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, and counter (CTR) modes
- ARC four execution unit (AFEU)
  - Stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
  - Static and/or dynamic assignment of crypto-execution units through an integrated controller
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

- Universal serial bus (USB) dual role controller
  - USB on-the-go mode with both device and host functionality
  - Complies with USB specification Rev. 2.0
  - Can operate as a stand-alone USB device
    - One upstream facing port
    - Six programmable USB endpoints
  - Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
  - Can operate as a stand-alone USB host controller
    - USB root hub with one or two downstream-facing ports

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8347E. The MPC8347E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 1.32 | V | |
| PLL supply voltage | | $AV_{DD}$ | –0.3 to 1.32 | V | |
| DDR DRAM I/O voltage | | $GV_{DD}$ | –0.3 to 3.63 | V | |
| Three-speed Ethernet I/O, MII management voltage | | $LV_{DD}$ | –0.3 to 3.63 | V | |
| PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | | $OV_{DD}$ | –0.3 to 3.63 | V | |
| Input voltage | DDR DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | DDR DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | Three-speed Ethernet signals | $LV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3) | V | 4, 5 |
| | Local bus, DUART, CLKIN, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 3, 5 |
| | PCI | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 6 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | |

**Notes:**

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $LV_{IN}$ must not exceed $LV_{DD}$ by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. $OV_{IN}$ on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

## 2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8347E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

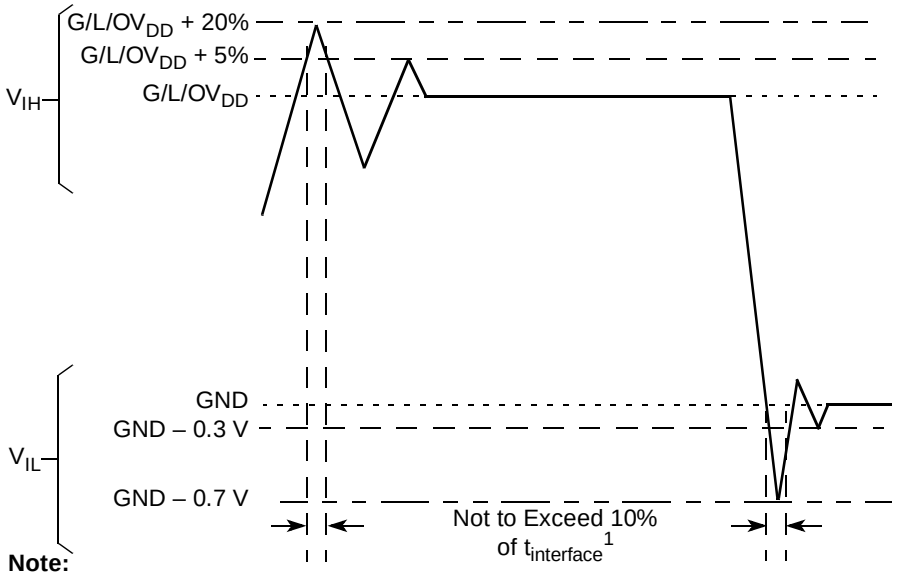
**Table 2. Recommended Operating Conditions**

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | 1.2 V ± 60 mV | V | 1 |
| PLL supply voltage | $AV_{DD}$ | 1.2 V ± 60 mV | V | 1 |
| DDR DRAM I/O supply voltage | $GV_{DD}$ | 2.5 V ± 125 mV | V | |
| Three-speed Ethernet I/O supply voltage | $LV_{DD1}$ | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | V | |
| Three-speed Ethernet I/O supply voltage | $LV_{DD2}$ | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | V | |
| PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | $OV_{DD}$ | 3.3 V ± 330 mV | V | |

**Note:**

1 $GV_{DD}$, $LV_{DD}$, $OV_{DD}$, $AV_{DD}$, and $V_{DD}$ must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8347E.




**Note:**

1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

**Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$**

Table 5 shows the estimated typical I/O power dissipation for MPC8347E.

**Table 5. MPC8347E Typical I/O Power Dissipation**

| Interface | Parameter | DDR2 $GV_{DD}$ (1.8 V) | DDR1 $GV_{DD}$ (2.5 V) | $OV_{DD}$ (3.3 V) | $LV_{DD}$ (3.3 V) | $LV_{DD}$ (2.5 V) | Unit | Comments |
|---|---|---|---|---|---|---|---|---|
| DDR I/O<br>65% utilization<br>2.5 V<br>Rs = 20 Ω<br>Rt = 50 Ω<br>2 pair of clocks | 200 MHz, 32 bits | — | 0.42 | — | — | — | W | — |
| | 200 MHz, 64 bits | — | 0.55 | — | — | — | W | — |
| | 266 MHz, 32 bits | — | 0.5 | — | — | — | W | — |
| | 266 MHz, 64 bits | — | 0.66 | — | — | — | W | — |
| | 300 MHz,[1] 32 bits | — | 0.54 | — | — | — | W | — |
| | 300 MHz,[1] 64 bits | — | 0.7 | — | — | — | W | — |
| | 333 MHz,[1] 32 bits | — | 0.58 | — | — | — | W | — |
| | 333 MHz,[1] 64 bits | — | 0.76 | — | — | — | W | — |
| | 400 MHz,[1] 32 bits | — | — | — | — | — | | — |
| | 400 MHz,[1] 64 bits | — | — | — | — | — | | — |
| PCI I/O<br>load = 30 pF | 33 MHz, 32 bits | — | — | 0.04 | — | — | W | — |
| | 66 MHz, 32 bits | — | — | 0.07 | — | — | W | — |
| Local bus I/O<br>load = 25 pF | 167 MHz, 32 bits | — | — | 0.34 | — | — | W | — |
| | 133 MHz, 32 bits | — | — | 0.27 | — | — | W | — |
| | 83 MHz, 32 bits | — | — | 0.17 | — | — | W | — |
| | 66 MHz, 32 bits | — | — | 0.14 | — | — | W | — |
| | 50 MHz, 32 bits | — | — | 0.11 | — | — | W | — |
| TSEC I/O<br>load = 25 pF | MII | — | — | — | 0.01 | — | W | Multiply by number of interfaces used. |
| | GMII or TBI | — | — | — | 0.06 | — | W | |
| | RGMII or RTBI | — | — | — | — | 0.04 | W | |
| USB | 12 MHz | — | — | 0.01 | — | — | W | Multiply by 2 if using 2 ports. |
| | 480 MHz | — | — | 0.2 | — | — | W | |
| Other I/O | | — | — | 0.01 | — | — | W | — |

[1] TBGA package only.

## 6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

### 6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

**Table 13. DDR SDRAM Input AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 2.5 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.31 | V | |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.31 | $GV_{DD}$ + 0.3 | V | |
| MDQS—MDQ/MECC input skew per byte<br>333 MHz<br>266 MHz | $t_{DISKEW}$ | — | <br>750<br>1125 | ps | 1 |

**Note:**

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 <= n <= 7) or ECC (MECC[{0...7}] if n = 8).

Figure 4 illustrates the DDR input timing diagram showing the $t_{DISKEW}$ timing parameter.

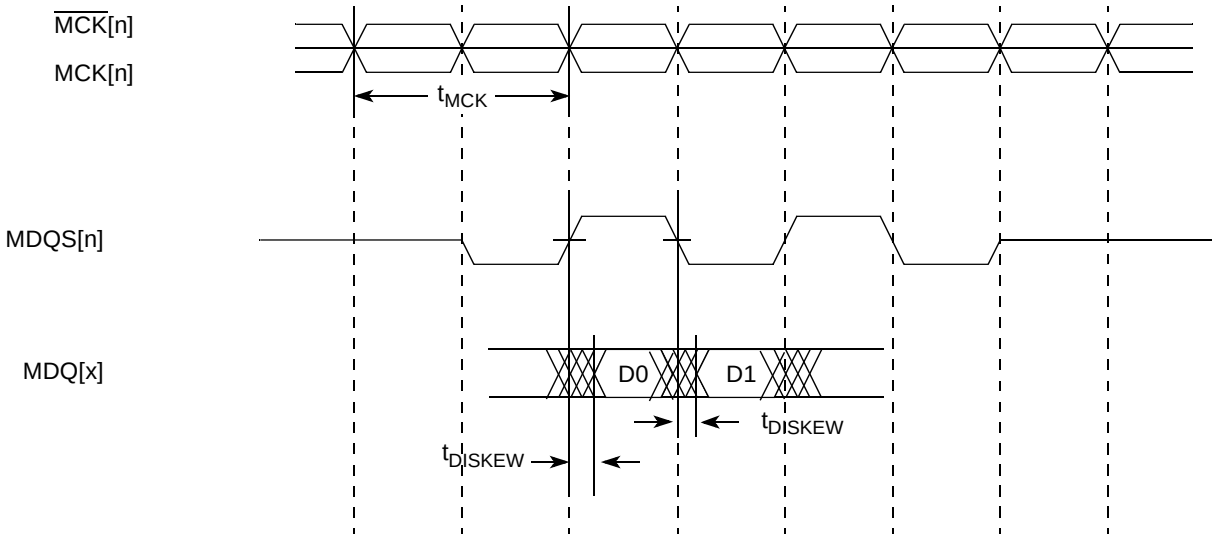



**Figure 4.** DDR Input Timing Diagram

### 6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

Figure 13 shows the TBI transmit AC timing diagram.

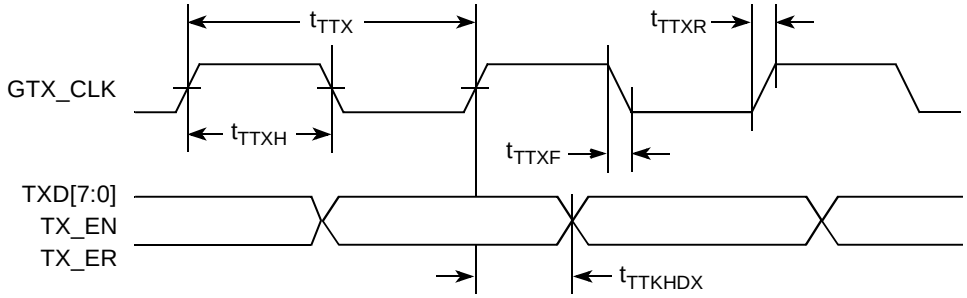



**Figure 13. TBI Transmit AC Timing Diagram**

### 8.2.3.2 TBI Receive AC Timing Specifications

Table 26 provides the TBI receive AC timing specifications.

**Table 26. TBI Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| PMA_RX_CLK clock period | $t_{TRX}$ | | 16.0 | | ns |
| PMA_RX_CLK skew | $t_{SKTRX}$ | 7.5 | — | 8.5 | ns |
| RX_CLK duty cycle | $t_{TRXH}/t_{TRX}$ | 40 | — | 60 | % |
| RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK | $t_{TRDVKH}$[2] | 2.5 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK | $t_{TRDXKH}$[2] | 1.5 | — | — | ns |
| RX_CLK clock rise time $V_{IL}$(min) to $V_{IH}$(max) | $t_{TRXR}$ | 0.7 | — | 2.4 | ns |
| RX_CLK clock fall time $V_{IH}$(max) to $V_{IL}$(min) | $t_{TRXF}$ | 0.7 | — | 2.4 | ns |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TRDVKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{TRDXKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of $t_{TRX}$ represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
2. Setup and hold time of even numbered RCG are measured from the riding edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the riding edge of PMA_RX_CLK0.

Figure 14 shows the TBI receive AC timing diagram.

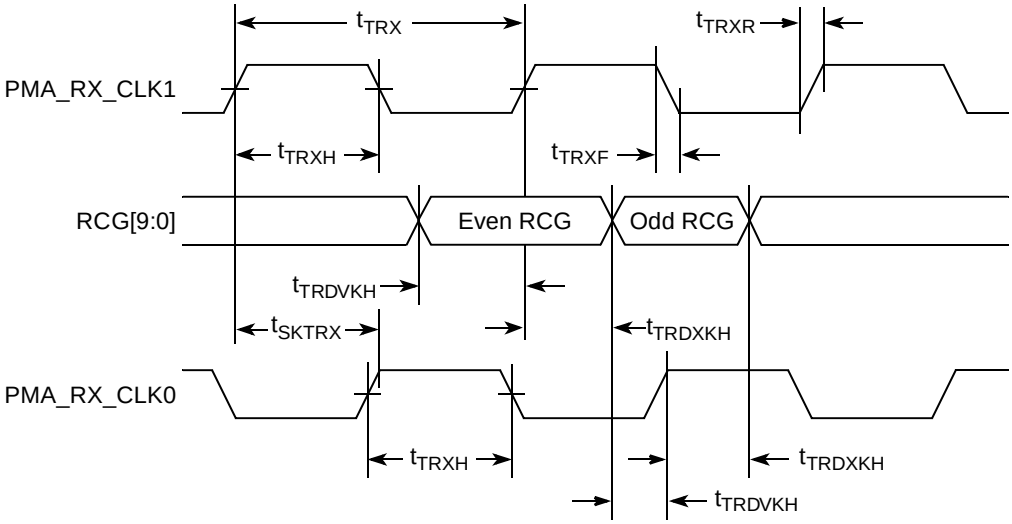



**Figure 14. TBI Receive AC Timing Diagram**

## 8.2.4 RGMII and RTBI AC Timing Specifications

Table 27 presents the RGMII and RTBI AC timing specifications.

**Table 27. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$ | –0.5 | — | 0.5 | ns |
| Data to clock input skew (at receiver)[2] | $t_{SKRGT}$ | 1.0 | — | 2.8 | ns |
| Clock cycle duration[3] | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 1000Base-T[4, 5] | $t_{RGTH}/t_{RGT}$ | 45 | 50 | 55 | % |
| Duty cycle for 10BASE-T and 100BASE-TX[3, 5] | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns |
| GTX_CLK125 reference clock period | $t_{G12}$[6] | — | 8.0 | — | ns |
| GTX_CLK125 reference clock duty cycle | $t_{G125H}/t_{G125}$ | 47 | — | 53 | % |

**Notes:**

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned.
5. Duty cycle reference is $LV_{DD}/2$.
6. This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention.

# 10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8347E.

## 10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

**Table 33. Local Bus DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

## 10.2 Local Bus AC Electrical Specification

Table 34 and Table 35 describe the general timing parameters of the local bus interface of the MPC8347E.

**Table 34. Local Bus General Timing Parameters—DLL On**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | — | ns | 2 |
| Input setup to local bus clock (except LUPWAIT) | $t_{LBIVKH1}$ | 1.5 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 2.2 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| LUPWAIT Input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |
| Local bus clock to LALE rise | $t_{LBKHLR}$ | — | 4.5 | ns | |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 4.5 | ns | |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 4.5 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 4.5 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 1 | — | ns | 3 |

**Table 34. Local Bus General Timing Parameters—DLL On (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 1 | — | ns | 3 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ}$ | — | 3.8 | ns | 8 |

**Notes:**
1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

**Table 35. Local Bus General Timing Parameters—DLL Bypass[9]**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 15 | — | ns | 2 |
| Input setup to local bus clock | $t_{LBIVKH}$ | 7 | — | ns | 3, 4 |
| Input hold from local bus clock | $t_{LBIXKH}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |

**Table 39. I²C AC Electrical Specifications (continued)**

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| Fall time of both SDA and SCL signals[5] | $t_{I2CF}$ | — | 300 | ns |
| Setup time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | µs |
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | µs |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times OV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times OV_{DD}$ | — | V |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8347E provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{I2DVKH}$ must be met only if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. $C_B$ = capacitance of one bus line in pF.
5. The MPC8347E does not follow the "I2C-BUS Specifications" version 2.1 regarding the $t_{I2CF}$ AC parameter.

Figure 31 provides the AC test load for the I²C.

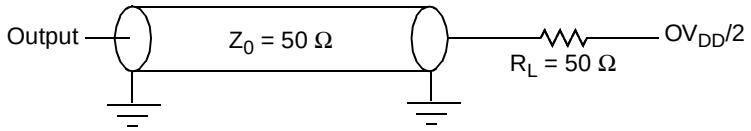



**Figure 31. I²C AC Test Load**

Figure 32 shows the AC timing diagram for the I²C bus.

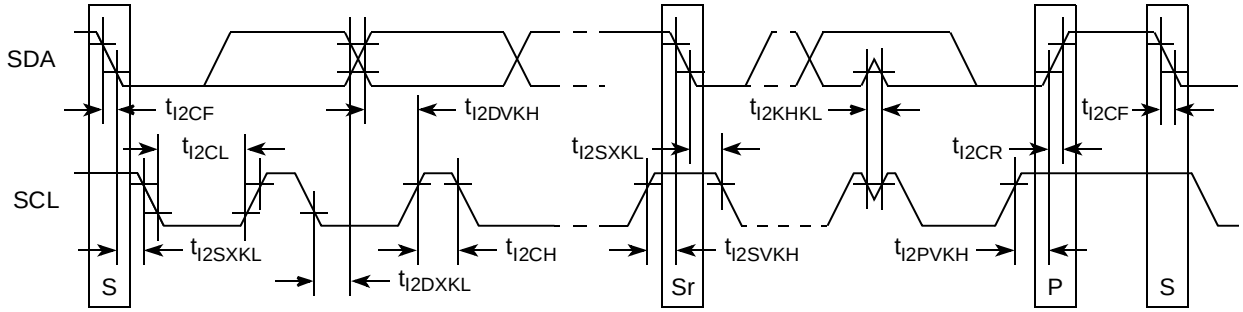



**Figure 32. I²C Bus AC Timing Diagram**

**Table 41. PCI AC Timing Specifications at 66 MHz[1] (continued)**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 3, 5 |

**Notes:**
1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
3. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

**Table 42. PCI AC Timing Specifications at 33 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 11 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 2 | — | ns | 2 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 2, 3 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 2, 4 |
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 2, 4 |

**Notes:**
1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 33 provides the AC test load for PCI.

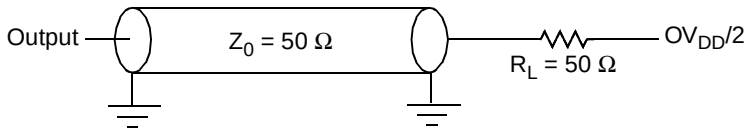



**Figure 33. PCI AC Test Load**

# 14 Timers

This section describes the DC and AC electrical specifications for the timers.

## 14.1 Timer DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the MPC8347E timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

**Table 43. Timer DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | | | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

## 14.2 Timer AC Timing Specifications

Table 44 provides the timer input and output AC timing specifications.

**Table 44. Timers Input AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Unit |
|---|---|---|---|
| Timers inputs—minimum pulse width | $t_{TIWID}$ | 20 | ns |

**Notes:**

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least $t_{TIWID}$ ns to ensure proper operation.

# 16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

## 16.1 IPIC DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the external interrupt pins.

**Table 47. IPIC DC Electrical Characteristics[1]**

| Characteristic | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | | 2.0 | $OV_{DD}$ + 0.3 | V | |
| Input low voltage | $V_{IL}$ | | –0.3 | 0.8 | V | |
| Input current | $I_{IN}$ | | | ±5 | μA | |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V | 2 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V | 2 |

**Notes:**
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, and $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open-drain pins; thus $V_{OH}$ is not relevant for those pins.

## 16.2 IPIC AC Timing Specifications

Table 48 provides the IPIC input and output AC timing specifications.

**Table 48. IPIC Input AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Unit |
|---|---|---|---|
| IPIC inputs—minimum pulse width | $t_{PICWID}$ | 20 | ns |

**Notes:**
1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least $t_{PICWID}$ ns to ensure proper operation in edge triggered mode.

Figure 36 provides the AC test load for the SPI.

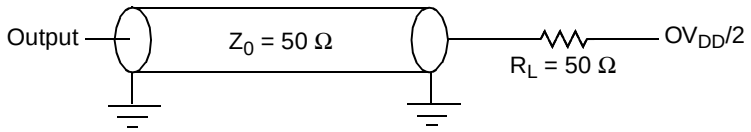
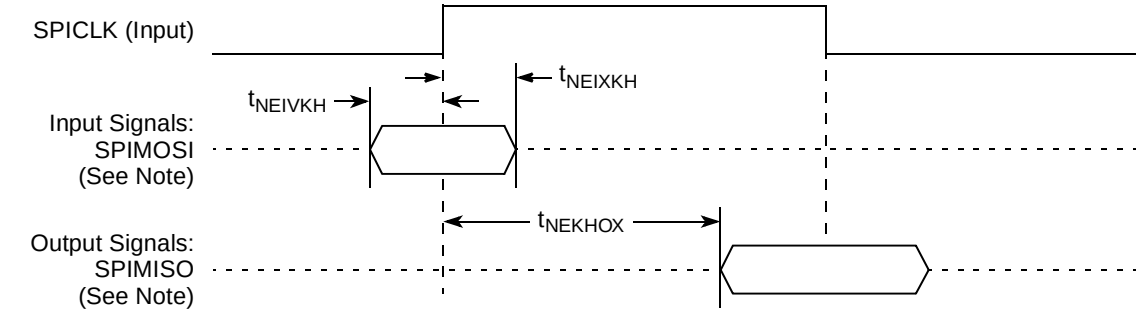



**Figure 36. SPI AC Test Load**

Figure 37 and Figure 38 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

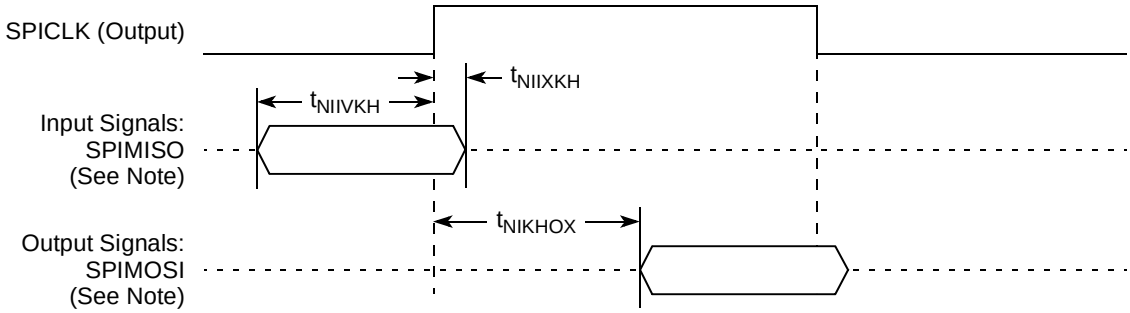
Figure 37 shows the SPI timings in slave mode (external clock).




**Note:** The clock edge is selectable on SPI.

**Figure 37. SPI AC Timing in Slave Mode (External Clock) Diagram**

Figure 38 shows the SPI timings in master mode (internal clock).




**Note:** The clock edge is selectable on SPI.

**Figure 38. SPI AC Timing in Master Mode (Internal Clock) Diagram**

**Table 52. MPC8347E (PBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| MPH0_D2_VMO_SE0/DR_D10_DPPD | B24 | I/O | $OV_{DD}$ | |
| MPH0_D3_SPEED/DR_D11_DMMD | A24 | I/O | $OV_{DD}$ | |
| MPH0_D4_DP/DR_D12_VBUS_VLD | D23 | I/O | $OV_{DD}$ | |
| MPH0_D5_DM/DR_D13_SESS_END | C23 | I/O | $OV_{DD}$ | |
| MPH0_D6_SER_RCV/DR_D14 | B23 | I/O | $OV_{DD}$ | |
| MPH0_D7_DRVVBUS/DR_D15_IDPULLUP | A23 | I/O | $OV_{DD}$ | |
| MPH0_NXT/DR_RX_ACTIVE_ID | D22 | I | $OV_{DD}$ | |
| MPH0_DIR_DPPULLUP/DR_RESET | C22 | I/O | $OV_{DD}$ | |
| MPH0_STP_SUSPEND/DR_TX_READY | B22 | I/O | $OV_{DD}$ | |
| MPH0_PWRFAULT/DR_RX_VALIDH | A22 | I | $OV_{DD}$ | |
| MPH0_PCTL0/DR_LINE_STATE0 | E21 | I/O | $OV_{DD}$ | |
| MPH0_PCTL1/DR_LINE_STATE1 | D21 | I/O | $OV_{DD}$ | |
| MPH0_CLK/DR_RX_VALID | C21 | I | $OV_{DD}$ | |
| **Programmable Interrupt Controller** | | | | |
| $\overline{\text{MCP\_OUT}}$ | E8 | O | $OV_{DD}$ | 2 |
| $\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12] | J28 | I/O | $OV_{DD}$ | |
| $\overline{\text{IRQ}}$[1:5]/GPIO2[13:17] | K25, J25, H26, L24, G27 | I/O | $OV_{DD}$ | |
| $\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT | G28 | I/O | $OV_{DD}$ | |
| $\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN | J26 | I/O | $OV_{DD}$ | |
| **Ethernet Management Interface** | | | | |
| EC_MDC | Y24 | O | $LV_{DD1}$ | |
| EC_MDIO | Y25 | I/O | $LV_{DD1}$ | 2 |
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | Y26 | I | $LV_{DD1}$ | |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_COL/GPIO2[20] | M26 | I/O | $OV_{DD}$ | |
| TSEC1_CRS/GPIO2[21] | U25 | I/O | $LV_{DD1}$ | |
| TSEC1_GTX_CLK | V24 | O | $LV_{DD1}$ | 3 |
| TSEC1_RX_CLK | U26 | I | $LV_{DD1}$ | |
| TSEC1_RX_DV | U24 | I | $LV_{DD1}$ | |
| TSEC1_RX_ER/GPIO2[26] | L28 | I/O | $OV_{DD}$ | |
| TSEC1_RXD[7:4]/GPIO2[22:25] | M27, M28, N26, N27 | I/O | $OV_{DD}$ | |
| TSEC1_RXD[3:0] | W26, W24, Y28, Y27 | I | $LV_{DD1}$ | |
| TSEC1_TX_CLK | N25 | I | $OV_{DD}$ | |

# 20 Thermal

This section describes the thermal specifications of the MPC8347E.

## 20.1 Thermal Characteristics

Table 61 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8347E.

**Table 61. Package Thermal Characteristics for TBGA**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient natural convection on single-layer board (1s) | $R_{\theta JA}$ | 14 | °C/W | 1, 2 |
| Junction-to-ambient natural convection on four-layer board (2s2p) | $R_{\theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction-to-ambient (@ 200 ft/min) on single-layer board (1s) | $R_{\theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p) | $R_{\theta JMA}$ | 8 | °C/W | 1, 3 |
| Junction-to-ambient (@ 2 m/s) on single-layer board (1s) | $R_{\theta JMA}$ | 9 | °C/W | 1, 3 |
| Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p) | $R_{\theta JMA}$ | 7 | °C/W | 1, 3 |
| Junction-to-board thermal | $R_{\theta JB}$ | 3.8 | °C/W | 4 |
| Junction-to-case thermal | $R_{\theta JC}$ | 1.7 | °C/W | 5 |
| Junction-to-package natural convection on top | $\Psi_{JT}$ | 1 | °C/W | 6 |

**Notes:**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 62 provides the package thermal characteristics for the 620 29 × 29 mm PBGA of the MPC8347E.

**Table 62. Package Thermal Characteristics for PBGA**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient natural convection on single-layer board (1s) | $R_{\theta JA}$ | 21 | °C/W | 1, 2 |
| Junction-to-ambient natural convection on four-layer board (2s2p) | $R_{\theta JMA}$ | 15 | °C/W | 1, 3 |
| Junction-to-ambient (@ 200 ft/min) on single-layer board (1s) | $R_{\theta JMA}$ | 17 | °C/W | 1, 3 |
| Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p) | $R_{\theta JMA}$ | 12 | °C/W | 1, 3 |
| Junction-to-board thermal | $R_{\theta JB}$ | 6 | °C/W | 4 |

required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_C$ = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$P_D$ = power dissipation (W)

# 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8347E.

## 21.1 System Clocking

The MPC8347E includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 19.1, “System PLL Configuration.”
2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, “Core PLL Configuration.”

## 21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The $AV_{DD}$ level should always equal to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 42, one to each of the four $AV_{DD}$ pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific $AV_{DD}$ pin being supplied. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of package, without the inductance of vias.

Figure 42 shows the PLL power supply filter circuit.

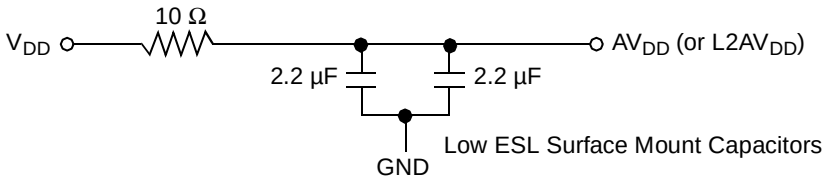



**Figure 42. PLL Power Supply Filter Circuit**

the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

## 21.7 Pull-Up Resistor Requirements

The MPC8347E requires high resistance pull-up resistors (10 kΩ is recommended) on open-drain pins, including $I^2C$ pins, the Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, *PowerQUICC™ Design Checklist*.

# 22 Document Revision History

Table 66 provides a revision history of this document.

**Table 66. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 11 | 2/2009 | In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list.<br>In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins."<br>In Table 35, removed row for rise time ($t_{I2CR}$). Removed minimum value of $t_{I2CF}$. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the $t_{I2CF}$ AC parameter.<br>In Table 54, corrected the max csb_clk to 266 MHz.<br>In Table 60, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz<br>In Table 35, corrected $t_{LBKHOV}$ parametr to $t_{LBKLOV}$ (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 21, Figure 23, and Figure 24 for output signals.<br>Added Figure 1 and Figure 4.<br>In Table 9.2, clarified that AC table is for ULPI only.<br>Added footnote 4 to Table 67.<br>In Table 67, updated note 1 to say the following: "For temperature range = C, processor frequency is up to 667(TBGA) with a platform frequency of 333 and limited to 400 (PBGA) with a platform frequency of 266."<br>Added footnote 10 and 11 to Table 51 and Table 52.<br>In Table 51, Table 52, updated note 11 to say the following: "SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net."<br>Added footnote 6 to Table 7.<br>In Table 7, updated the note 6 to say the following: "The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency."<br>In 8.1.1, removed the note "The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver power supply (that is, a RGMII driver powered from a 3.6 V supply driving VOH into a RGMII receiver powered from a 2.5-V supply). Tolerance for dissimilar RGMII driver and receiver supply potentials is implicit in these specifications." |
| 10 | 4/2007 | In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row.<br>In Table 54, "Operating Frequencies for TBGA," added column for 400 MHz.<br>In Section 21.7, "Pull-Up Resistor Requirements," deleted last two paragraphs and after first paragraph, added a new paragraph.<br>Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection." |
| 9 | 3/2007 | In Table 54, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (*csb_clk*)' row, changed the value in the 533 MHz column to 100–333.<br>In Table 60, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110.<br>In Section 23, "Ordering Information," replaced first paragraph and added a note.<br>In Section 23.1, "Part Numbers Fully Addressed by This Document," replaced first paragraph. |