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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347eczujfb

1 Overview

This section provides a high-level overview of the MPC8347E features. [Figure 1](#) shows the major functional units within the MPC8347E.

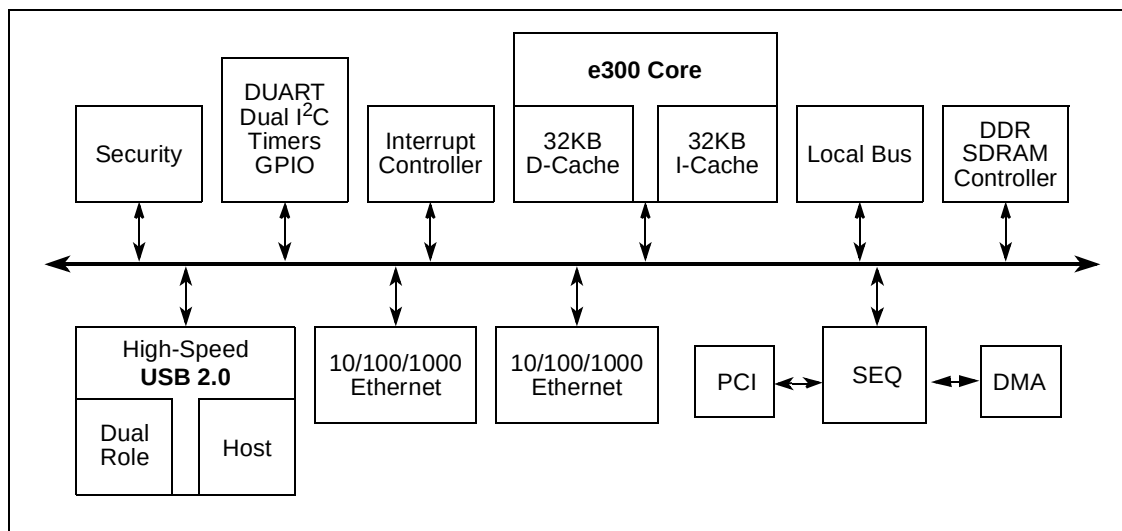


Figure 1. MPC8347E Block Diagram

Major features of the MPC8347E are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR SDRAM memory controller
 - Programmable timing for DDR-1 SDRAM
 - 32- or 64-bit data interface, up to 333-MHz data rate for TBGA, 266 MHz for PBGA
 - Four banks of memory, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbit to 1 Gbit with x8/x16 data ports
 - Full error checking and correction (ECC) support
 - Page mode support (up to 16 simultaneous open pages)
 - Contiguous or discontiguous memory mapping
 - Read-modify-write support
 - Sleep mode for self-refresh SDRAM
 - Auto refresh

- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3ac® standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- PCI interface
 - Designed to comply with *PCI Specification Revision 2.2*
 - Data bus width:
 - 32-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities
 - PCI agent mode on PCI interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration supporting five masters on PCI
 - Accesses to all PCI address spaces
 - Parity supported
 - Selectable hardware-enforced coherency
 - Address translation units for address mapping between host and peripheral
 - Dual address cycle for target
 - Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms

3 Power Characteristics

The estimated typical power dissipation for the MPC8347E device is shown in [Table 4](#).

Table 4. MPC8347E Power Dissipation¹

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T _J = 65	Typical ^{2,3}	Maximum ⁴	Unit
PBGA	266	266	1.3	1.6	1.8	W
		133	1.1	1.4	1.6	W
	400	266	1.5	1.9	2.1	W
		133	1.4	1.7	1.9	W
	400	200	1.5	1.8	2.0	W
		100	1.3	1.7	1.9	W
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W

¹ The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see [Table 5](#).

² Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.

³ Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.

⁴ Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8347E.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8347E.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	−0.3	0.4	V
CLKIN input current	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0\text{ V} \leq V_{IN} \leq 0.5\text{ V}$ or $OV_{DD} - 0.5\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5\text{ V} \leq V_{IN} \leq OV_{DD} - 0.5\text{ V}$	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8347E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8347E.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

- Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at −20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
- The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8347E.

7.1 DUART DC Electrical Characteristics

Table 17 provides the DC electrical characteristics for the DUART interface of the MPC8347E.

Table 17. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($0.8\text{ V} \leq V_{IN} \leq 2\text{ V}$)	I_{IN}	—	± 5	μA
High-level output voltage, $I_{OH} = -100\text{ }\mu\text{A}$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100\text{ }\mu\text{A}$	V_{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 18 provides the AC timing parameters for the DUART interface of the MPC8347E.

Table 18. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

Figure 13 shows the TBI transmit AC timing diagram.

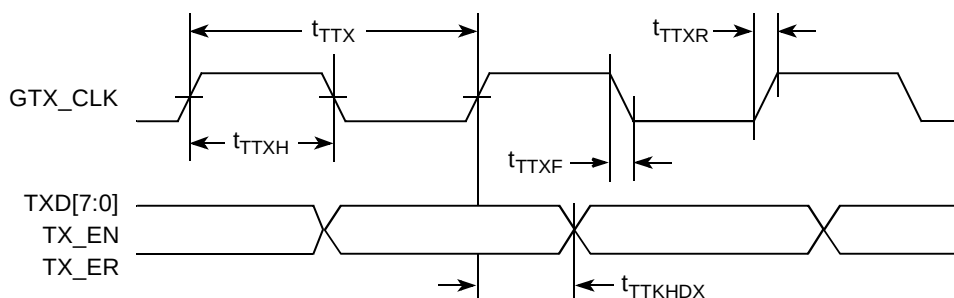


Figure 13. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 26 provides the TBI receive AC timing specifications.

Table 26. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
PMA_RX_CLK clock period	t_{TRX}		16.0		ns
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t_{TRDVKH}^2	2.5	—	—	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t_{TRDXKH}^2	1.5	—	—	ns
RX_CLK clock rise time $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{TRXF}	0.7	—	2.4	ns

Notes:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
- Setup and hold time of even numbered RCG are measured from the rising edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the rising edge of PMA_RX_CLK0.

Figure 15 shows the RBMII and RTBI AC timing and multiplexing diagrams.

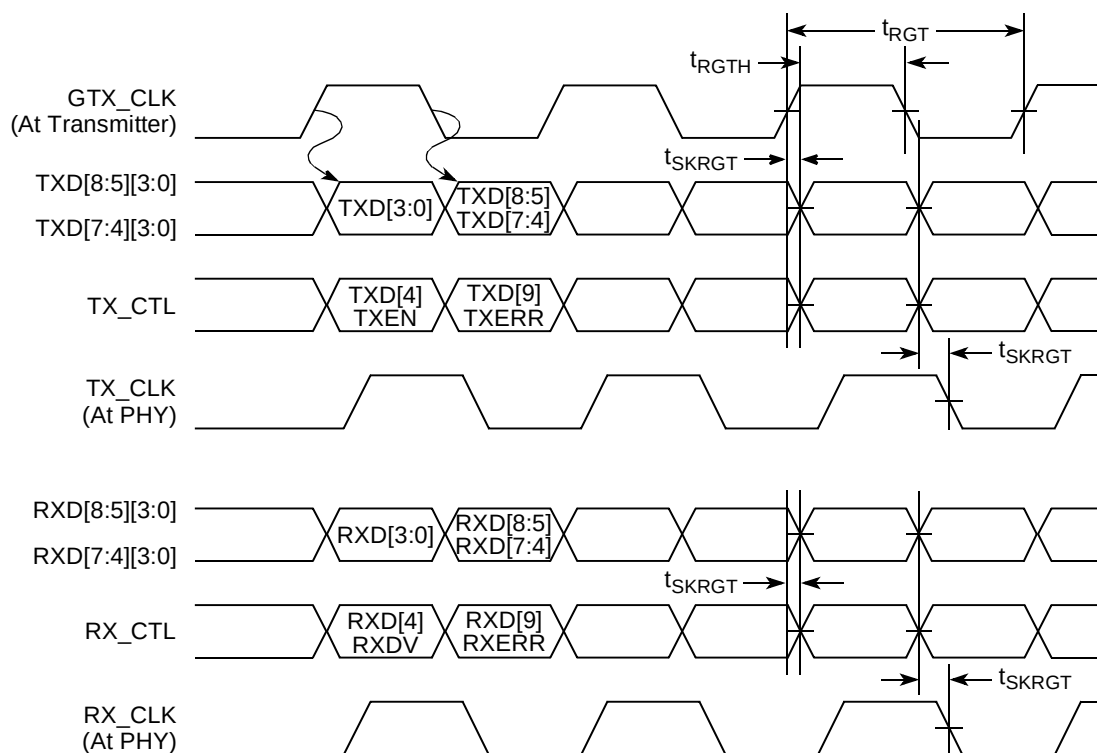


Figure 15. RGMII and RTBI AC Timing and Multiplexing Diagrams

Table 41. PCI AC Timing Specifications at 66 MHz¹ (continued)

Parameter	Symbol ²	Min	Max	Unit	Notes
Input hold from clock	t_{PCIXKH}	0	—	ns	3, 5

Notes:

1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
2. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
3. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

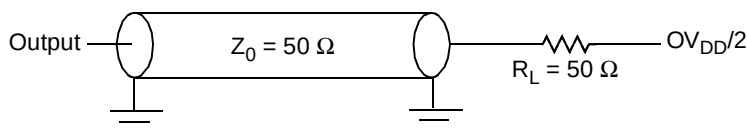
Table 42. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

Figure 33 provides the AC test load for PCI.

**Figure 33. PCI AC Test Load**

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8347E is available in two packages—a tape ball grid array (TBGA) and a plastic ball grid array (PBGA). See [Section 18.1, “Package Parameters for the MPC8347E TBGA,”](#) [Section 18.2, “Mechanical Dimensions for the MPC8347E TBGA,”](#) [Section 18.3, “Package Parameters for the MPC8347E PBGA,”](#) and [Section 18.4, “Mechanical Dimensions for the MPC8347E PBGA.”](#)

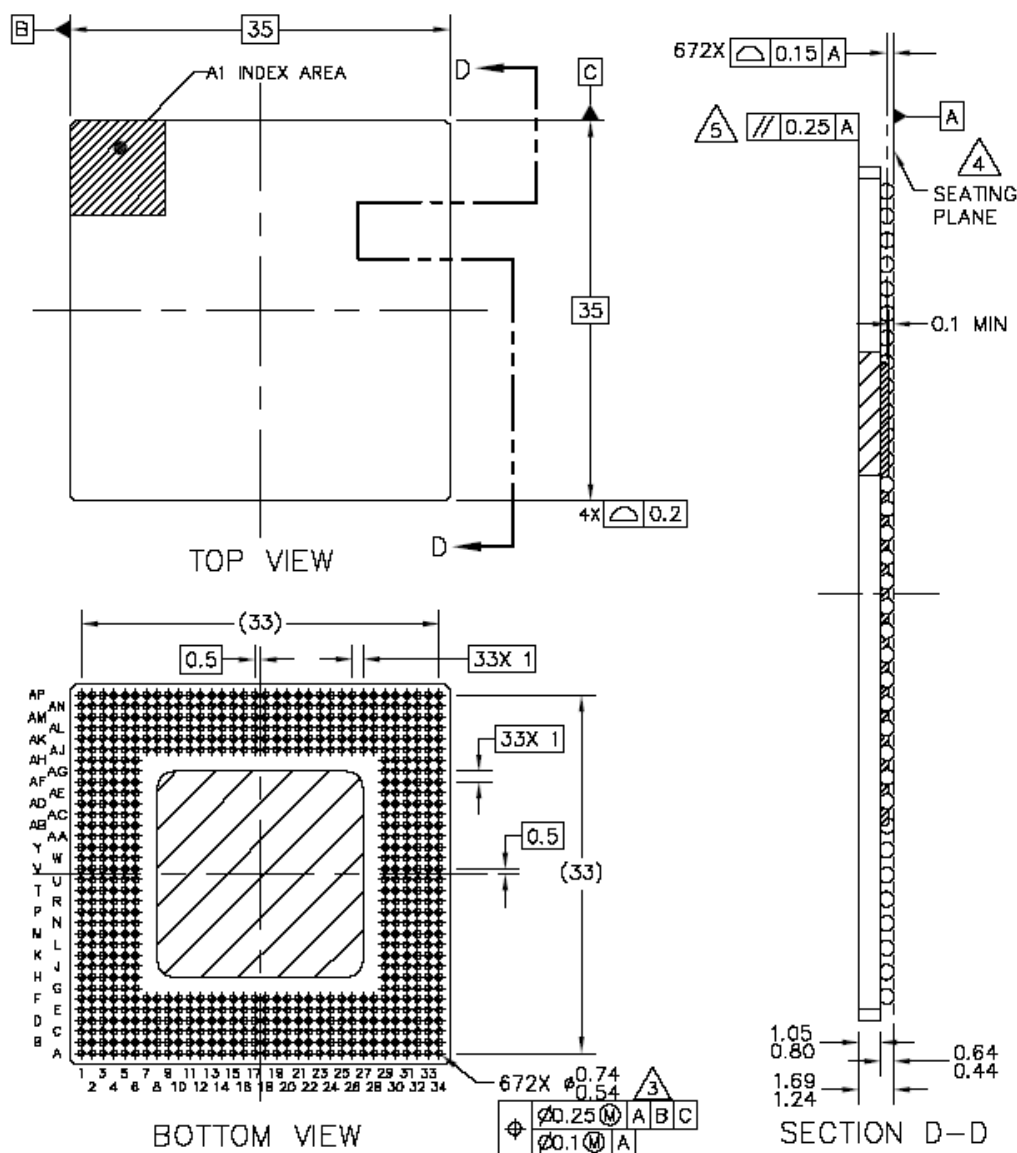
18.1 Package Parameters for the MPC8347E TBGA

The package parameters are provided in the following list. The package type is 35 mm × 35 mm, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm

18.2 Mechanical Dimensions for the MPC8347E TBGA

Figure 39 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 672-TBGA package.



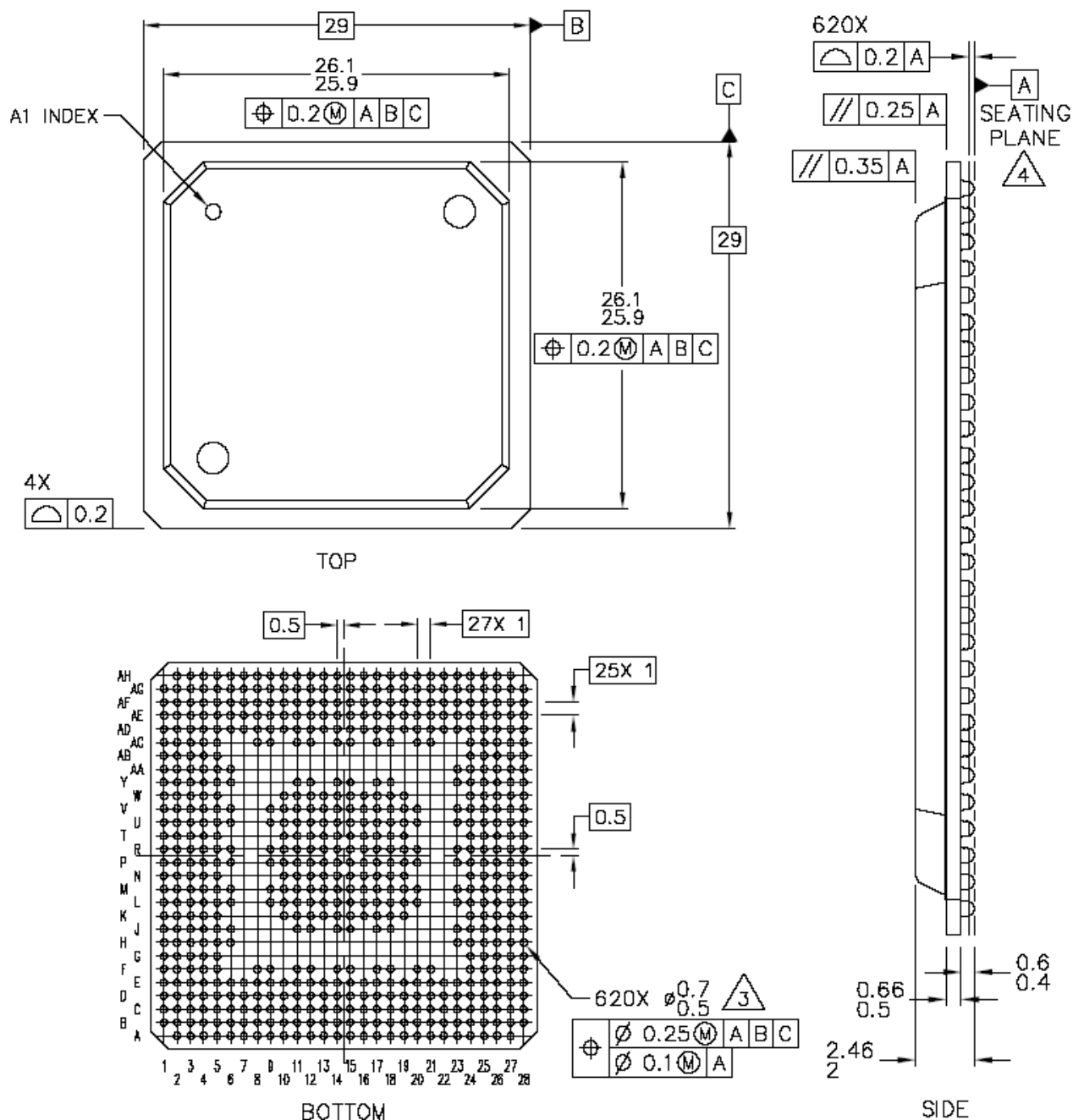
Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 39. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E TBGA

18.4 Mechanical Dimensions for the MPC8347E PBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 620-PBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E PBGA

18.5 Pinout Listings

Table 51 provides the pinout listing for the MPC8347E, 672 TBGA package.

Table 51. MPC8347E (TBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_INTA/IRQ_OUT	B34	O	OV _{DD}	2
PCI_RESET_OUT	C33	O	OV _{DD}	
PCI_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV _{DD}	
PCI_C/BE[3:0]	J30, M31, P33, T34	I/O	OV _{DD}	
PCI_PAR	P32	I/O	OV _{DD}	
PCI_FRAME	M32	I/O	OV _{DD}	5
PCI_TRDY	N29	I/O	OV _{DD}	5
PCI_IRDY	M34	I/O	OV _{DD}	5
PCI_STOP	N31	I/O	OV _{DD}	5
PCI_DEVSEL	N30	I/O	OV _{DD}	5
PCI_IDSEL	J31	I	OV _{DD}	
PCI_SERR	N34	I/O	OV _{DD}	5
PCI_PERR	N33	I/O	OV _{DD}	5
PCI_REQ[0]	D32	I/O	OV _{DD}	
PCI_REQ[1]/CPCI1_HS_ES	D34	I	OV _{DD}	
PCI_REQ[2:4]	E34, F32, G29	I	OV _{DD}	
PCI_GNT0	C34	I/O	OV _{DD}	
PCI_GNT1/CPCI1_HS_LED	D33	O	OV _{DD}	
PCI_GNT2/CPCI1_HS_ENUM	E33	O	OV _{DD}	
PCI_GNT[3:4]	F31, F33	O	OV _{DD}	
M66EN	A19	I	OV _{DD}	
DDR SDRAM Memory Interface				
MDQ[0:63]	D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8	I/O	GV _{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connection				
NC	W32, AA31, AA32, AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30, AC32, AE32, AH31, AL32, AG34, AE33, AF32, AE34, AF34, AF33, AG33, AG32, AL11, AM11, AP10, Y32, Y34, Y31, Y33	—	—	

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be pulled up to OV_{DD}.
8. This pin must always be left not connected.
9. Thermal sensitive resistor.
10. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
11. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

Table 52 provides the pinout listing for the MPC8347E, 620 PBGA package.

Table 52. MPC8347E (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI1_INTA/IRQ_OUT	D20	O	OV _{DD}	2
PCI1_RESET_OUT	B21	O	OV _{DD}	
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV _{DD}	
PCI1_C/BE[3:0]	A17, A14, A11, B10	I/O	OV _{DD}	
PCI1_PAR	D13	I/O	OV _{DD}	
PCI1_FRAME	B14	I/O	OV _{DD}	5
PCI1_TRDY	A13	I/O	OV _{DD}	5

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCAS}}$	AG6	O	GV_{DD}	
$\overline{\text{MCS}}[0:3]$	AE7, AH7, AH4, AF2	O	GV_{DD}	
$\text{MCKE}[0:1]$	AG23, AH23	O	GV_{DD}	3
$\text{MCK}[0:5]$	AH15, AE24, AE2, AF14, AE23, AD3	O	GV_{DD}	
$\overline{\text{MCK}}[0:5]$	AG15, AD23, AE3, AG14, AF24, AD2	O	GV_{DD}	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
$\text{MODT}[0:3]$	AG5, AD4, AH6, AF4	—	—	
$\text{MBA}[2]$	AD22			
SPARE1	AF12	—	—	7
SPARE2	AG11	—	—	6
Local Bus Controller Interface				
$\text{LAD}[0:31]$	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV_{DD}	
$\text{LDP}[0]/\overline{\text{CKSTOP_OUT}}$	H1	I/O	OV_{DD}	
$\text{LDP}[1]/\overline{\text{CKSTOP_IN}}$	K5	I/O	OV_{DD}	
$\text{LDP}[2]$	H2	I/O	OV_{DD}	
$\text{LDP}[3]$	G1	I/O	OV_{DD}	
$\text{LA}[27:31]$	J4, H3, G2, F1, G3	O	OV_{DD}	
$\overline{\text{LCS}}[0:3]$	J5, H4, F2, E1	O	OV_{DD}	
$\overline{\text{LWE}}[0:3]/\text{LSDDQM}[0:3]/\overline{\text{LBS}}[0:3]$	F3, G4, D1, E2	O	OV_{DD}	
LBCTL	H5	O	OV_{DD}	
LALE	E3	O	OV_{DD}	
$\text{LGPL0}/\text{LSDA10}/\text{cfg_reset_source0}$	F4	I/O	OV_{DD}	
$\text{LGPL1}/\overline{\text{LSDWE}}/\text{cfg_reset_source1}$	D2	I/O	OV_{DD}	
$\text{LGPL2}/\overline{\text{LSDRAS}}/\text{LOE}$	C1	O	OV_{DD}	
$\text{LGPL3}/\overline{\text{LSDCAS}}/\text{cfg_reset_source2}$	C2	I/O	OV_{DD}	
$\text{LGPL4}/\overline{\text{LGTA}}/\text{LUPWAIT}/\text{LPBSE}$	C3	I/O	OV_{DD}	
$\text{LGPL5}/\text{cfg_clkin_div}$	B3	I/O	OV_{DD}	
LCKE	E4	O	OV_{DD}	
$\text{LCLK}[0:2]$	D4, A3, C4	O	OV_{DD}	
LSYNC_OUT	U3	O	OV_{DD}	
LSYNC_IN	Y2	I	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV _{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV _{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV _{DD}	
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV _{DD}	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV _{DD}	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV _{DD}	
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV _{DD}	
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV _{DD}	
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV _{DD}	
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV _{DD}	
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV _{DD}	
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV _{DD}	
MPH0_CLK/DR_RX_VALID	C21	I	OV _{DD}	
Programmable Interrupt Controller				
MCP_OUT	E8	O	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	J28	I/O	OV _{DD}	
IRQ[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV _{DD}	
IRQ[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV _{DD}	
IRQ[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV _{DD}	
Ethernet Management Interface				
EC_MDC	Y24	O	LV _{DD1}	
EC_MDIO	Y25	I/O	LV _{DD1}	2
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV _{DD1}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV _{DD}	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV _{DD1}	
TSEC1_GTX_CLK	V24	O	LV _{DD1}	3
TSEC1_RX_CLK	U26	I	LV _{DD1}	
TSEC1_RX_DV	U24	I	LV _{DD1}	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV _{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV _{DD}	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV _{DD1}	
TSEC1_TX_CLK	N25	I	OV _{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[7:4]/GPIO2[27:30]	N28, P25, P26, P27	I/O	OV _{DD}	
TSEC1_TXD[3:0]	V28, V27, V26, W28	O	LV _{DD1}	10
TSEC1_TX_EN	W27	O	LV _{DD1}	
TSEC1_TX_ER/GPIO2[31]	N24	I/O	OV _{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	P28	I/O	OV _{DD}	
TSEC2_CRS/GPIO1[22]	AC28	I/O	LV _{DD2}	
TSEC2_GTX_CLK	AC27	O	LV _{DD2}	
TSEC2_RX_CLK	AB25	I	LV _{DD2}	
TSEC2_RX_DV/GPIO1[23]	AC26	I/O	LV _{DD2}	
TSEC2_RXD[7:4]/GPIO1[26:29]	R28, T24, T25, T26	I/O	OV _{DD}	
TSEC2_RXD[3:0]/GPIO1[13:16]	AA25, AA26, AA27, AA28	I/O	LV _{DD2}	
TSEC2_RX_ER/GPIO1[25]	R25	I/O	OV _{DD}	
TSEC2_TXD[7]/GPIO1[31]	T27	I/O	OV _{DD}	
TSEC2_TXD[6]/DR_XCVR_TERM_SEL	T28	O	OV _{DD}	
TSEC2_TXD[5]/DR_UTMI_OPMODE1	U28	O	OV _{DD}	
TSEC2_TXD[4]/DR_UTMI_OPMODE0	U27	O	OV _{DD}	
TSEC2_TXD[3:0]/GPIO1[17:20]	AB26, AB27, AA24, AB28	I/O	LV _{DD2}	
TSEC2_TX_ER/GPIO1[24]	R27	I/O	OV _{DD}	
TSEC2_TX_EN/GPIO1[12]	AD28	I/O	LV _{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	R26	I/O	OV _{DD}	
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	B4, A4	O	OV _{DD}	
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	D5, C5	I/O	OV _{DD}	
UART_CTS[1]/MSRCID4/LSRCID4	B5	I/O	OV _{DD}	
UART_CTS[2]/MDVAL/LDVAL	A5	I/O	OV _{DD}	
UART_RTS[1:2]	D6, C6	O	OV _{DD}	
I²C interface				
IIC1_SDA	E5	I/O	OV _{DD}	2
IIC1_SCL	A6	I/O	OV _{DD}	2
IIC2_SDA	B6	I/O	OV _{DD}	2
IIC2_SCL	E7	I/O	OV _{DD}	2
SPI				
SPIMOSI	D7	I/O	OV _{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF1	AF19	I	DDR reference voltage	
MVREF2	AE10	I	DDR reference voltage	
No Connection				
NC	V1, V2, V5			

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be left not connected.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
10. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

Table 57. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk : Input Clock Ratio ²	Input Clock Frequency (MHz) ²					
			16.67	25	33.33	66.67		
			csb_clk Frequency (MHz)					
Low	0010	2 : 1				133		
Low	0011	3 : 1				100	200	
Low	0100	4 : 1				100	133	266
Low	0101	5 : 1				125	166	333
Low	0110	6 : 1	100	150	200			
Low	0111	7 : 1	116	175	233			
Low	1000	8 : 1	133	200	266			
Low	1001	9 : 1	150	225	300			
Low	1010	10 : 1	166	250	333			
Low	1011	11 : 1	183	275				
Low	1100	12 : 1	200	300				
Low	1101	13 : 1	216	325				
Low	1110	14 : 1	233					
Low	1111	15 : 1	250					
Low	0000	16 : 1	266					
High	0010	2 : 1					133	
High	0011	3 : 1					100	200
High	0100	4 : 1					133	266
High	0101	5 : 1					166	333
High	0110	6 : 1		200				
High	0111	7 : 1		233				
High	1000	8 : 1						

¹ CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

20 Thermal

This section describes the thermal specifications of the MPC8347E.

20.1 Thermal Characteristics

Table 61 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8347E.

Table 61. Package Thermal Characteristics for TBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	3.8	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.7	°C/W	5
Junction-to-package natural convection on top	Ψ_{JT}	1	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 62 provides the package thermal characteristics for the 620 29 × 29 mm PBGA of the MPC8347E.

Table 62. Package Thermal Characteristics for PBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	17	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	12	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	°C/W	4

the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8347E requires high resistance pull-up resistors (10 k Ω is recommended) on open-drain pins, including I²C pins, the Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, *PowerQUICC™ Design Checklist*.