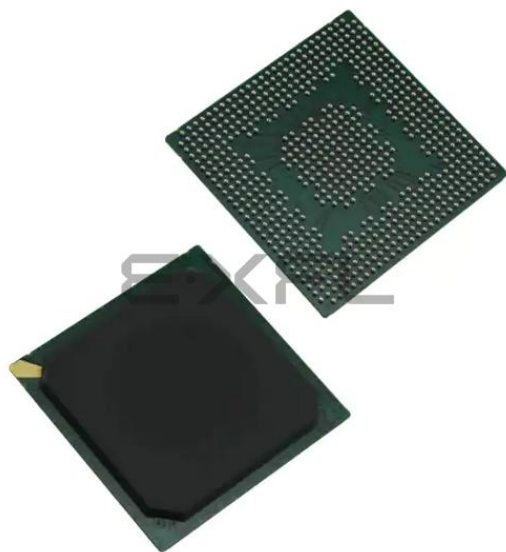




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347evradd

- Enhanced host controller interface (EHCI) compatible
 - Complies with *USB Specification Rev. 2.0*
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
 - Direct connection to a high-speed device without an external hub
 - External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Four chip selects support four external slaves
 - Up to eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
 - Three protocol engines on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user-programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for 8 external and 35 internal discrete interrupt sources
 - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
 - Programmable highest priority request
 - Four groups of interrupts with programmable priority
 - External and internal interrupts directed to host processor
 - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
 - Unique vector number for each interrupt source
- Dual industry-standard I²C interfaces
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
 - System initialization data optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - All channels accessible to local core and remote PCI masters
 - Misaligned transfer capability

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8347E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	$1.2\text{ V} \pm 60\text{ mV}$	V	1
PLL supply voltage	AV_{DD}	$1.2\text{ V} \pm 60\text{ mV}$	V	1
DDR DRAM I/O supply voltage	GV_{DD}	$2.5\text{ V} \pm 125\text{ mV}$	V	
Three-speed Ethernet I/O supply voltage	LV_{DD1}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	
Three-speed Ethernet I/O supply voltage	LV_{DD2}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage	OV_{DD}	$3.3\text{ V} \pm 330\text{ mV}$	V	

Note:

¹ GV_{DD} , LV_{DD} , OV_{DD} , AV_{DD} , and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8347E.

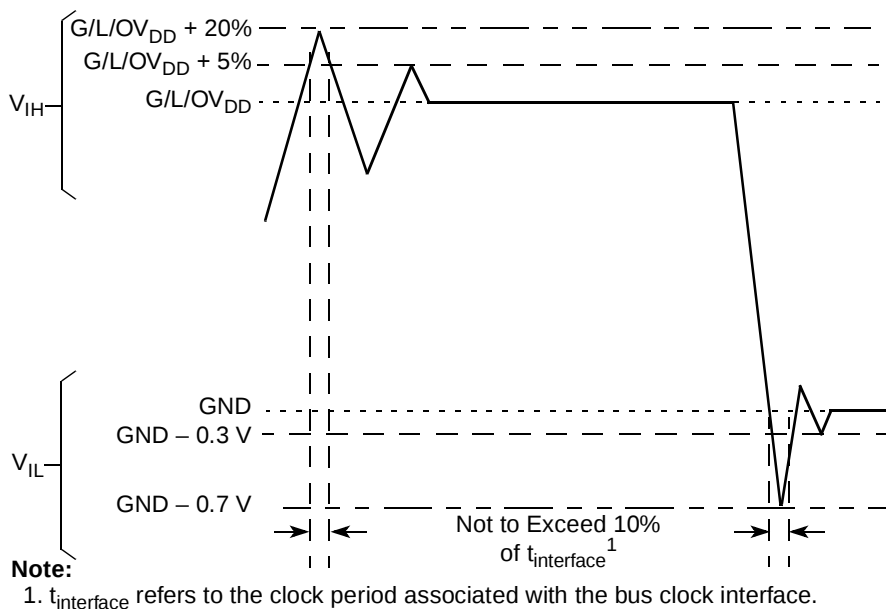


Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8347E for the 3.3-V signals, respectively.

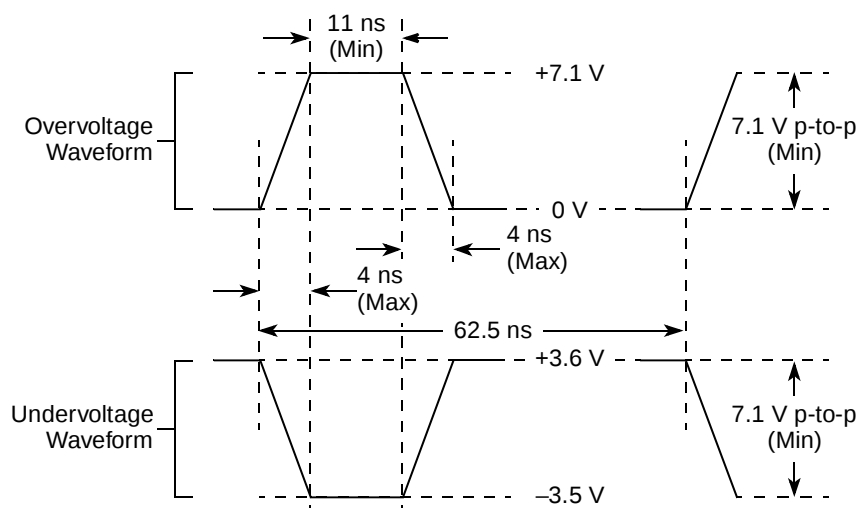


Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	$OV_{DD} = 3.3\text{ V}$
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	$GV_{DD} = 2.5\text{ V}$
TSEC/10/100 signals	40	$LV_{DD} = 2.5/3.3\text{ V}$
DUART, system control, I ² C, JTAG, USB	40	$OV_{DD} = 3.3\text{ V}$
GPIO signals	40	$OV_{DD} = 3.3\text{ V}$, $LV_{DD} = 2.5/3.3\text{ V}$

2.2 Power Sequencing

MPC8347E does not require the core supply voltage and I/O supply voltages to be applied in any particular order. Note that during the power ramp up, before the power supplies are stable, there may be a period of time that I/O pins are actively driven. After the power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most I/O pins are three-stated. To minimize the time that I/O pins are actively driven, it is recommended to apply core voltage before I/O voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up.

3 Power Characteristics

The estimated typical power dissipation for the MPC8347E device is shown in [Table 4](#).

Table 4. MPC8347E Power Dissipation¹

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T _J = 65	Typical ^{2,3}	Maximum ⁴	Unit
PBGA	266	266	1.3	1.6	1.8	W
		133	1.1	1.4	1.6	W
	400	266	1.5	1.9	2.1	W
		133	1.4	1.7	1.9	W
	400	200	1.5	1.8	2.0	W
		100	1.3	1.7	1.9	W
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W

¹ The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see [Table 5](#).

² Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.

³ Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.

⁴ Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous ModeAt recommended operating conditions with GV_{DD} of 2.5 V $\pm$ 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/ $\overline{\text{MCK}}[n]$ crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t_{AOSKEW}	–1000 –1100 –1200	200 300 400	ps	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	2.8 3.45 4.6	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	2.0 2.65 3.8	—	ns	4
$\overline{\text{MCS}}(n)$ output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	2.8 3.45 4.6	—	ns	4
$\overline{\text{MCS}}(n)$ output hold with respect to MCK 333 MHz 266 MHz 200 MHz	$t_{DDKHCSX}$	2.0 2.65 3.8	—	ns	4
MCK to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKMHM}	–0.9 –1.1 –1.2	0.3 0.5 0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	900 900 1200	—	ps	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	900 900 1200	—	ps	6
MDQS preamble start	t_{DDKHMP}	$-0.25 \times t_{MCK} - 0.9$	$-0.25 \times t_{MCK} + 0.3$	ns	7

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8347E.

7.1 DUART DC Electrical Characteristics

Table 17 provides the DC electrical characteristics for the DUART interface of the MPC8347E.

Table 17. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($0.8\text{ V} \leq V_{IN} \leq 2\text{ V}$)	I_{IN}	—	± 5	μA
High-level output voltage, $I_{OH} = -100\text{ }\mu\text{A}$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100\text{ }\mu\text{A}$	V_{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 18 provides the AC timing parameters for the DUART interface of the MPC8347E.

Table 18. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to the gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.3](#), “Ethernet Management Interface Electrical Characteristics.”

8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 19](#) and [Table 20](#). The RGMII and RTBI signals in [Table 20](#) are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 19. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}^2	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.40	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	40	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-600	—	μA

Notes:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).
2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Figure 8 shows the GMII transmit AC timing diagram.

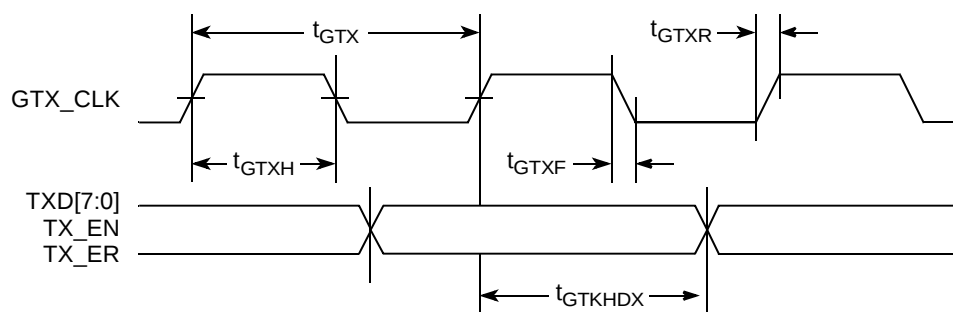


Figure 8. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 22 provides the GMII receive AC timing specifications.

Table 22. GMII Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise, $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time, $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{GRXF}	—	—	1.0	ns

Note:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 shows the MII receive AC timing diagram.

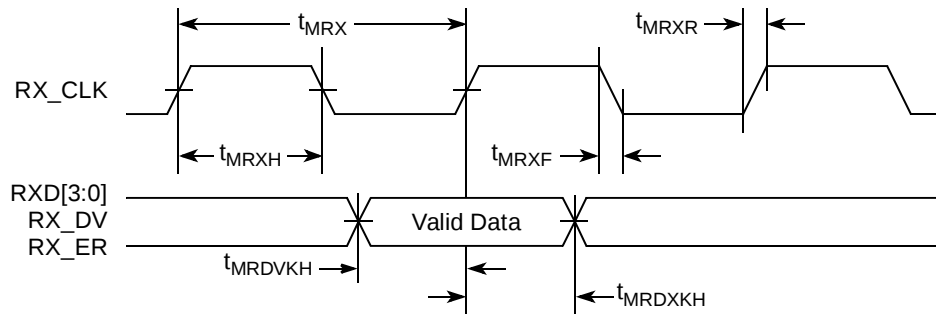


Figure 12. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 25 provides the TBI transmit AC timing specifications.

Table 25. TBI Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t_{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise, $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time, $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{TTXF}	—	—	1.0	ns
GTX_CLK125 reference clock period	t_{G125}^2	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	45	—	55	ns

Notes:

- The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in [Section 8.1, “Three-Speed Ethernet Controller \(TSEC\)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”](#)

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 28](#) and [Table 29](#).

Table 28. MII Management DC Electrical Characteristics Powered at 2.5 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (2.5 V)	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	$\text{GND} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$LV_{DD} = \text{Min}$	1.7	—	V
Input low voltage	V_{IL}	—	$LV_{DD} = \text{Min}$	-0.3	0.70	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN} = LV_{DD}$		-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

Table 29. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	LV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.10	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	$LV_{DD} = \text{Max}$	$V_{IN}^1 = 2.1 \text{ V}$	—	40	μA
Input low current	I_{IL}	$LV_{DD} = \text{Max}$	$V_{IN} = 0.5 \text{ V}$	-600	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8347E.

10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

Table 33. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current	I_{IN}	—	± 5	μA
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V

10.2 Local Bus AC Electrical Specification

Table 34 and Table 35 describe the general timing parameters of the local bus interface of the MPC8347E.

Table 34. Local Bus General Timing Parameters—DLL On

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3

Table 34. Local Bus General Timing Parameters—DLL On (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Table 35. Local Bus General Timing Parameters—DLL Bypass⁹

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7

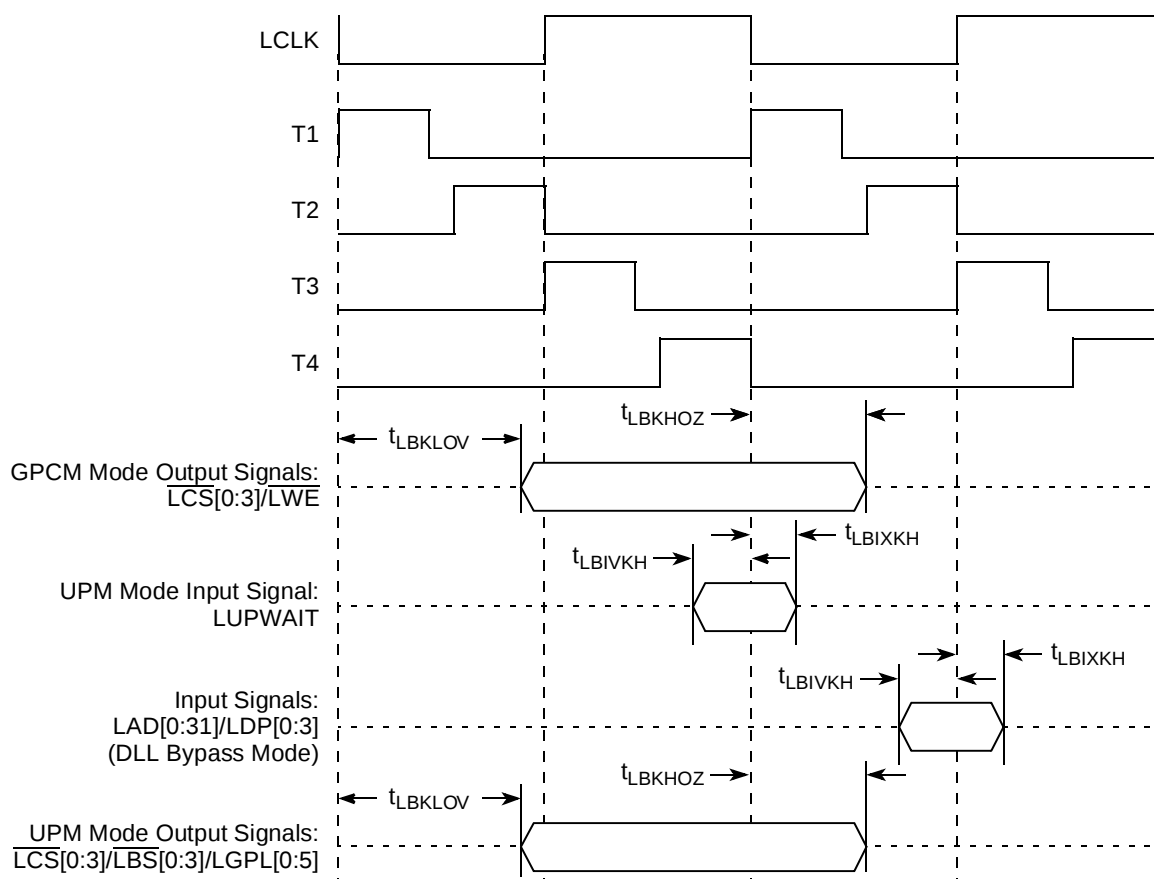


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

Figure 36 provides the AC test load for the SPI.

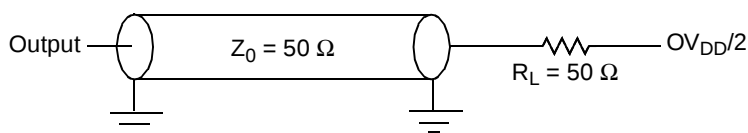
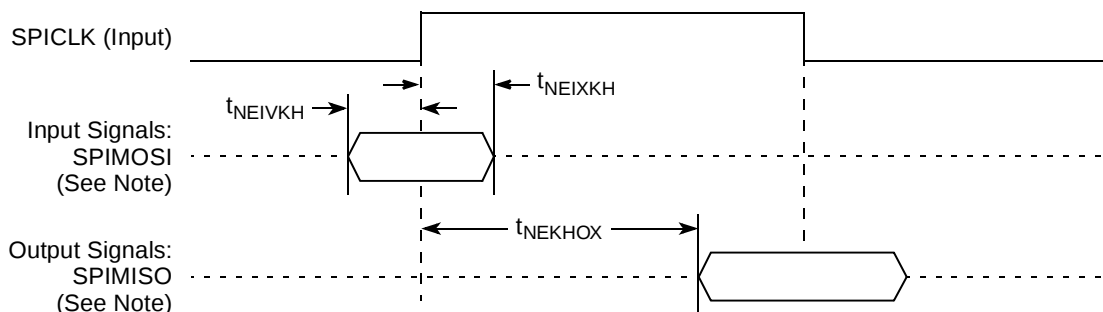


Figure 36. SPI AC Test Load

Figure 37 and Figure 38 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

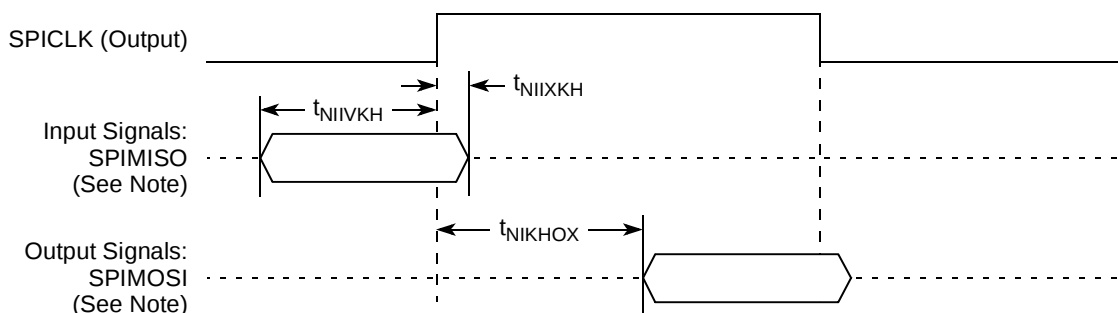
Figure 37 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 37. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 38 shows the SPI timings in master mode (internal clock).

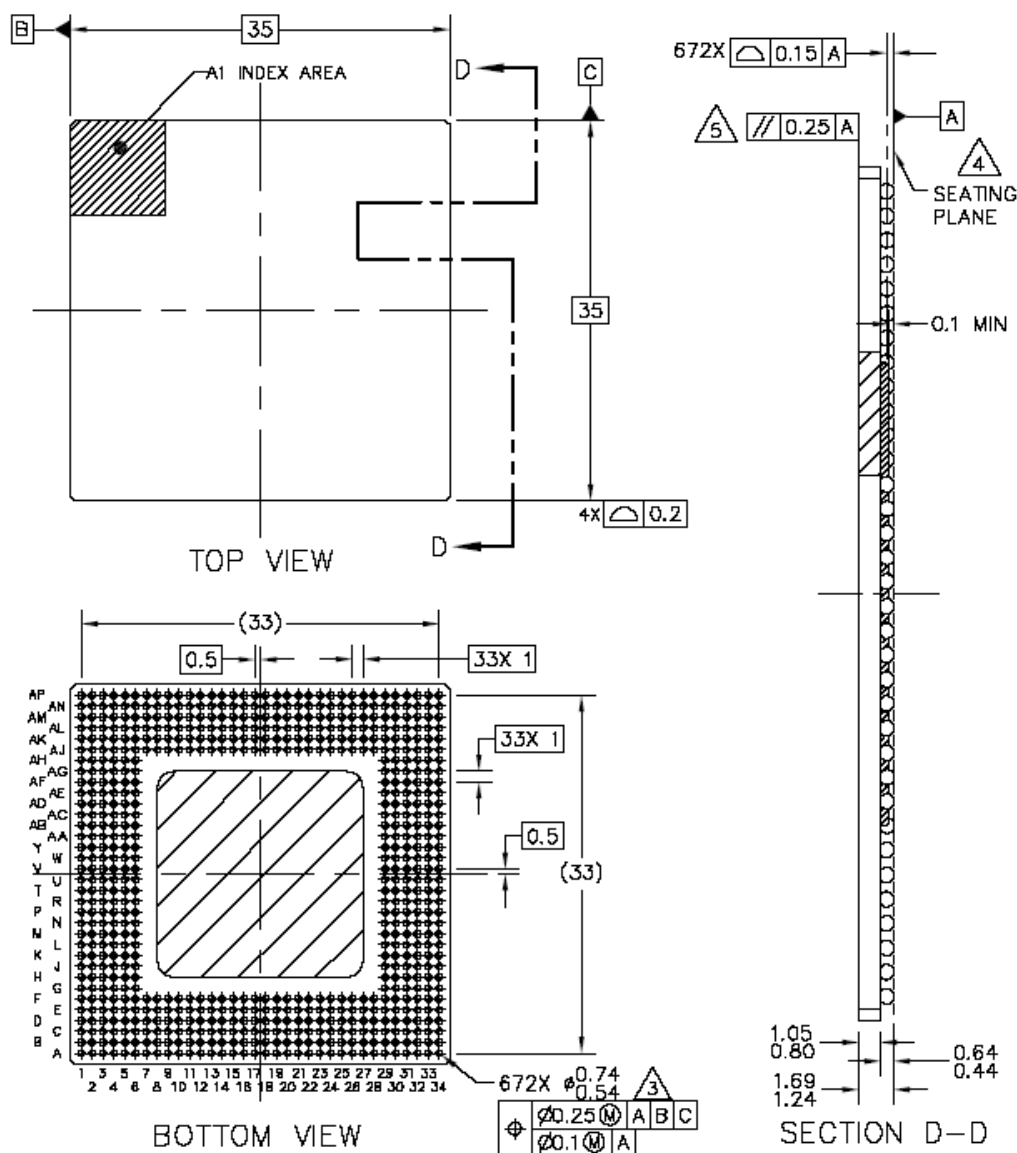


Note: The clock edge is selectable on SPI.

Figure 38. SPI AC Timing in Master Mode (Internal Clock) Diagram

18.2 Mechanical Dimensions for the MPC8347E TBGA

Figure 39 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 672-TBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 39. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E TBGA

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LBCTL	AN26	O	OV _{DD}	
LALE	AK24	O	OV _{DD}	
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV _{DD}	
LGPL1/LSDWE/cfg_reset_source1	AL25	I/O	OV _{DD}	
LGPL2/LSDRAS/LOE	AJ24	O	OV _{DD}	
LGPL3/LSDCAS/cfg_reset_source2	AN27	I/O	OV _{DD}	
LGPL4/LGTA/LUPWAIT/LPBSE	AP28	I/O	OV _{DD}	
LGPL5/cfg_clkin_div	AL26	I/O	OV _{DD}	
LCKE	AM27	O	OV _{DD}	
LCLK[0:2]	AN28, AK26, AP29	O	OV _{DD}	
LSYNC_OUT	AM12	O	OV _{DD}	
LSYNC_IN	AJ10	I	OV _{DD}	
General Purpose I/O Timers				
GPIO1[0]/GTM1_TIN1/GTM2_TIN2	F24	I/O	OV _{DD}	
GPIO1[1]/GTM1_TGATE1/GTM2_TGATE2	E24	I/O	OV _{DD}	
GPIO1[2]/GTM1_TOUT1	B25	I/O	OV _{DD}	
GPIO1[3]/GTM1_TIN2/GTM2_TIN1	D24	I/O	OV _{DD}	
GPIO1[4]/GTM1_TGATE2/GTM2_TGATE1	A25	I/O	OV _{DD}	
GPIO1[5]/GTM1_TOUT2/GTM2_TOUT1	B24	I/O	OV _{DD}	
GPIO1[6]/GTM1_TIN3/GTM2_TIN4	A24	I/O	OV _{DD}	
GPIO1[7]/GTM1_TGATE3/GTM2_TGATE4	D23	I/O	OV _{DD}	
GPIO1[8]/GTM1_TOUT3	B23	I/O	OV _{DD}	
GPIO1[9]/GTM1_TIN4/GTM2_TIN3	A23	I/O	OV _{DD}	
GPIO1[10]/GTM1_TGATE4/GTM2_TGATE3	F22	I/O	OV _{DD}	
GPIO1[11]/GTM1_TOUT4/GTM2_TOUT3	E22	I/O	OV _{DD}	
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	A26	I/O	OV _{DD}	
MPH1_D1_SER_TXD/DR_D1_SER_TXD	B26	I/O	OV _{DD}	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	D25	I/O	OV _{DD}	
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV _{DD}	
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV _{DD}	
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV _{DD}	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	D26	I/O	OV _{DD}	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	E26	I/O	OV _{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Gigabit Reference Clock				
EC_GTX_CLK125	C8	I	LV _{DD1}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	A17	I/O	OV _{DD}	
TSEC1_CRS/GPIO2[21]	F12	I/O	LV _{DD1}	
TSEC1_GTX_CLK	D10	O	LV _{DD1}	3
TSEC1_RX_CLK	A11	I	LV _{DD1}	
TSEC1_RX_DV	B11	I	LV _{DD1}	
TSEC1_RX_ER/GPIO2[26]	B17	I/O	OV _{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	B16, D16, E16, F16	I/O	OV _{DD}	
TSEC1_RXD[3:0]	E10, A8, F10, B8	I	LV _{DD1}	
TSEC1_TX_CLK	D17	I	OV _{DD}	
TSEC1_TXD[7:4]/GPIO2[27:30]	A15, B15, A14, B14	I/O	OV _{DD}	
TSEC1_TXD[3:0]	A10, E11, B10, A9	O	LV _{DD1}	11
TSEC1_TX_EN	B9	O	LV _{DD1}	
TSEC1_TX_ER/GPIO2[31]	A16	I/O	OV _{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	C14	I/O	OV _{DD}	
TSEC2_CRS/GPIO1[22]	D6	I/O	LV _{DD2}	
TSEC2_GTX_CLK	A4	O	LV _{DD2}	
TSEC2_RX_CLK	B4	I	LV _{DD2}	
TSEC2_RX_DV/GPIO1[23]	E6	I/O	LV _{DD2}	
TSEC2_RXD[7:4]/GPIO1[26:29]	A13, B13, C13, A12	I/O	OV _{DD}	
TSEC2_RXD[3:0]/GPIO1[13:16]	D7, A6, E8, B7	I/O	LV _{DD2}	
TSEC2_RX_ER/GPIO1[25]	D14	I/O	OV _{DD}	
TSEC2_TXD[7]/GPIO1[31]	B12	I/O	OV _{DD}	
TSEC2_TXD[6]/DR_XCVR_TERM_SEL	C12	O	OV _{DD}	
TSEC2_TXD[5]/DR_UTMI_OPMODE1	D12	O	OV _{DD}	
TSEC2_TXD[4]/DR_UTMI_OPMODE0	E12	O	OV _{DD}	
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV _{DD2}	
TSEC2_TX_ER/GPIO1[24]	F14	I/O	OV _{DD}	
TSEC2_TX_EN/GPIO1[12]	C5	I/O	LV _{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	E14	I/O	OV _{DD}	

Table 58. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	Input Clock Frequency (MHz) ²					
			16.67	25	33.33	66.67		
			<i>csb_clk</i> Frequency (MHz)					
Low	0010	2 : 1				133		
Low	0011	3 : 1				100	200	
Low	0100	4 : 1				100	133	266
Low	0101	5 : 1				125	166	333
Low	0110	6 : 1	100	150	200			
Low	0111	7 : 1	116	175	233			
Low	1000	8 : 1	133	200	266			
Low	1001	9 : 1	150	225	300			
Low	1010	10 : 1	166	250	333			
Low	1011	11 : 1	183	275				
Low	1100	12 : 1	200	300				
Low	1101	13 : 1	216	325				
Low	1110	14 : 1	233					
Low	1111	15 : 1	250					
Low	0000	16 : 1	266					
High	0010	4 : 1		100	133	266		
High	0011	6 : 1	100	150	200			
High	0100	8 : 1	133	200	266			
High	0101	10 : 1	166	250	333			
High	0110	12 : 1	200	300				
High	0111	14 : 1	233					
High	1000	16 : 1	266					

¹ CFG_CLKIN_DIV doubles *csb_clk* if set high.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 59 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 59 should be considered as reserved.

the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8347E requires high resistance pull-up resistors (10 k Ω is recommended) on open-drain pins, including I²C pins, the Ethernet Management MDIO pin, and IPIC interrupt pins.

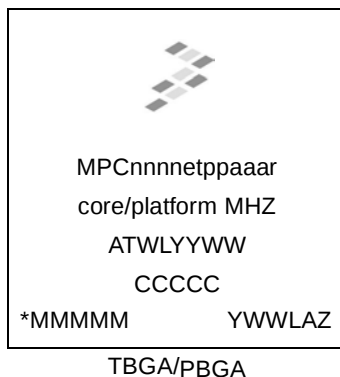
For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, *PowerQUICC™ Design Checklist*.

Table 68. SVR Settings (continued)

MPC8347E	PBGA	8054_0010
MPC8347	PBGA	8055_0010

23.2 Part Marking

Parts are marked as in the example shown in [Figure 44](#).



Notes:

ATWLYYWW is the traceability code.

CCCCC is the country code.

MMMMM is the mask number.

YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA or PBGA Devices