Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347evvajd

- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O

- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3®, 802.3u®, 820.3x®, 802.3z®, 802.3ac® standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- PCI interface
  - Designed to comply with *PCI Specification Revision 2.2*
  - Data bus width:
    - 32-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities
  - PCI agent mode on PCI interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration supporting five masters on PCI
  - Accesses to all PCI address spaces
  - Parity supported
  - Selectable hardware-enforced coherency
  - Address translation units for address mapping between host and peripheral
  - Dual address cycle for target
  - Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
  - Public key execution unit (PKEU) :
    - RSA and Diffie-Hellman algorithms

  - Programmable field size up to 2048 bits
  - Elliptic curve cryptography
  - F2m and F(p) modes
  - Programmable field size up to 511 bits
- Data encryption standard (DES) execution unit (DEU)
  - DES and 3DES algorithms
  - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
  - ECB and CBC modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rijndael symmetric-key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, and counter (CTR) modes
- ARC four execution unit (AFEU)
  - Stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
  - Static and/or dynamic assignment of crypto-execution units through an integrated controller
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

• Universal serial bus (USB) dual role controller
  - USB on-the-go mode with both device and host functionality
  - Complies with USB specification Rev. 2.0
  - Can operate as a stand-alone USB device
    - One upstream facing port
    - Six programmable USB endpoints
  - Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)

• Universal serial bus (USB) multi-port host controller
  - Can operate as a stand-alone USB host controller
    - USB root hub with one or two downstream-facing ports

    – Enhanced host controller interface (EHCI) compatible
    – Complies with *USB Specification Rev. 2.0*
  — High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  — Direct connection to a high-speed device without an external hub
  — External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
  — Multiplexed 32-bit address and data operating at up to 133 MHz
  — Four chip selects support four external slaves
  — Up to eight-beat burst transfers
  — 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  — Three protocol engines on a per chip select basis:
    – General-purpose chip select machine (GPCM)
    – Three user-programmable machines (UPMs)
    – Dedicated single data rate SDRAM controller
  — Parity support
  — Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  — Functional and programming compatibility with the MPC8260 interrupt controller
  — Support for 8 external and 35 internal discrete interrupt sources
  — Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  — Programmable highest priority request
  — Four groups of interrupts with programmable priority
  — External and internal interrupts directed to host processor
  — Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  — Unique vector number for each interrupt source
- Dual industry-standard I^2C interfaces
  — Two-wire interface
  — Multiple master support
  — Master or slave I^2C mode support
  — On-chip digital filtering rejects spikes on the bus
  — System initialization data optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  — Four independent virtual channels
  — Concurrent execution across multiple channels with programmable bandwidth control
  — All channels accessible to local core and remote PCI masters
  — Misaligned transfer capability

  - Data chaining and direct mode
  - Interrupt on completed segment and chain
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
  - 52 parallel I/O pins multiplexed on various chip interfaces
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
Input hold time for POR configuration signals with respect to negation of $\overline{HRESET}$	0	—	ns	
Time for the MPC8347E to turn off POR configuration signals with respect to the assertion of $\overline{HRESET}$	—	4	ns	3
Time for the MPC8347E to turn on POR configuration signals with respect to the negation of $\overline{HRESET}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*.
3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 lists the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

Table 13. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	
AC input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz	t_{DISKEW}	—	 750 1125	ps	1

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 <= n <= 7) or ECC (MECC[{0...7}] if n = 8).

Figure 4 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

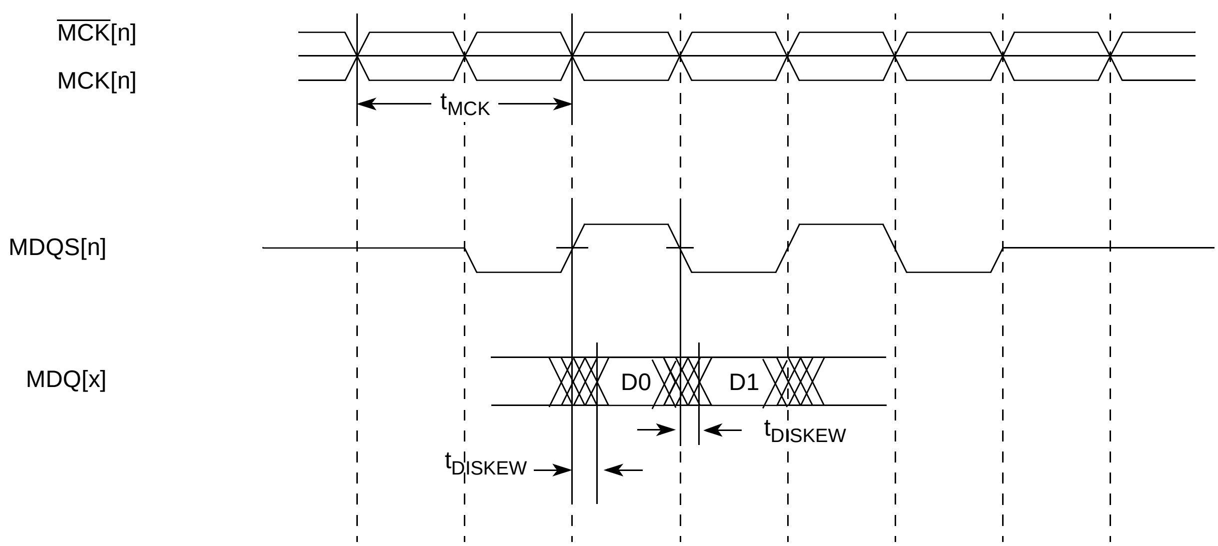

Figure 4. DDR Input Timing Diagram

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

Figure 9 shows the GMII receive AC timing diagram.

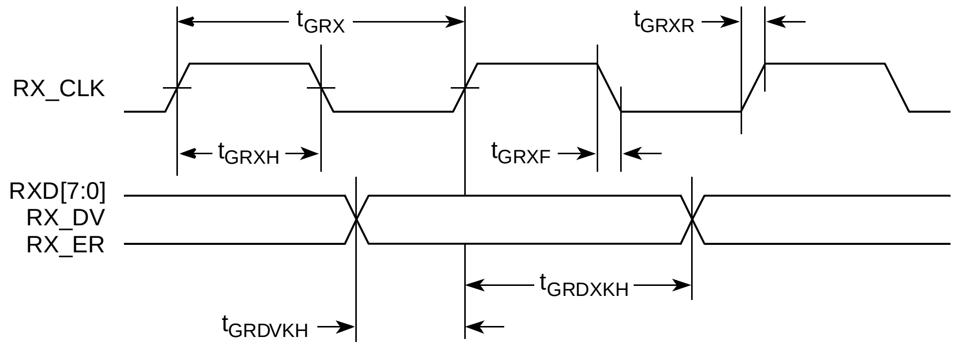

Figure 9. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Table 34. Local Bus General Timing Parameters—DLL On (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Table 35. Local Bus General Timing Parameters—DLL Bypass[9]

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7

Table 35. Local Bus General Timing Parameters—DLL Bypass[9] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output valid	t_{LBKLOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.the
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals to the load on the LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 19 provides the AC test load for the local bus.

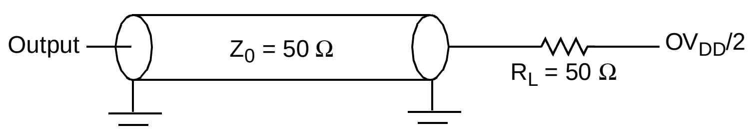

Figure 19. Local Bus C Test Load

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E

11.1 JTAG DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E.

Table 36. JTAG interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		OV_{DD} – 0.3	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E. Table 37 provides the JTAG AC timing specifications as defined in Figure 27 through Figure 30.

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data	t_{JTDVKH}	4	—		4
TMS, TDI	t_{JTIVKH}	4	—		
Input hold times:				ns	
Boundary-scan data	t_{JTDXKH}	10	—		4
TMS, TDI	t_{JTIXKH}	10	—		
Valid times:				ns	
Boundary-scan data	t_{JTKLDV}	2	11		5
TDO	t_{JTKLOV}	2	11		

12 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface of the MPC8347E.

12.1 I^2C DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the I^2C interface of the MPC8347E.

Table 38. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8349E Integrated Host Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I^2C AC Electrical Specifications

Table 39 provides the AC timing parameters for the I^2C interface of the MPC8347E. Note that all values refer to V_{IH}(min) and V_{IL}(max) levels (see Table 38).

Table 39. I^2C AC Electrical Specifications

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	μs

Figure 34 shows the PCI input AC timing diagram.

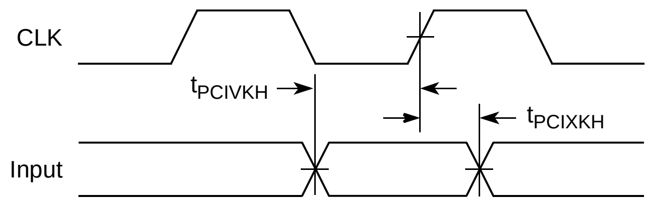

Figure 34. PCI Input AC Timing Diagram

Figure 35 shows the PCI output AC timing diagram.

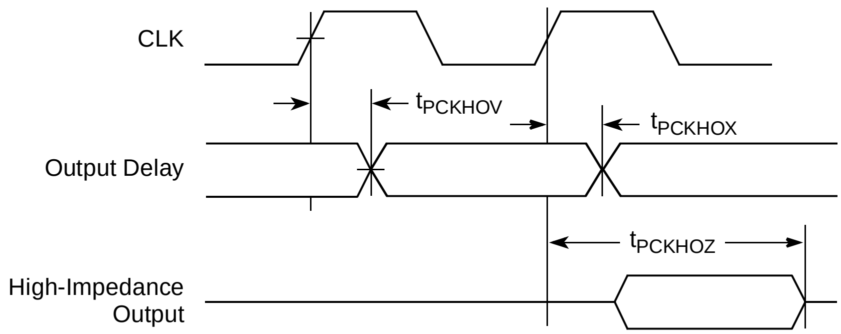

Figure 35. PCI Output AC Timing Diagram

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	O	OV_{DD}	
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV_{DD}	
$\overline{\text{UART\_CTS}}$[1]/MSRCID4/LSRCID4	AP30	I/O	OV_{DD}	
$\overline{\text{UART\_CTS}}$[2]/MDVAL/ LDVAL	AN30	I/O	OV_{DD}	
$\overline{\text{UART\_RTS}}$[1:2]	AP31, AM30	O	OV_{DD}	
I^2C interface				
IIC1_SDA	AK29	I/O	OV_{DD}	2
IIC1_SCL	AP32	I/O	OV_{DD}	2
IIC2_SDA	AN31	I/O	OV_{DD}	2
IIC2_SCL	AM31	I/O	OV_{DD}	2
SPI				
SPIMOSI	AN32	I/O	OV_{DD}	
SPIMISO	AP33	I/O	OV_{DD}	
SPICLK	AK30	I/O	OV_{DD}	
SPISEL	AL31	I	OV_{DD}	
Clocks				
PCI_CLK_OUT[0:4]	AN9, AP9, AM10, AN10, AJ11	O	OV_{DD}	
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV_{DD}	
PCI_SYNC_OUT	AP11	O	OV_{DD}	3
RTC/PIT_CLOCK	AM32	I	OV_{DD}	
CLKIN	AM9	I	OV_{DD}	
JTAG				
TCK	E20	I	OV_{DD}	
TDI	F20	I	OV_{DD}	4
TDO	B20	O	OV_{DD}	3
TMS	A20	I	OV_{DD}	4
$\overline{\text{TRST}}$	B19	I	OV_{DD}	4
Test				
TEST	D22	I	OV_{DD}	6
TEST_SEL	AL13	I	OV_{DD}	7
PMC				
$\overline{\text{QUIESCE}}$	A18	O	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SPIMISO	C7	I/O	OV_{DD}	
SPICLK	B7	I/O	OV_{DD}	
SPISEL	A7	I	OV_{DD}	
Clocks				
PCI_CLK_OUT[0:2]	Y1, W3, W2	O	OV_{DD}	
PCI_CLK_OUT[3]/$\overline{\text{LCS}}$[6]	W1	O	OV_{DD}	
PCI_CLK_OUT[4]/$\overline{\text{LCS}}$[7]	V3	O	OV_{DD}	
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV_{DD}	
PCI_SYNC_OUT	U5	O	OV_{DD}	3
RTC/PIT_CLOCK	E9	I	OV_{DD}	
CLKIN	W5	I	OV_{DD}	
JTAG				
TCK	H27	I	OV_{DD}	
TDI	H28	I	OV_{DD}	4
TDO	M24	O	OV_{DD}	3
TMS	J27	I	OV_{DD}	4
$\overline{\text{TRST}}$	K26	I	OV_{DD}	4
Test				
TEST	F28	I	OV_{DD}	6
TEST_SEL	T3	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	K27	O	OV_{DD}	
System Control				
$\overline{\text{PORESET}}$	K28	I	OV_{DD}	
$\overline{\text{HRESET}}$	M25	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	L27	I/O	OV_{DD}	2
Thermal Management				
THERM0	B15	I	—	8
Power and Ground Signals				
$AV_{DD}1$	C15	Power for e300 PLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	U1	Power for system PLL (1.2 V)	$AV_{DD}2$	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$AV_{DD}3$	AF9	Power for DDR DLL (1.2 V)	$AV_{DD}3$	
$AV_{DD}4$	U2	Power for LBIU DLL (1.2 V)	$AV_{DD}4$	
GND	A2, B1, B2, D10, D18, E6, E14, E22, F9, F12, F15, F18, F21, F24, G5, H6, J23, L4, L6, L12, L13, L14, L15, L16, L17, M11, M12, M13, M14, M15, M16, M17, M18, M23, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, P24, R5, R11, R12, R13, R14, R15, R16, R17, R18, R23, T11, T12, T13, T14, T15, T16, T17, T18, U6, U11, U12, U13, U14, U15, U16, U17, U18, V12, V13, V14, V15, V16, V17, V23, V25, W4, Y6, AA23, AB24, AC5, AC8, AC11, AC14, AC17, AC20, AD9, AD15, AD21, AE12, AE18, AF3, AF26	—	—	
GV_{DD}	U9, V9, W10, W19, Y11, Y12, Y14, Y15, Y17, Y18, AA6, AB5, AC9, AC12, AC15, AC18, AC21, AC24, AD6, AD8, AD14, AD20, AE5, AE11, AE17, AG2, AG27	Power for DDR DRAM I/O voltage (2.5 V)	GV_{DD}	
$LV_{DD}1$	U20, W25	Power for three-speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	$LV_{DD}1$	
$LV_{DD}2$	V20, Y23	Power for three-speed Ethernet #2 I/O (2.5 V, 3.3 V)	$LV_{DD}2$	
V_{DD}	J11, J12, J15, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L10, L11, L18, L19, M10, M19, N10, N19, P9, P10, P19, R10, R19, R20, T10, T19, U10, U19, V10, V11, V18, V19, W11, W12, W13, W14, W15, W16, W17, W18	Power for core (1.2 V)	V_{DD}	
OV_{DD}	B27, D3, D11, D19, E15, E23, F5, F8, F11, F14, F17, F20, G24, H23, H24, J6, J14, J17, J18, K4, L9, L20, L23, L25, M6, M9, M20, P5, P20, P23, R6, R9, R24, U23, V4, V6	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	

Table 54 provides the operating frequencies for the MPC8347E TBGA under recommended operating conditions (see Table 2).

Table 54. Operating Frequencies for TBGA

Characteristic[1]	400 MHz	533 MHz	667 MHz	Unit
e300 core frequency (*core_clk*)	266–400	266–533	266–667	MHz
Coherent system bus frequency (*csb_clk*)	100–266	100–266	100–333	MHz
DDR and memory bus frequency (MCLK)[2]	100–133	100–133	100–166.67	MHz
Local bus frequency (LCLK*n*)[3]	16.67–133	16.67–133	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66	25–66	25–66	MHz
Security core maximum internal operating frequency	133	133	166	MHz
USB_DR, USB_MPH maximum internal operating frequency	133	133	166	MHz

[1] The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

[2] The DDR data rate is 2x the DDR memory bus frequency.

[3] The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

Table 55 provides the operating frequencies for the MPC8347E PBGA under recommended operating conditions.

Table 55. Operating Frequencies for PBGA

Characteristic[1]	266 MHz	333 MHz	400 MHz	Unit
e300 core frequency (*core_clk*)	200–266	200–333	200–400	MHz
Coherent system bus frequency (*csb_clk*)		100–266		MHz
Local bus frequency (LCLK*n*)[2]		16.67–133		MHz
PCI input frequency (CLKIN or PCI_CLK)		25–66		MHz
Security core maximum internal operating frequency		133		MHz
USB_DR, USB_MPH maximum internal operating frequency		133		MHz

[1] The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

[2] The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

Table 62. Package Thermal Characteristics for PBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{\theta JC}$	5	°C/W	5
Junction-to-package natural convection on top	ψ_{JT}	5	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 63 and Table 64 show heat sink thermal resistance for TBGA and PBGA of the MPC8347E.

Table 63. Heat Sink and Thermal Resistance of MPC8347E (TBGA)

Heat Sink Assuming Thermal Grease	Air Flow	35 × 35 mm TBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	10
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.5
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.6
AAVID 31 × 35 × 23 mm pin fin	Natural convection	8.4
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.7
AAVID 31 × 35 × 23 mm pin fin	2 m/s	4
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	5.7
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.5
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	6.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	4.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.8
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	3.1

Table 64. Heat Sink and Thermal Resistance of MPC8347E (PBGA)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	13.5
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	9.6

Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally

THIS PAGE INTENTIONALLY LEFT BLANK