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8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to the gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.3](#), “Ethernet Management Interface Electrical Characteristics.”

8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 19](#) and [Table 20](#). The RGMII and RTBI signals in [Table 20](#) are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 19. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}^2	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.40	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	40	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-600	—	μA

Notes:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).
2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Figure 12 shows the MII receive AC timing diagram.

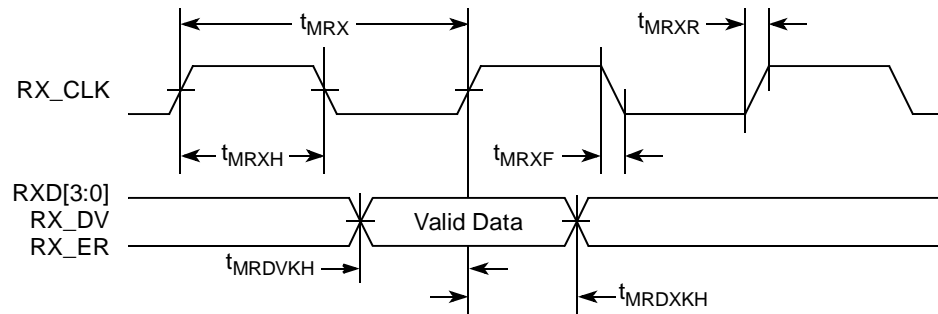


Figure 12. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 25 provides the TBI transmit AC timing specifications.

Table 25. TBI Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t_{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise, $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time, $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{TTXF}	—	—	1.0	ns
GTX_CLK125 reference clock period	t_{G125}^2	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	45	—	55	ns

Notes:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
Output hold times:				ns	
Boundary-scan data	t_{JTKLDX}	2	—		5
TDO	t_{JTKLOX}	2	—		
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 26). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design and characterization.

Figure 26 provides the AC test load for TDO and the boundary-scan outputs of the MPC8347E.

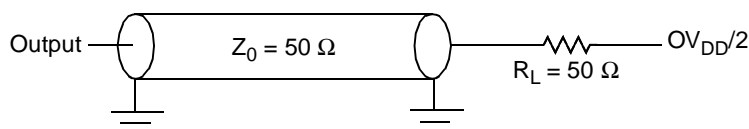
**Figure 26. AC Test Load for the JTAG Interface**

Figure 27 provides the JTAG clock input timing diagram.

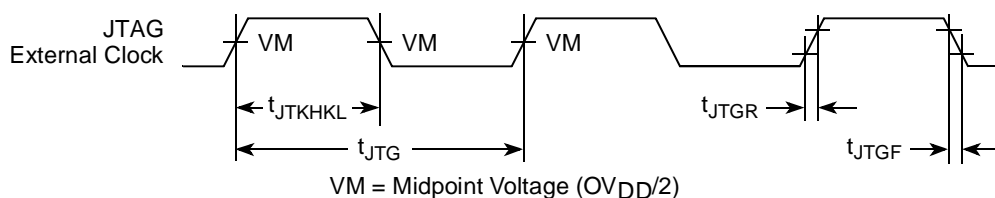
**Figure 27. JTAG Clock Input Timing Diagram**

Table 39. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

- The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8347E provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.
- The MPC8347E does not follow the "I²C-BUS Specifications" version 2.1 regarding the t_{I2CF} AC parameter.

Figure 31 provides the AC test load for the I²C.

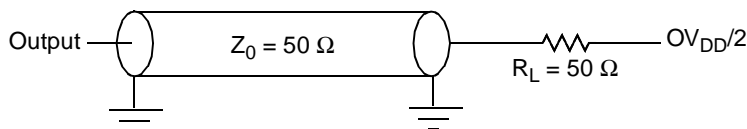
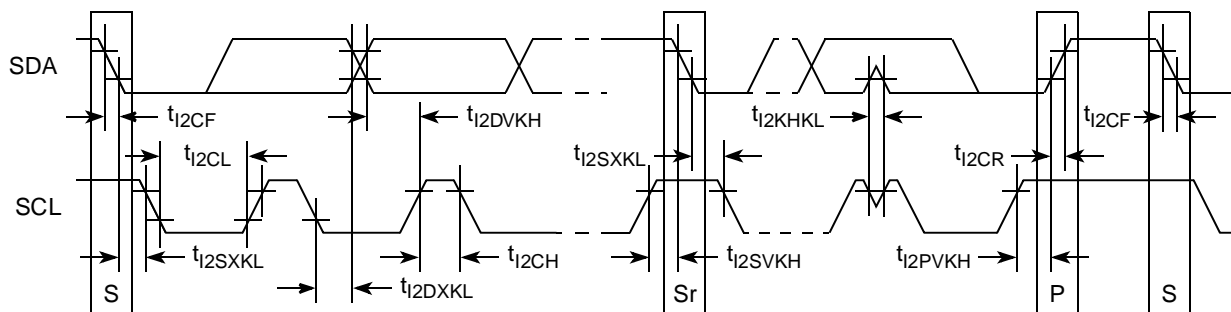
Figure 31. I²C AC Test Load

Figure 32 shows the AC timing diagram for the I²C bus.

Figure 32. I²C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8347E.

13.1 PCI DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the PCI interface of the MPC8347E.

Table 40. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}	$V_{IN}^1 = 0 \text{ V or } V_{IN} = OV_{DD}$	—	± 5	μA
High-level output voltage	V_{OH}	$OV_{DD} = \text{min, } I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min, } I_{OL} = 100 \mu\text{A}$	—	0.2	V

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8347E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8347E is configured as a host or agent device. Table 41 provides the PCI AC timing specifications at 66 MHz.

Table 41. PCI AC Timing Specifications at 66 MHz¹

Parameter	Symbol ²	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	3
Output hold from clock	t_{PCKHOX}	1	—	ns	3
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t_{PCIVKH}	3.0	—	ns	3, 5

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the MPC8347E timer pins, including $\overline{\text{TIN}}$, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK .

Table 43. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}			± 5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

14.2 Timer AC Timing Specifications

Table 44 provides the timer input and output AC timing specifications.

Table 44. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t_{TWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TWID} ns to ensure proper operation.

Figure 36 provides the AC test load for the SPI.

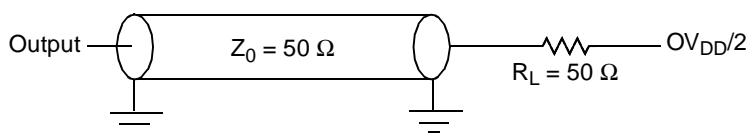
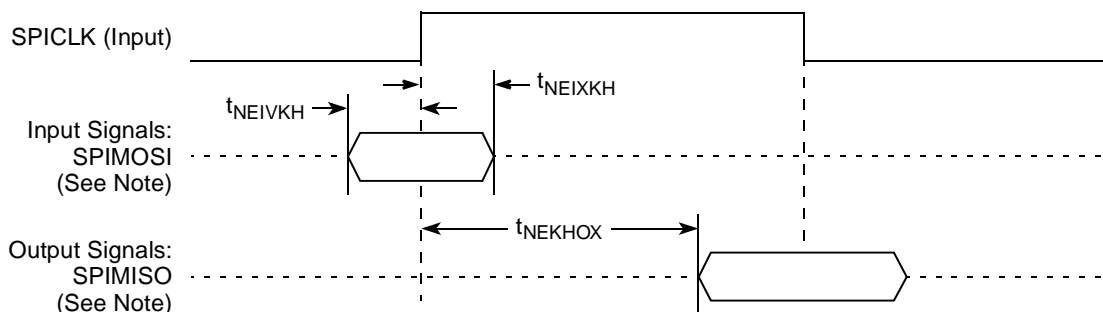


Figure 36. SPI AC Test Load

Figure 37 and Figure 38 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

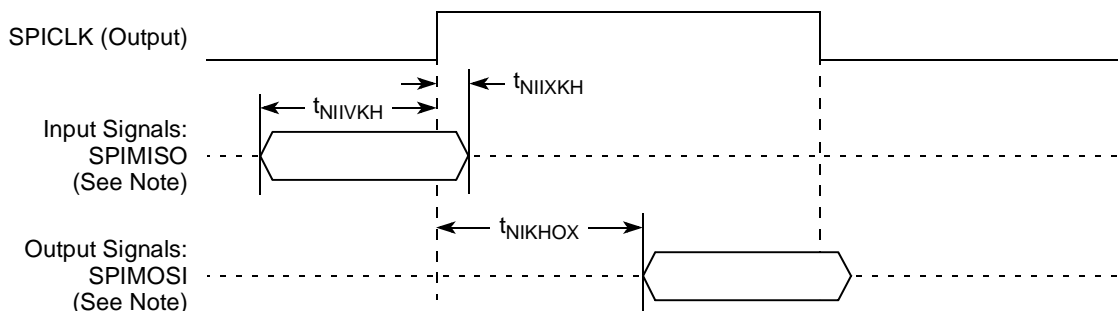
Figure 37 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 37. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 38 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 38. SPI AC Timing in Master Mode (Internal Clock) Diagram

18.3 Package Parameters for the MPC8347E PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.60 mm

18.5 Pinout Listings

Table 51 provides the pinout listing for the MPC8347E, 672 TBGA package.

Table 51. MPC8347E (TBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_INTA/IRQ_OUT	B34	O	OV _{DD}	2
PCI_RESET_OUT	C33	O	OV _{DD}	
PCI_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV _{DD}	
PCI_C/BE[3:0]	J30, M31, P33, T34	I/O	OV _{DD}	
PCI_PAR	P32	I/O	OV _{DD}	
PCI_FRAME	M32	I/O	OV _{DD}	5
PCI_TRDY	N29	I/O	OV _{DD}	5
PCI_IRDY	M34	I/O	OV _{DD}	5
PCI_STOP	N31	I/O	OV _{DD}	5
PCI_DEVSEL	N30	I/O	OV _{DD}	5
PCI_IDSEL	J31	I	OV _{DD}	
PCI_SERR	N34	I/O	OV _{DD}	5
PCI_PERR	N33	I/O	OV _{DD}	5
PCI_REQ[0]	D32	I/O	OV _{DD}	
PCI_REQ[1]/CPCI1_HS_ES	D34	I	OV _{DD}	
PCI_REQ[2:4]	E34, F32, G29	I	OV _{DD}	
PCI_GNT0	C34	I/O	OV _{DD}	
PCI_GNT1/CPCI1_HS_LED	D33	O	OV _{DD}	
PCI_GNT2/CPCI1_HS_ENUM	E33	O	OV _{DD}	
PCI_GNT[3:4]	F31, F33	O	OV _{DD}	
M66EN	A19	I	OV _{DD}	
DDR SDRAM Memory Interface				
MDQ[0:63]	D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8	I/O	GV _{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV _{DD}	
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV _{DD}	
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	O	OV _{DD}	
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	E27	I	OV _{DD}	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A29	O	OV _{DD}	
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	D28	O	OV _{DD}	
MPH1_CLK/DR_CLK	B29	I	OV _{DD}	
USB Port 0				
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	C29	I/O	OV _{DD}	
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	A30	I/O	OV _{DD}	
MPH0_D2_VMO_SE0/DR_D10_DPPD	E28	I/O	OV _{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	B30	I/O	OV _{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	C30	I/O	OV _{DD}	
MPH0_D5_DM/DR_D13_SESS_END	A31	I/O	OV _{DD}	
MPH0_D6_SER_RCV/DR_D14	B31	I/O	OV _{DD}	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	C31	I/O	OV _{DD}	
MPH0_NXT/DR_RX_ACTIVE_ID	B32	I	OV _{DD}	
MPH0_DIR_DPPULLUP/DR_RESET	A32	I/O	OV _{DD}	
MPH0_STP_SUSPEND/DR_TX_READY	A33	I/O	OV _{DD}	
MPH0_PWRFAULT/DR_RX_VALIDH	C32	I	OV _{DD}	
MPH0_PCTL0/DR_LINE_STATE0	D31	I/O	OV _{DD}	
MPH0_PCTL1/DR_LINE_STATE1	E30	I/O	OV _{DD}	
MPH0_CLK/DR_RX_VALID	B33	I	OV _{DD}	
Programmable Interrupt Controller				
MCP_OUT	AN33	O	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	C19	I/O	OV _{DD}	
IRQ[1:5]/GPIO2[13:17]	C22, A22, D21, C21, B21	I/O	OV _{DD}	
IRQ[6]/GPIO2[18]/CKSTOP_OUT	A21	I/O	OV _{DD}	
IRQ[7]/GPIO2[19]/CKSTOP_IN	C20	I/O	OV _{DD}	
Ethernet Management Interface				
EC_MDC	A7	O	LV _{DD1}	
EC_MDIO	E9	I/O	LV _{DD1}	2

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV _{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV _{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV _{DD}	
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV _{DD}	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV _{DD}	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV _{DD}	
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV _{DD}	
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV _{DD}	
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV _{DD}	
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV _{DD}	
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV _{DD}	
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV _{DD}	
MPH0_CLK/DR_RX_VALID	C21	I	OV _{DD}	
Programmable Interrupt Controller				
MCP_OUT	E8	O	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	J28	I/O	OV _{DD}	
IRQ[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV _{DD}	
IRQ[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV _{DD}	
IRQ[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV _{DD}	
Ethernet Management Interface				
EC_MDC	Y24	O	LV _{DD1}	
EC_MDIO	Y25	I/O	LV _{DD1}	2
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV _{DD1}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV _{DD}	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV _{DD1}	
TSEC1_GTX_CLK	V24	O	LV _{DD1}	3
TSEC1_RX_CLK	U26	I	LV _{DD1}	
TSEC1_RX_DV	U24	I	LV _{DD1}	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV _{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV _{DD}	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV _{DD1}	
TSEC1_TX_CLK	N25	I	OV _{DD}	

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. [Table 56](#) shows the multiplication factor encodings for the system PLL.

Table 56. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

As described in [Section 19, “Clocking,”](#) the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). [Table 57](#) and [Table 58](#) show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 62. Package Thermal Characteristics for PBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{\theta JC}$	5	°C/W	5
Junction-to-package natural convection on top	Ψ_{JT}	5	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For

many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Table 64. Heat Sink and Thermal Resistance of MPC8347E (PBGA) (continued)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	8.8
AAVID 31 × 35 × 23 mm pin fin	Natural convection	11.3
AAVID 31 × 35 × 23 mm pin fin	1 m/s	8.1
AAVID 31 × 35 × 23 mm pin fin	2 m/s	7.5
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	9.1
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	7.1
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	6.5
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	10.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	7.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	6.6
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	6.9

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770

Table 66. Document Revision History (continued)

Revision	Date	Substantive Change(s)
8	2/2007	<p>Page 1, updated first paragraph to reflect PowerQUICC II information. Updated note after second paragraph.</p> <p>In the features list in Section 1, "Overview," corrected DDR data rate to show:</p> <ul style="list-style-type: none"> • 266 MHz for PBGA parts for all silicon revisions • 333 MHz for DDR for TBGA parts for silicon Rev. 1.x <p>In Table 5, "MPC8347E Typical I/O Power Dissipation," added GV_{DD} 1.8-V values for DDR2; added table footnote to designate rates that apply only to the TBGA package.</p> <p>In Figure 43, "JTAG Interface Connection," updated with new figure.</p> <p>In Section 23, "Ordering Information," replicated note from document introduction.</p> <p>In Section 23.1, "Part Numbers Fully Addressed by This Document," replaced third sentence of first paragraph directing customer to product summary page for available frequency configuration parts. Updated back page information.</p>
7	8/2006	<p>Changed all references to revision 2.0 silicon to revision 3.0 silicon.</p> <p>Changed V_{IH} minimum value in Table 36, "JTAG Interface DC Electrical Characteristics," to $OV_{DD} - 0.3$.</p> <p>In Table 60, "Suggested PLL Configurations," deleted reference-number rows 902 and 703.</p>
6	3/2006	<p>Section 2, "Electrical Characteristics," moved to second section and all other section, table, and figure numbering change accordingly.</p> <p>Table 7, "CLKIN AC Timing Specifications:" Changed max rise and fall time from 1.2 to 2.3.</p> <p>Table 22, "GMII Receive AC Timing Specifications:" Changed min t_{TTKHDX} from 0.5 to 1.0.</p> <p>Table 30, "MII Management AC Timing Specifications:" Changed max value of t_{MDKHDX} from 70 to 170.</p> <p>Table 34, "Local Bus General Timing Parameters—DLL on:" Changed min $t_{LBIVKH2}$ from 1.7 to 2.2.</p> <p>Table 36, "JTAG interface DC Electrical Characteristics:" Changed V_{IH} input high voltage min to 2.0.</p> <p>Table 54, "Operating Frequencies for TBGA:"</p> <ul style="list-style-type: none"> • Updated TBD values. • Changed maximum coherent system bus frequency for TBGA 667-MHz device to 333 MHz. <p>Table 55, "Operating Frequencies for PBGA:"</p> <ul style="list-style-type: none"> • Updated TBD values. • Changed PBGA maximum coherent system bus frequency to 266 MHz, and maximum DDR memory bus frequency to 133 MHz. <p>Table 60, "Suggested PLL Configurations": Removed some values from suggested PLL configurations for reference numbers 902, 922, 903, and 923.</p> <p>Table 67, "Part Numbering Nomenclature": Updated TBD values in note 1.</p> <p>Added Table 68, "SVR Settings."</p> <p>Added Section 23.2, "Part Marking."</p>
5	10/2005	In Table 57, updated AAVID 30x30x9.4 mm Pin Fin (natural convection) junction-to-ambient thermal resistance, from 11 to 10.
4	9/2005	Added Table 2, "MPC8347E Typical I/O Power Dissipation."
3	8/2005	Table 1: Updated values for power dissipation that were TBD in Revision 2.
2	5/2005	<p>Table 1: Typical values for power dissipation are changed to TBD.</p> <p>Table 48: Footnote numbering was wrong. THERM0 should have footnote 9 instead of 8.</p>

Table 66. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1	4/2005	Table 1: Addition of note 1 Table 48: Addition of Therm0 (K32) Table 49: Addition of Therm0 (B15)
0	4/2005	Initial release.

23 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

NOTE

The information in this document is accurate for revision 1.1 silicon and earlier. For information on revision 3.0 silicon and later versions (orderable part numbers ending with A or B), see the *MPC8347EA PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8347EAEC).

23.1 Part Numbers Fully Addressed by This Document

Table 67 shows an analysis of the Freescale part numbering nomenclature for the MPC8347E. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration parts including extended temperatures, refer to the MPC8347E product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 67. Part Numbering Nomenclature

MPC	nnnn	e	t	pp	aa	a	r
Product Code	Part Identifier	Encryption Acceleration	Temperature ¹ Range	Package ²	Processor Frequency ³	Platform Frequency	Revision Level
MPC	8347	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	ZU = TBGA VV = PB free TBGA ZQ = PBGA VR = PB Free PBGA	e300 core speed AD = 266 AG = 400 AJ = 533 AL = 667	D = 266 F = 333 ⁴	Blank = 1.1 or 1.0

Notes:

1. For temperature range = C, processor frequency is limited to 400 (PBGA) with a platform frequency of 266 and up to 667(TBGA)with a platform frequency of 333
2. See [Section 18, "Package and Pin Listings,"](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. ALF marked parts support DDR1 up to 333 MHz (at 333 MHz CSB as the 'F' marking implies) and DDR2 up to 400 MHz (at 200 MHz CSB). AJF marked parts support DDR1 and DDR2 up to 333 MHz (at a CSB of 333 MHz), but DDR2 at 400 MHz (CSB at 200 MHz) is NOT guaranteed.

Table 68 shows the SVR settings by device and package type.

Table 68. SVR Settings

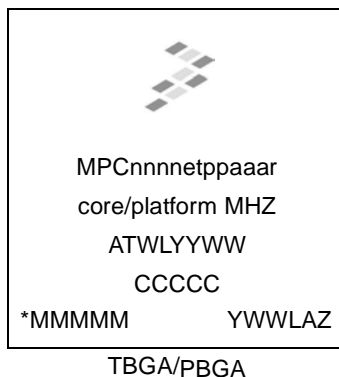
Device	Package	SVR (Rev. 1.0)
MPC8347E	TBGA	8052_0010
MPC8347	TBGA	8053_0010

Table 68. SVR Settings (continued)

MPC8347E	PBGA	8054_0010
MPC8347	PBGA	8055_0010

23.2 Part Marking

Parts are marked as in the example shown in [Figure 44](#).



Notes:

ATWLYYWW is the traceability code.

CCCCC is the country code.

MMMMM is the mask number.

YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA or PBGA Devices

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