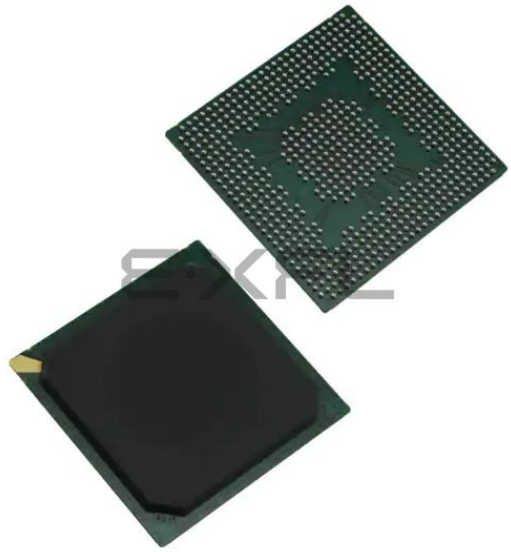

**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 266MHz |
| Co-Processors/DSP | Security; SEC |
| RAM Controllers | DDR |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 620-BBGA Exposed Pad |
| Supplier Device Package | 620-HBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347ezqadd |

  - Programmable field size up to 2048 bits
  - Elliptic curve cryptography
  - F2m and F(p) modes
  - Programmable field size up to 511 bits
- Data encryption standard (DES) execution unit (DEU)
  - DES and 3DES algorithms
  - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
  - ECB and CBC modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rijndael symmetric-key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, and counter (CTR) modes
- ARC four execution unit (AFEU)
  - Stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
  - Static and/or dynamic assignment of crypto-execution units through an integrated controller
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

- Universal serial bus (USB) dual role controller
  - USB on-the-go mode with both device and host functionality
  - Complies with USB specification Rev. 2.0
  - Can operate as a stand-alone USB device
    - One upstream facing port
    - Six programmable USB endpoints
  - Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
  - Can operate as a stand-alone USB host controller
    - USB root hub with one or two downstream-facing ports

  - Enhanced host controller interface (EHCI) compatible
  - Complies with *USB Specification Rev. 2.0*
- High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Direct connection to a high-speed device without an external hub
- External PHY with serial and low-pin count (ULPI) interfaces

- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Four chip selects support four external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
  - Unique vector number for each interrupt source
- Dual industry-standard $I^2C$ interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from $I^2C$-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible to local core and remote PCI masters
  - Misaligned transfer capability

Table 5 shows the estimated typical I/O power dissipation for MPC8347E.

**Table 5. MPC8347E Typical I/O Power Dissipation**

| Interface | Parameter | DDR2 $GV_{DD}$ (1.8 V) | DDR1 $GV_{DD}$ (2.5 V) | $OV_{DD}$ (3.3 V) | $LV_{DD}$ (3.3 V) | $LV_{DD}$ (2.5 V) | Unit | Comments |
|---|---|---|---|---|---|---|---|---|
| DDR I/O<br>65% utilization<br>2.5 V<br>Rs = 20 Ω<br>Rt = 50 Ω<br>2 pair of clocks | 200 MHz, 32 bits | — | 0.42 | — | — | — | W | — |
| | 200 MHz, 64 bits | — | 0.55 | — | — | — | W | — |
| | 266 MHz, 32 bits | — | 0.5 | — | — | — | W | — |
| | 266 MHz, 64 bits | — | 0.66 | — | — | — | W | — |
| | 300 MHz,[1] 32 bits | — | 0.54 | — | — | — | W | — |
| | 300 MHz,[1] 64 bits | — | 0.7 | — | — | — | W | — |
| | 333 MHz,[1] 32 bits | — | 0.58 | — | — | — | W | — |
| | 333 MHz,[1] 64 bits | — | 0.76 | — | — | — | W | — |
| | 400 MHz,[1] 32 bits | — | — | — | — | — | | — |
| | 400 MHz,[1] 64 bits | — | — | — | — | — | | — |
| PCI I/O<br>load = 30 pF | 33 MHz, 32 bits | — | — | 0.04 | — | — | W | — |
| | 66 MHz, 32 bits | — | — | 0.07 | — | — | W | — |
| Local bus I/O<br>load = 25 pF | 167 MHz, 32 bits | — | — | 0.34 | — | — | W | — |
| | 133 MHz, 32 bits | — | — | 0.27 | — | — | W | — |
| | 83 MHz, 32 bits | — | — | 0.17 | — | — | W | — |
| | 66 MHz, 32 bits | — | — | 0.14 | — | — | W | — |
| | 50 MHz, 32 bits | — | — | 0.11 | — | — | W | — |
| TSEC I/O<br>load = 25 pF | MII | — | — | — | 0.01 | — | W | Multiply by number of interfaces used. |
| | GMII or TBI | — | — | — | 0.06 | — | W | |
| | RGMII or RTBI | — | — | — | — | 0.04 | W | |
| USB | 12 MHz | — | — | 0.01 | — | — | W | Multiply by 2 if using 2 ports. |
| | 480 MHz | — | — | 0.2 | — | — | W | |
| Other I/O | | — | — | 0.01 | — | — | W | — |

[1] TBGA package only.

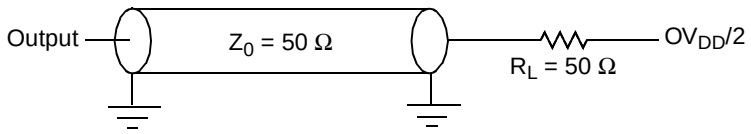


**Figure 6. DDR AC Test Load**

Table 15 shows the DDR SDRAM measurement conditions.

**Table 15. DDR SDRAM Measurement Conditions**

| Symbol | DDR | Unit | Notes |
|---|---|---|---|
| $V_{TH}$ | $MV_{REF}$ ± 0.31 V | V | 1 |
| $V_{OUT}$ | 0.5 × $GV_{DD}$ | V | 2 |

**Notes:**
1. Data input threshold measurement point.
2. Data output measurement point.

Figure 7 shows the DDR SDRAM output timing diagram for source synchronous mode.

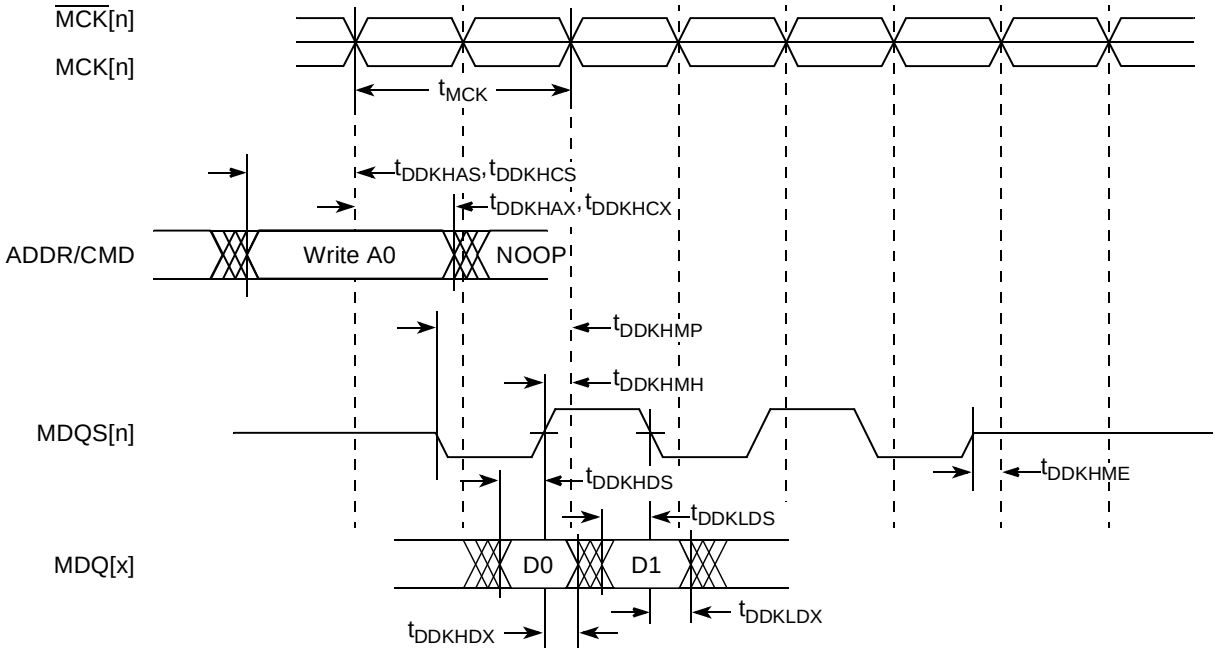


**Figure 7. DDR SDRAM Output Timing Diagram for Source Synchronous Mode**

Table 16 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings, which can be useful for a system utilizing the DLL. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

**Table 20. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics**

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}$ | — | | 2.37 | 2.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $LV_{DD}$ = Min | 2.00 | $LV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $LV_{DD}$ = Min | GND – 0.3 | 0.40 | V |
| Input high voltage | $V_{IH}$ | — | $LV_{DD}$ = Min | 1.7 | $LV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | $LV_{DD}$ = Min | –0.3 | 0.70 | V |
| Input high current | $I_{IH}$ | $V_{IN}$[1] = $LV_{DD}$ | | — | 10 | µA |
| Input low current | $I_{IL}$ | $V_{IN}$[1] = GND | | –15 | — | µA |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

## 8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

### 8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

#### 8.2.1.1 GMII Transmit AC Timing Specifications

Table 21 provides the GMII transmit AC timing specifications.

**Table 21. GMII Transmit AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{GTX}$ | — | 8.0 | — | ns |
| GTX_CLK duty cycle | $t_{GTXH}/t_{GTX}$ | 43.75 | — | 56.25 | % |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$ | 0.5 | — | 5.0 | ns |
| GTX_CLK clock rise time, $V_{IL}$(min) to $V_{IH}$(max) | $t_{GTXR}$ | — | — | 1.0 | ns |
| GTX_CLK clock fall time, $V_{IH}$(max) to $V_{IL}$(min) | $t_{GTXF}$ | — | — | 1.0 | ns |
| GTX_CLK125 clock period | $t_{G125}$[2] | — | 8.0 | — | ns |
| GTX_CLK125 reference clock duty cycle measured at $LV_{DD}/2$ | $t_{G125H}/t_{G125}$ | 45 | — | 55 | % |

**Notes:**
1. The symbols for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GTKHDV}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, $t_{GTKHDX}$ symbolizes GMII transmit timing (GT) with respect to the $t_{GTX}$ clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of $t_{GTX}$ represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol represents the external GTX_CLK125 signal and does not follow the original symbol naming convention.

# 9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8347E.

## 9.1 USB DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the USB interface.

**Table 31. USB DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

## 9.2 USB AC Electrical Specifications

Table 32 describes the general timing parameters of the USB interface of the MPC8347E.

**Table 32. USB General Timing Parameters (ULPI Mode Only)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| USB clock cycle time | $t_{USCK}$ | 15 | — | ns | 2–5 |
| Input setup to USB clock—all inputs | $t_{USIVKH}$ | 4 | — | ns | 2–5 |
| Input hold to USB clock—all inputs | $t_{USIXKH}$ | 1 | — | ns | 2–5 |
| USB clock to output valid—all outputs | $t_{USKHOV}$ | — | 7 | ns | 2–5 |
| Output hold from USB clock—all outputs | $t_{USKHOX}$ | 2 | — | ns | 2–5 |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{USIXKH}$ symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, $t_{USKHOX}$ symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

# 10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8347E.

## 10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

**Table 33. Local Bus DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

## 10.2 Local Bus AC Electrical Specification

Table 34 and Table 35 describe the general timing parameters of the local bus interface of the MPC8347E.

**Table 34. Local Bus General Timing Parameters—DLL On**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | — | ns | 2 |
| Input setup to local bus clock (except LUPWAIT) | $t_{LBIVKH1}$ | 1.5 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 2.2 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| LUPWAIT Input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |
| Local bus clock to LALE rise | $t_{LBKHLR}$ | — | 4.5 | ns | |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 4.5 | ns | |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 4.5 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 4.5 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 1 | — | ns | 3 |

Figure 20 through Figure 25 show the local bus signals.

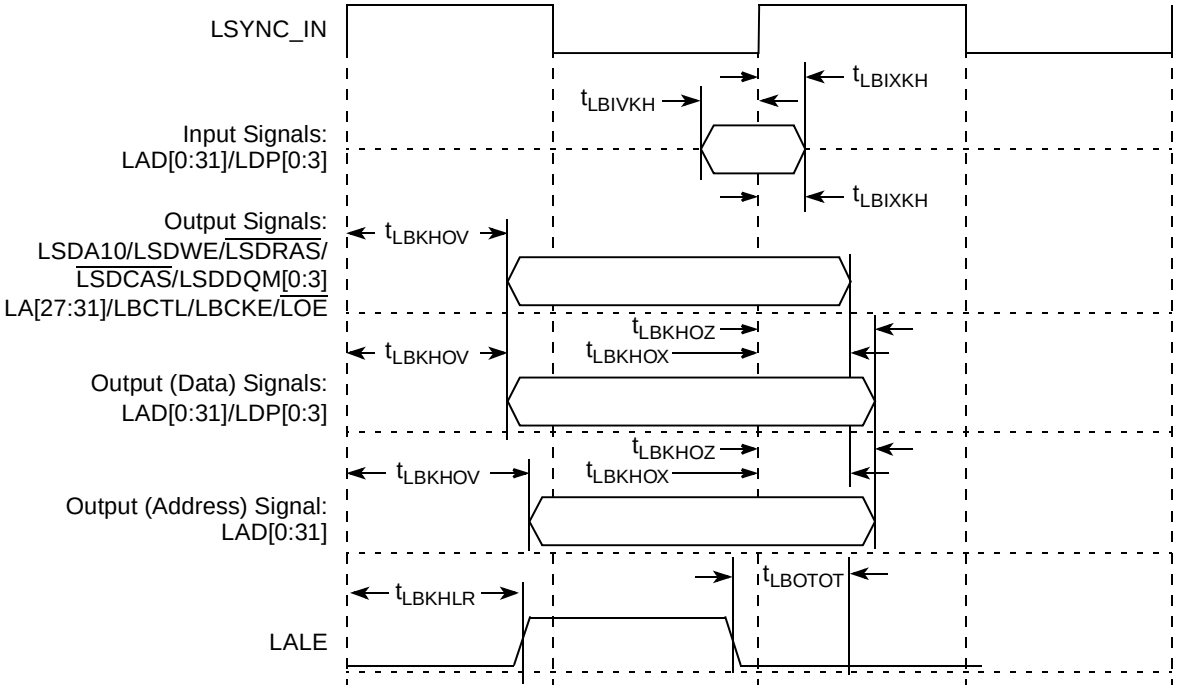


**Figure 20. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)**

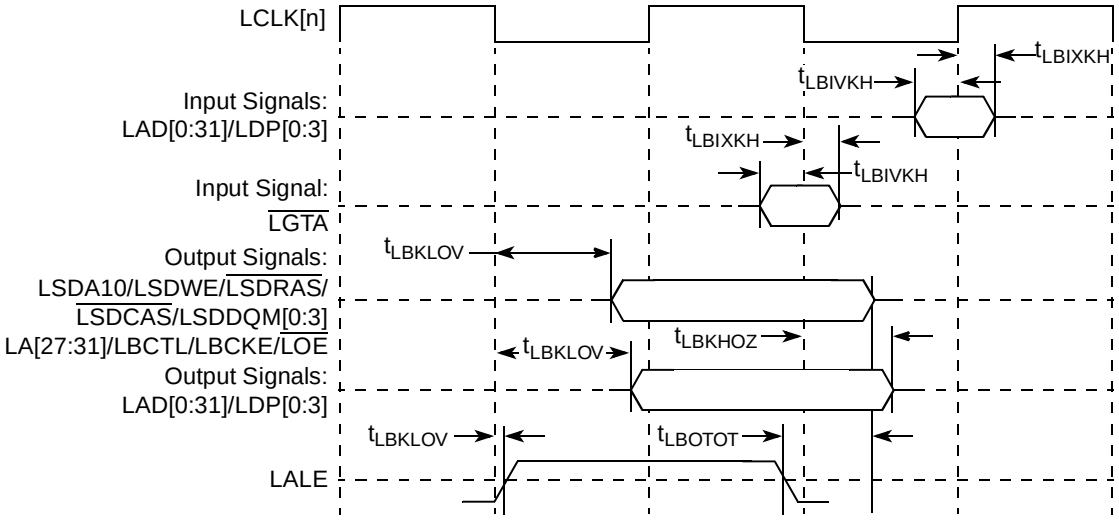


**Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)**

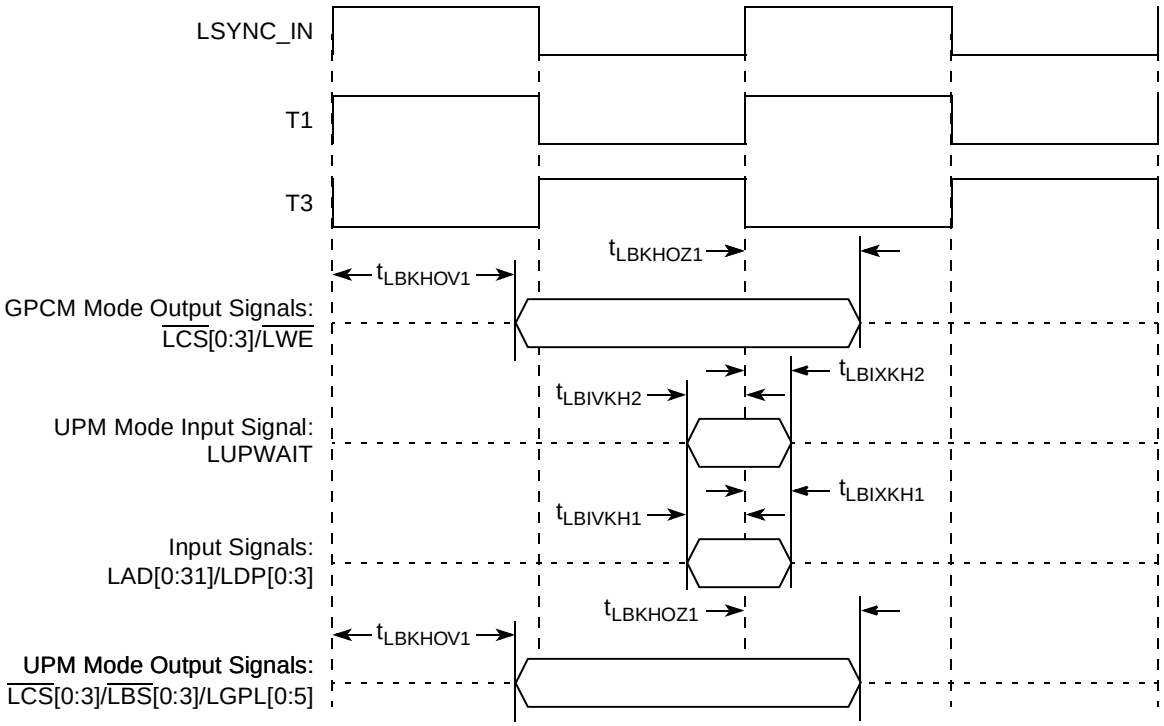


**Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)**

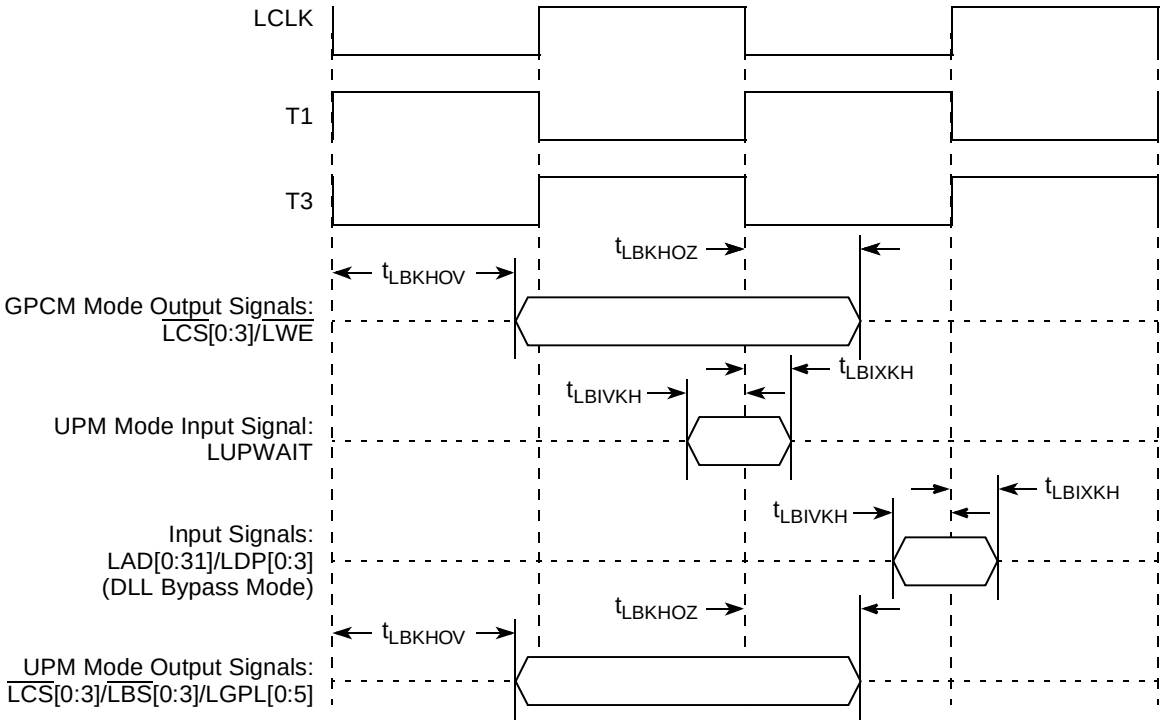


**Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)**

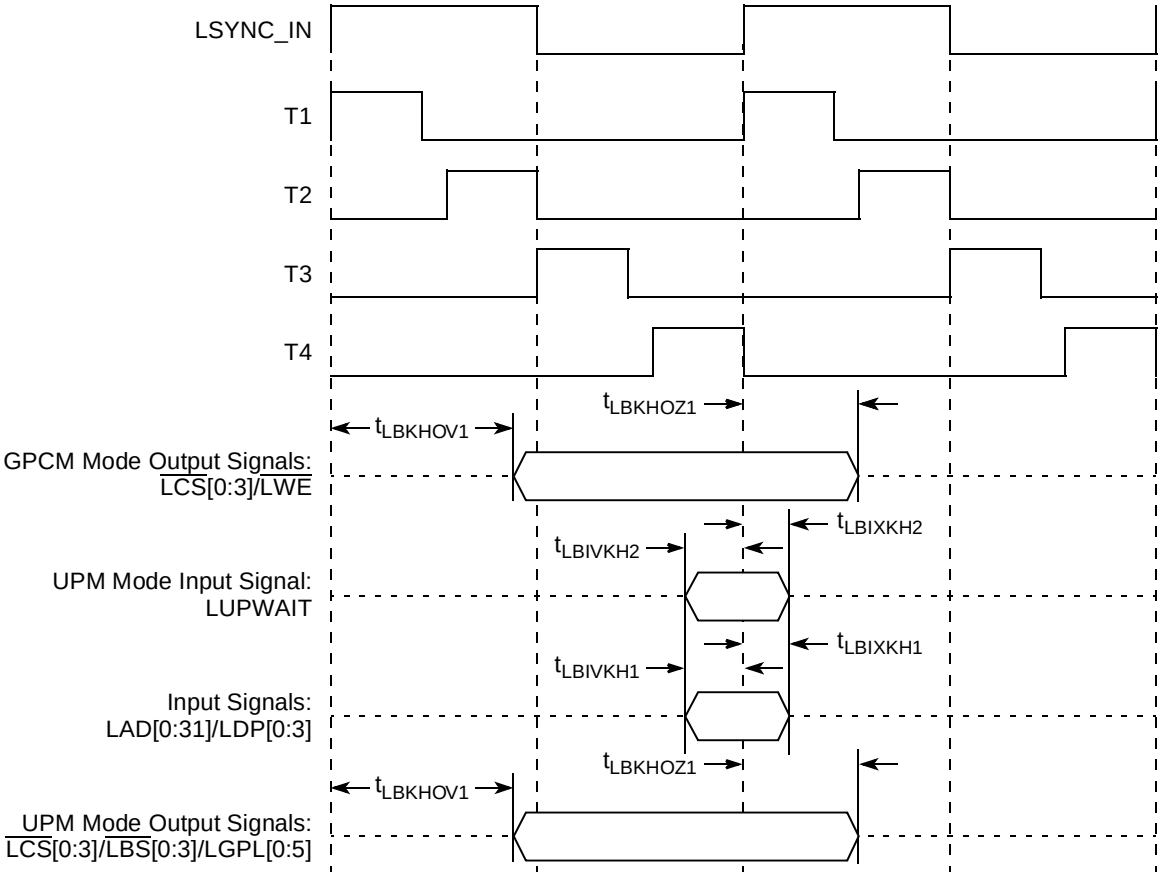


**Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)**

**Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)**

At recommended operating conditions (see Table 2).

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>2<br>2 | <br>—<br>— | ns | 5 |
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>2<br>2 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 26). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design and characterization.

Figure 26 provides the AC test load for TDO and the boundary-scan outputs of the MPC8347E.

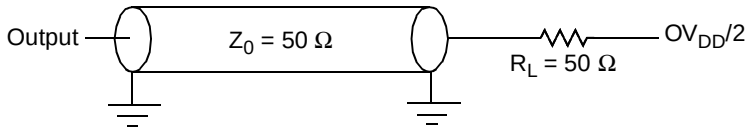


**Figure 26. AC Test Load for the JTAG Interface**

Figure 27 provides the JTAG clock input timing diagram.

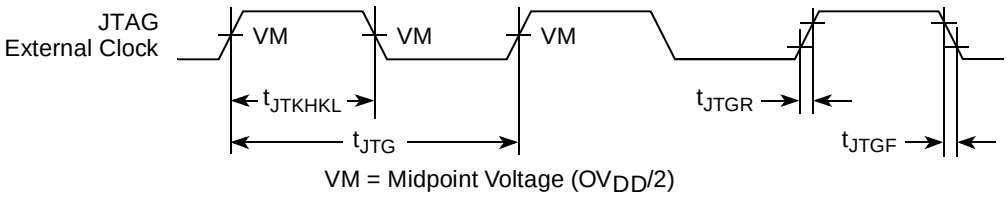


**Figure 27. JTAG Clock Input Timing Diagram**

# 13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8347E.

## 13.1 PCI DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the PCI interface of the MPC8347E.

**Table 40. PCI DC Electrical Characteristics**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{OUT} \geq V_{OH}$ (min) or | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | $V_{OUT} \leq V_{OL}$ (max) | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $V_{IN}$[1]= 0 V or $V_{IN} = OV_{DD}$ | — | ±5 | µA |
| High-level output voltage | $V_{OH}$ | $OV_{DD}$ = min, $I_{OH}$ = –100 µA | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage | $V_{OL}$ | $OV_{DD}$ = min, $I_{OL}$ = 100 µA | — | 0.2 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1.

## 13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8347E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8347E is configured as a host or agent device. Table 41 provides the PCI AC timing specifications at 66 MHz.

**Table 41. PCI AC Timing Specifications at 66 MHz[1]**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 6.0 | ns | 3 |
| Output hold from clock | $t_{PCKHOX}$ | 1 | — | ns | 3 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 3, 4 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 3, 5 |

Figure 34 shows the PCI input AC timing diagram.

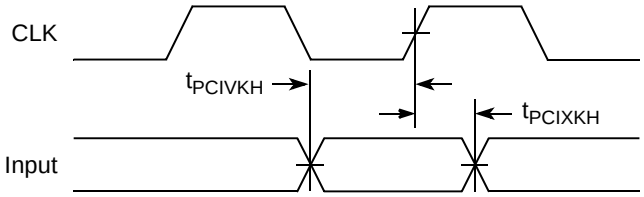


**Figure 34. PCI Input AC Timing Diagram**

Figure 35 shows the PCI output AC timing diagram.

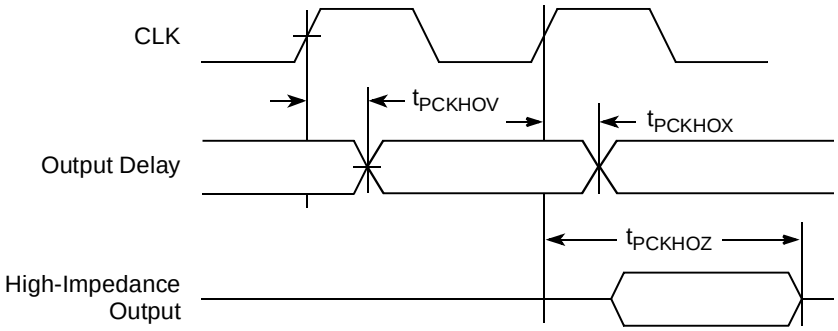


**Figure 35. PCI Output AC Timing Diagram**

**Table 57. CSB Frequency Options for Host Mode**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0010 | 2 : 1 | | | | 133 |
| Low | 0011 | 3 : 1 | | | 100 | 200 |
| Low | 0100 | 4 : 1 | | 100 | 133 | 266 |
| Low | 0101 | 5 : 1 | | 125 | 166 | 333 |
| Low | 0110 | 6 : 1 | 100 | 150 | 200 | |
| Low | 0111 | 7 : 1 | 116 | 175 | 233 | |
| Low | 1000 | 8 : 1 | 133 | 200 | 266 | |
| Low | 1001 | 9 : 1 | 150 | 225 | 300 | |
| Low | 1010 | 10 : 1 | 166 | 250 | 333 | |
| Low | 1011 | 11 : 1 | 183 | 275 | | |
| Low | 1100 | 12 : 1 | 200 | 300 | | |
| Low | 1101 | 13 : 1 | 216 | 325 | | |
| Low | 1110 | 14 : 1 | 233 | | | |
| Low | 1111 | 15 : 1 | 250 | | | |
| Low | 0000 | 16 : 1 | 266 | | | |
| High | 0010 | 2 : 1 | | | | 133 |
| High | 0011 | 3 : 1 | | | 100 | 200 |
| High | 0100 | 4 : 1 | | | 133 | 266 |
| High | 0101 | 5 : 1 | | | 166 | 333 |
| High | 0110 | 6 : 1 | | | 200 | |
| High | 0111 | 7 : 1 | | | 233 | |
| High | 1000 | 8 : 1 | | | | |

1 CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

**Table 58. CSB Frequency Options for Agent Mode**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0010 | 2 : 1 | | | | 133 |
| Low | 0011 | 3 : 1 | | | 100 | 200 |
| Low | 0100 | 4 : 1 | | 100 | 133 | 266 |
| Low | 0101 | 5 : 1 | | 125 | 166 | 333 |
| Low | 0110 | 6 : 1 | 100 | 150 | 200 | |
| Low | 0111 | 7 : 1 | 116 | 175 | 233 | |
| Low | 1000 | 8 : 1 | 133 | 200 | 266 | |
| Low | 1001 | 9 : 1 | 150 | 225 | 300 | |
| Low | 1010 | 10 : 1 | 166 | 250 | 333 | |
| Low | 1011 | 11 : 1 | 183 | 275 | | |
| Low | 1100 | 12 : 1 | 200 | 300 | | |
| Low | 1101 | 13 : 1 | 216 | 325 | | |
| Low | 1110 | 14 : 1 | 233 | | | |
| Low | 1111 | 15 : 1 | 250 | | | |
| Low | 0000 | 16 : 1 | 266 | | | |
| High | 0010 | 4 : 1 | | 100 | 133 | 266 |
| High | 0011 | 6 : 1 | 100 | 150 | 200 | |
| High | 0100 | 8 : 1 | 133 | 200 | 266 | |
| High | 0101 | 10 : 1 | 166 | 250 | 333 | |
| High | 0110 | 12 : 1 | 200 | 300 | | |
| High | 0111 | 14 : 1 | 233 | | | |
| High | 1000 | 16 : 1 | 266 | | | |

1 CFG_CLKIN_DIV doubles csb_clk if set high.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

## 19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 59 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 59 should be considered as reserved.

**NOTE**

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

**Table 59. e300 Core PLL Configuration**

| RCWL[COREPLL] | | | *core_clk* : *csb_clk* Ratio | VCO Divider[1] |
|---|---|---|---|---|
| 0–1 | 2–5 | 6 | | |
| nn | 0000 | n | PLL bypassed (PLL off, *csb_clk* clocks core directly) | PLL bypassed (PLL off, *csb_clk* clocks core directly) |
| 00 | 0001 | 0 | 1:1 | 2 |
| 01 | 0001 | 0 | 1:1 | 4 |
| 10 | 0001 | 0 | 1:1 | 8 |
| 11 | 0001 | 0 | 1:1 | 8 |
| 00 | 0001 | 1 | 1.5:1 | 2 |
| 01 | 0001 | 1 | 1.5:1 | 4 |
| 10 | 0001 | 1 | 1.5:1 | 8 |
| 11 | 0001 | 1 | 1.5:1 | 8 |
| 00 | 0010 | 0 | 2:1 | 2 |
| 01 | 0010 | 0 | 2:1 | 4 |
| 10 | 0010 | 0 | 2:1 | 8 |
| 11 | 0010 | 0 | 2:1 | 8 |
| 00 | 0010 | 1 | 2.5:1 | 2 |
| 01 | 0010 | 1 | 2.5:1 | 4 |
| 10 | 0010 | 1 | 2.5:1 | 8 |
| 11 | 0010 | 1 | 2.5:1 | 8 |
| 00 | 0011 | 0 | 3:1 | 2 |
| 01 | 0011 | 0 | 3:1 | 4 |
| 10 | 0011 | 0 | 3:1 | 8 |
| 11 | 0011 | 0 | 3:1 | 8 |

[1] Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

## 19.3 Suggested PLL Configurations

Table 60 shows suggested PLL configurations for 33 and 66 MHz input clocks.

# 20 Thermal

This section describes the thermal specifications of the MPC8347E.

## 20.1 Thermal Characteristics

Table 61 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8347E.

**Table 61. Package Thermal Characteristics for TBGA**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient natural convection on single-layer board (1s) | $R_{\theta JA}$ | 14 | °C/W | 1, 2 |
| Junction-to-ambient natural convection on four-layer board (2s2p) | $R_{\theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction-to-ambient (@ 200 ft/min) on single-layer board (1s) | $R_{\theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p) | $R_{\theta JMA}$ | 8 | °C/W | 1, 3 |
| Junction-to-ambient (@ 2 m/s) on single-layer board (1s) | $R_{\theta JMA}$ | 9 | °C/W | 1, 3 |
| Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p) | $R_{\theta JMA}$ | 7 | °C/W | 1, 3 |
| Junction-to-board thermal | $R_{\theta JB}$ | 3.8 | °C/W | 4 |
| Junction-to-case thermal | $R_{\theta JC}$ | 1.7 | °C/W | 5 |
| Junction-to-package natural convection on top | $\Psi_{JT}$ | 1 | °C/W | 6 |

**Notes:**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 62 provides the package thermal characteristics for the 620 29 × 29 mm PBGA of the MPC8347E.

**Table 62. Package Thermal Characteristics for PBGA**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient natural convection on single-layer board (1s) | $R_{\theta JA}$ | 21 | °C/W | 1, 2 |
| Junction-to-ambient natural convection on four-layer board (2s2p) | $R_{\theta JMA}$ | 15 | °C/W | 1, 3 |
| Junction-to-ambient (@ 200 ft/min) on single-layer board (1s) | $R_{\theta JMA}$ | 17 | °C/W | 1, 3 |
| Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p) | $R_{\theta JMA}$ | 12 | °C/W | 1, 3 |
| Junction-to-board thermal | $R_{\theta JB}$ | 6 | °C/W | 4 |

many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_J$ = junction temperature (°C)
$T_A$ = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D$ = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

### 20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter ($\Psi_{JT}$) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = junction temperature (°C)
$T_T$ = thermocouple temperature on top of package (°C)
$\Psi_{JT}$ = junction-to-ambient thermal resistance (°C/W)
$P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### 20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_C$ = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$P_D$ = power dissipation (W)

THIS PAGE INTENTIONALLY LEFT BLANK