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Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347ezuagd

1 Overview

This section provides a high-level overview of the MPC8347E features. [Figure 1](#) shows the major functional units within the MPC8347E.

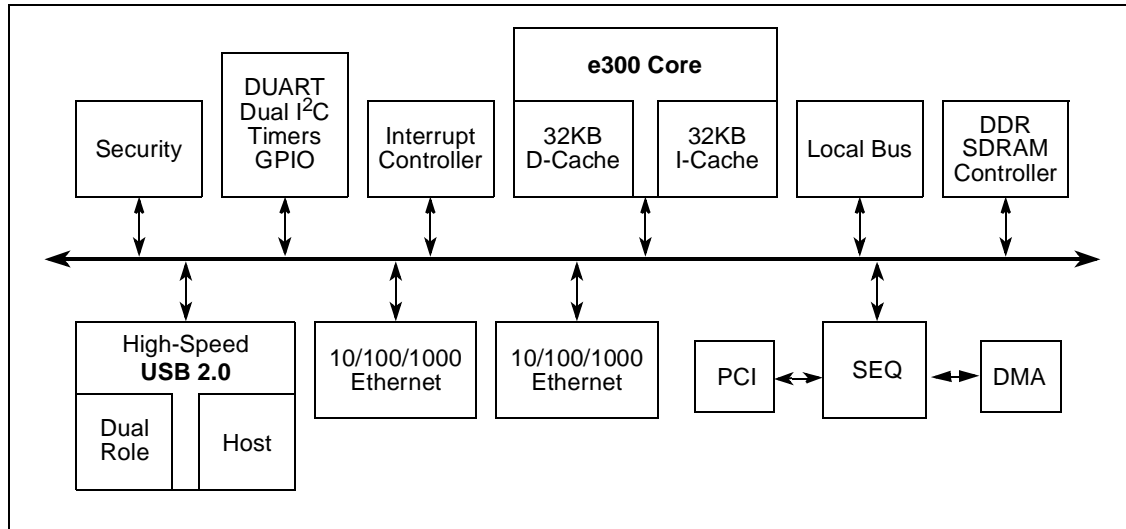


Figure 1. MPC8347E Block Diagram

Major features of the MPC8347E are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR SDRAM memory controller
 - Programmable timing for DDR-1 SDRAM
 - 32- or 64-bit data interface, up to 333-MHz data rate for TBGA, 266 MHz for PBGA
 - Four banks of memory, each up to 1 Gbyte
 - DRAM chip configurations from 64 Mbit to 1 Gbit with x8/x16 data ports
 - Full error checking and correction (ECC) support
 - Page mode support (up to 16 simultaneous open pages)
 - Contiguous or discontiguous memory mapping
 - Read-modify-write support
 - Sleep mode for self-refresh SDRAM
 - Auto refresh

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8347E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	$1.2\text{ V} \pm 60\text{ mV}$	V	1
PLL supply voltage	AV_{DD}	$1.2\text{ V} \pm 60\text{ mV}$	V	1
DDR DRAM I/O supply voltage	GV_{DD}	$2.5\text{ V} \pm 125\text{ mV}$	V	
Three-speed Ethernet I/O supply voltage	LV_{DD1}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	
Three-speed Ethernet I/O supply voltage	LV_{DD2}	$3.3\text{ V} \pm 330\text{ mV}$ $2.5\text{ V} \pm 125\text{ mV}$	V	
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage	OV_{DD}	$3.3\text{ V} \pm 330\text{ mV}$	V	

Note:

¹ GV_{DD} , LV_{DD} , OV_{DD} , AV_{DD} , and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8347E.

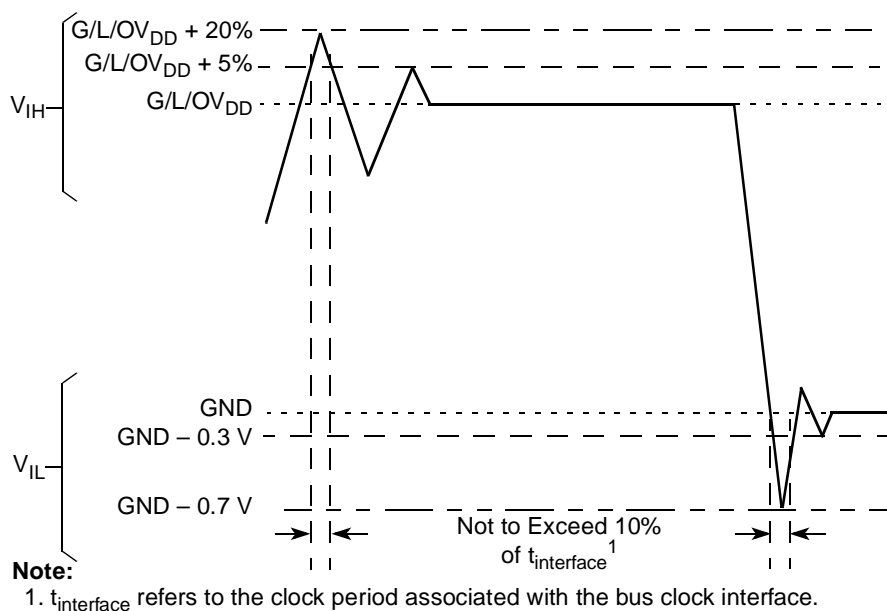


Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8347E.

5.1 RESET DC Electrical Characteristics

Table 8 provides the DC electrical characteristics for the RESET pins of the MPC8347E.

Table 8. RESET Pins DC Electrical Characteristics¹

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}			± 5	μA
Output high voltage ²	V_{OH}	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

Notes:

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

Table 9 provides the reset initialization AC timing specifications of the MPC8347E.

Table 9. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{\text{PCI_SYNC_IN}}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8347E is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the MPC8347E is in PCI agent mode	32	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8347E is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the MPC8347E is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1

8.3.2 MII Management AC Electrical Specifications

Table 30 provides the MII management AC timing specifications.

Table 30. MII Management AC Timing Specifications

At recommended operating conditions with V_{DD} is 3.3 V \pm 10% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 16 shows the MII management AC timing diagram.

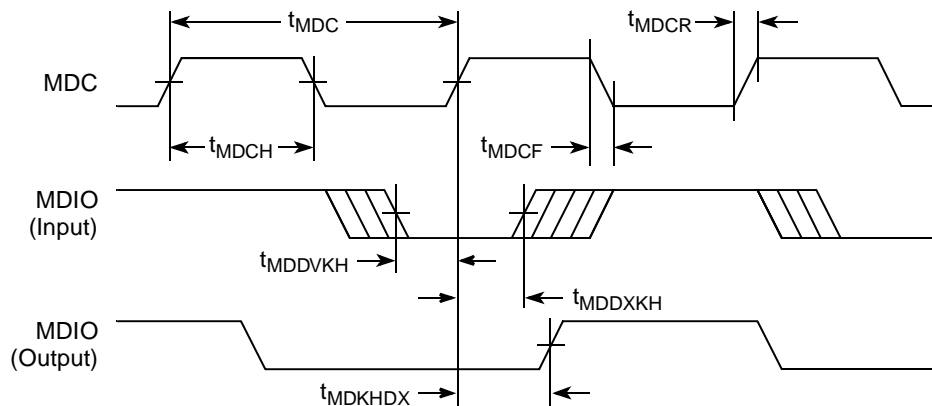


Figure 16. MII Management Interface Timing Diagram

Table 35. Local Bus General Timing Parameters—DLL Bypass⁹ (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid	t_{LBKLOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for $\overline{LGT\bar{A}}$ and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals to the load on the LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 19 provides the AC test load for the local bus.

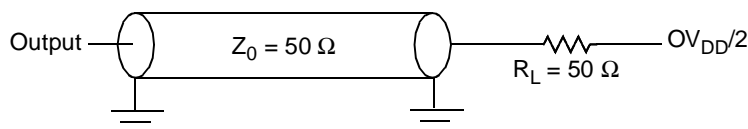
**Figure 19. Local Bus C Test Load**

Table 39. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μ s
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μ s
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

- The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8347E provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.
- The MPC8347E does not follow the "I²C-BUS Specifications" version 2.1 regarding the t_{I2CF} AC parameter.

Figure 31 provides the AC test load for the I²C.

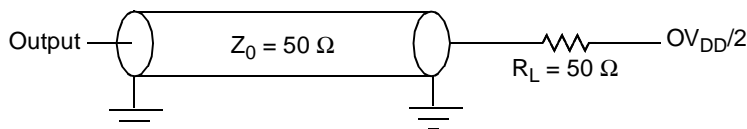
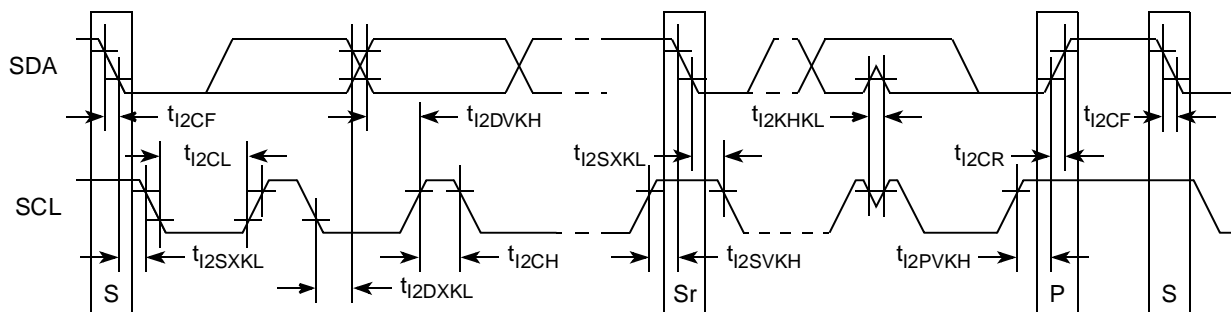
Figure 31. I²C AC Test Load

Figure 32 shows the AC timing diagram for the I²C bus.

Figure 32. I²C Bus AC Timing Diagram

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the external interrupt pins.

Table 47. IPIC DC Electrical Characteristics¹

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}		2.0	$OV_{DD} + 0.3$	V	
Input low voltage	V_{IL}		-0.3	0.8	V	
Input current	I_{IN}			±5	μA	
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V	2
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	2

Notes:

1. This table applies for pins $\overline{IRQ}[0:7]$, $\overline{IRQ_OUT}$, and $\overline{MCP_OUT}$.
2. $\overline{IRQ_OUT}$ and $\overline{MCP_OUT}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 48 provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC Timing Specifications¹

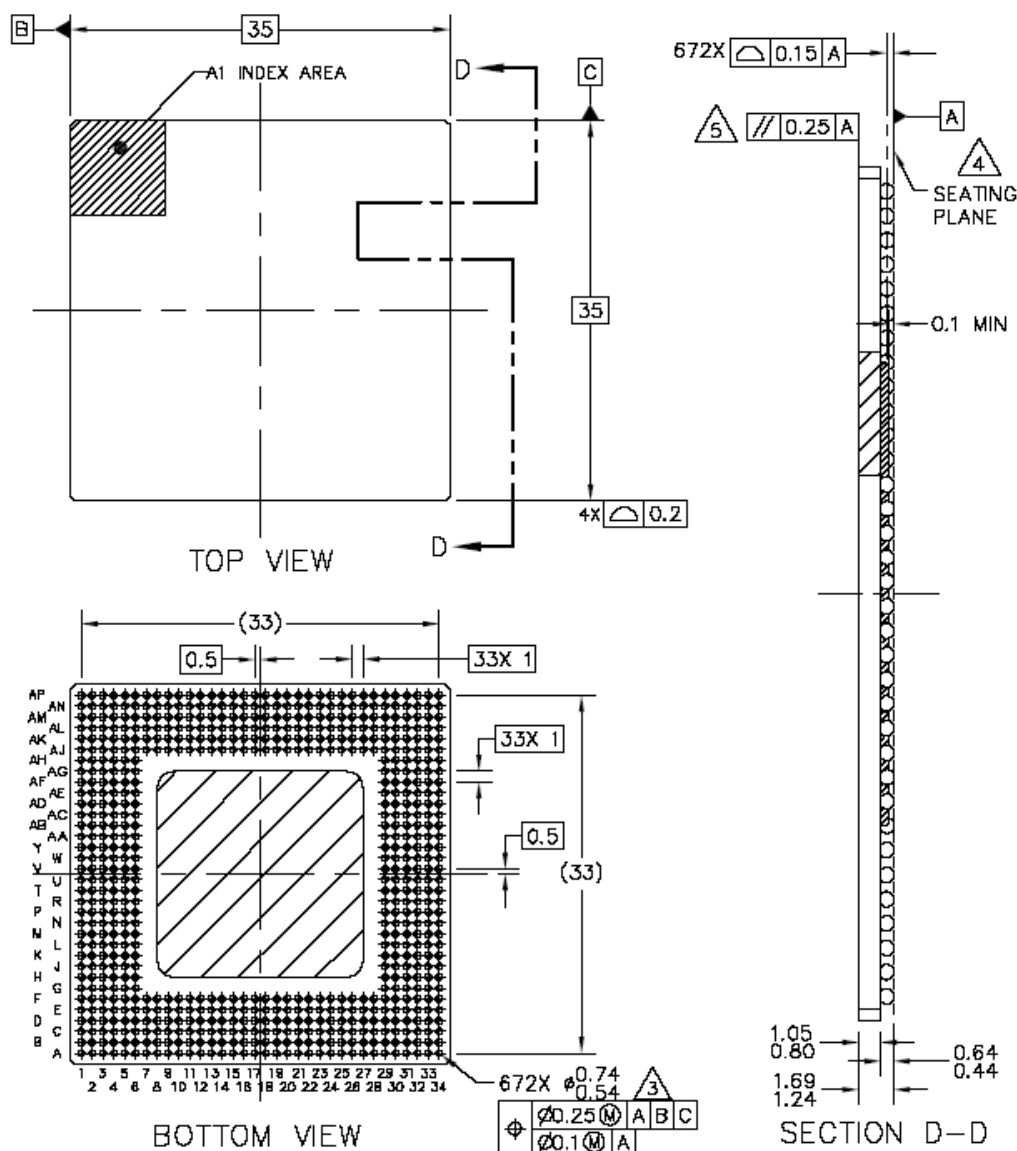
Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t_{PICWID}	20	ns

Notes:

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

18.2 Mechanical Dimensions for the MPC8347E TBGA

Figure 39 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 672-TBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 39. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E TBGA

18.3 Package Parameters for the MPC8347E PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.60 mm

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD2}	C6, D9	Power for three-speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV _{DD2}	
V _{DD}	E19, E29, F7, F9, F11, F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V)	V _{DD}	
OV _{DD}	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	
MVREF1	M3	I	DDR reference voltage	
MVREF2	AD2	I	DDR reference voltage	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_IRDY	E13	I/O	OV _{DD}	5
PCI1_STOP	C13	I/O	OV _{DD}	5
PCI1_DEVSEL	B13	I/O	OV _{DD}	5
PCI1_IDSEL	C17	I	OV _{DD}	
PCI1_SERR	C12	I/O	OV _{DD}	5
PCI1_PERR	B12	I/O	OV _{DD}	5
PCI1_REQ[0]	A21	I/O	OV _{DD}	
PCI1_REQ[1]/CPCI1_HS_ES	C19	I	OV _{DD}	
PCI1_REQ[2:4]	C18, A19, E20	I	OV _{DD}	
PCI1_GNT0	B20	I/O	OV _{DD}	
PCI1_GNT1/CPCI1_HS_LED	C20	O	OV _{DD}	
PCI1_GNT2/CPCI1_HS_ENUM	B19	O	OV _{DD}	
PCI1_GNT[3:4]	A20, E18	O	OV _{DD}	
M66EN	L26	I	OV _{DD}	
DDR SDRAM Memory Interface				
MDQ[0:63]	AC25, AD27, AD25, AH27, AE28, AD26, AD24, AF27, AF25, AF28, AH24, AG26, AE25, AG25, AH26, AH25, AG22, AH22, AE21, AD19, AE22, AF23, AE19, AG20, AG19, AD17, AE16, AF16, AF18, AG18, AH17, AH16, AG9, AD12, AG7, AE8, AD11, AH9, AH8, AF6, AF8, AE6, AF1, AE4, AG8, AH3, AG3, AG4, AH2, AD7, AB4, AB3, AG1, AD5, AC2, AC1, AC4, AA3, Y4, AA4, AB1, AB2, Y5, Y3	I/O	GV _{DD}	
MECC[0:4]/MSRCID[0:4]	AG13, AE14, AH12, AH10, AE15	I/O	GV _{DD}	
MECC[5]/MDVAL	AH14	I/O	GV _{DD}	
MECC[6:7]	AE13, AH11	I/O	GV _{DD}	
MDM[0:8]	AG28, AG24, AF20, AG17, AE9, AH5, AD1, AA2, AG12	O	GV _{DD}	
MDQS[0:8]	AE27, AE26, AE20, AH18, AG10, AF5, AC3, AA1, AH13	I/O	GV _{DD}	
MBA[0:1]	AF10, AF11	O	GV _{DD}	
MA[0:14]	AF13, AF15, AG16, AD16, AF17, AH20, AH19, AH21, AD18, AG21, AD13, AF21, AF22, AE1, AA5	O	GV _{DD}	
MWE	AD10	O	GV _{DD}	
MRAS	AF7	O	GV _{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCAS}}$	AG6	O	GV_{DD}	
$\overline{\text{MCS}}[0:3]$	AE7, AH7, AH4, AF2	O	GV_{DD}	
$\text{MCKE}[0:1]$	AG23, AH23	O	GV_{DD}	3
$\text{MCK}[0:5]$	AH15, AE24, AE2, AF14, AE23, AD3	O	GV_{DD}	
$\overline{\text{MCK}}[0:5]$	AG15, AD23, AE3, AG14, AF24, AD2	O	GV_{DD}	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
$\text{MODT}[0:3]$	AG5, AD4, AH6, AF4	—	—	
$\text{MBA}[2]$	AD22			
SPARE1	AF12	—	—	7
SPARE2	AG11	—	—	6
Local Bus Controller Interface				
$\text{LAD}[0:31]$	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV_{DD}	
$\text{LDP}[0]/\overline{\text{CKSTOP_OUT}}$	H1	I/O	OV_{DD}	
$\text{LDP}[1]/\overline{\text{CKSTOP_IN}}$	K5	I/O	OV_{DD}	
$\text{LDP}[2]$	H2	I/O	OV_{DD}	
$\text{LDP}[3]$	G1	I/O	OV_{DD}	
$\text{LA}[27:31]$	J4, H3, G2, F1, G3	O	OV_{DD}	
$\overline{\text{LCS}}[0:3]$	J5, H4, F2, E1	O	OV_{DD}	
$\overline{\text{LWE}}[0:3]/\text{LSDDQM}[0:3]/\overline{\text{LBS}}[0:3]$	F3, G4, D1, E2	O	OV_{DD}	
LBCTL	H5	O	OV_{DD}	
LALE	E3	O	OV_{DD}	
$\text{LGPL0}/\text{LSDA10}/\text{cfg_reset_source0}$	F4	I/O	OV_{DD}	
$\text{LGPL1}/\overline{\text{LSDWE}}/\text{cfg_reset_source1}$	D2	I/O	OV_{DD}	
$\text{LGPL2}/\overline{\text{LSDRAS}}/\text{LOE}$	C1	O	OV_{DD}	
$\text{LGPL3}/\overline{\text{LSDCAS}}/\text{cfg_reset_source2}$	C2	I/O	OV_{DD}	
$\text{LGPL4}/\overline{\text{LGT\AA}}/\text{LUPWAIT}/\text{LPBSE}$	C3	I/O	OV_{DD}	
$\text{LGPL5}/\text{cfg_clkin_div}$	B3	I/O	OV_{DD}	
LCKE	E4	O	OV_{DD}	
$\text{LCLK}[0:2]$	D4, A3, C4	O	OV_{DD}	
LSYNC_OUT	U3	O	OV_{DD}	
LSYNC_IN	Y2	I	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV _{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV _{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV _{DD}	
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV _{DD}	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV _{DD}	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV _{DD}	
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV _{DD}	
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV _{DD}	
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV _{DD}	
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV _{DD}	
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV _{DD}	
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV _{DD}	
MPH0_CLK/DR_RX_VALID	C21	I	OV _{DD}	
Programmable Interrupt Controller				
MCP_OUT	E8	O	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	J28	I/O	OV _{DD}	
IRQ[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV _{DD}	
IRQ[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV _{DD}	
IRQ[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV _{DD}	
Ethernet Management Interface				
EC_MDC	Y24	O	LV _{DD1}	
EC_MDIO	Y25	I/O	LV _{DD1}	2
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV _{DD1}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV _{DD}	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV _{DD1}	
TSEC1_GTX_CLK	V24	O	LV _{DD1}	3
TSEC1_RX_CLK	U26	I	LV _{DD1}	
TSEC1_RX_DV	U24	I	LV _{DD1}	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV _{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV _{DD}	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV _{DD1}	
TSEC1_TX_CLK	N25	I	OV _{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF1	AF19	I	DDR reference voltage	
MVREF2	AE10	I	DDR reference voltage	
No Connection				
NC	V1, V2, V5			

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be left not connected.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
10. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8347E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8347E system, and the MPC8347E itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the MPC8347E. These capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μF (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the MPC8347E.

21.5 Output Buffer DC Impedance

The MPC8347E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see [Figure 43](#)). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

22 Document Revision History

Table 66 provides a revision history of this document.

Table 66. Document Revision History

Revision	Date	Substantive Change(s)
11	2/2009	<p>In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2)" from bulleted list.</p> <p>In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins."</p> <p>In Table 35, removed row for rise time (t_{12CR}). Removed minimum value of t_{12CF}. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the t_{12CF} AC parameter.</p> <p>In Table 54, corrected the max csb_clk to 266 MHz.</p> <p>In Table 60, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz</p> <p>In Table 35, corrected t_{LBKHOV} parametr to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 21, Figure 23, and Figure 24 for output signals.</p> <p>Added Figure 1 and Figure 4.</p> <p>In Table 9.2, clarified that AC table is for ULPI only.</p> <p>Added footnote 4 to Table 67.</p> <p>In Table 67, updated note 1 to say the following: "For temperature range = C, processor frequency is up to 667(TBGA) with a platform frequency of 333 and limited to 400 (PBGA) with a platform frequency of 266."</p> <p>Added footnote 10 and 11 to Table 51 and Table 52.</p> <p>In Table 51, Table 52, updated note 11 to say the following: "SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net."</p> <p>Added footnote 6 to Table 7.</p> <p>In Table 7, updated the note 6 to say the following: "The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency."</p> <p>In 8.1.1, removed the note "The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver power supply (that is, a RGMII driver powered from a 3.6 V supply driving VOH into a RGMII receiver powered from a 2.5-V supply). Tolerance for dissimilar RGMII driver and receiver supply potentials is implicit in these specifications."</p>
10	4/2007	<p>In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row.</p> <p>In Table 54, "Operating Frequencies for TBGA," added column for 400 MHz.</p> <p>In Section 21.7, "Pull-Up Resistor Requirements," deleted last two paragraphs and after first paragraph, added a new paragraph.</p> <p>Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."</p>
9	3/2007	<p>In Table 54, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (csb_clk)' row, changed the value in the 533 MHz column to 100–333.</p> <p>In Table 60, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110.</p> <p>In Section 23, "Ordering Information," replaced first paragraph and added a note.</p> <p>In Section 23.1, "Part Numbers Fully Addressed by This Document," replaced first paragraph.</p>

Table 66. Document Revision History (continued)

Revision	Date	Substantive Change(s)
8	2/2007	<p>Page 1, updated first paragraph to reflect PowerQUICC II information. Updated note after second paragraph.</p> <p>In the features list in Section 1, "Overview," corrected DDR data rate to show:</p> <ul style="list-style-type: none"> • 266 MHz for PBGA parts for all silicon revisions • 333 MHz for DDR for TBGA parts for silicon Rev. 1.x <p>In Table 5, "MPC8347E Typical I/O Power Dissipation," added GV_{DD} 1.8-V values for DDR2; added table footnote to designate rates that apply only to the TBGA package.</p> <p>In Figure 43, "JTAG Interface Connection," updated with new figure.</p> <p>In Section 23, "Ordering Information," replicated note from document introduction.</p> <p>In Section 23.1, "Part Numbers Fully Addressed by This Document," replaced third sentence of first paragraph directing customer to product summary page for available frequency configuration parts. Updated back page information.</p>
7	8/2006	<p>Changed all references to revision 2.0 silicon to revision 3.0 silicon.</p> <p>Changed V_{IH} minimum value in Table 36, "JTAG Interface DC Electrical Characteristics," to $OV_{DD} - 0.3$.</p> <p>In Table 60, "Suggested PLL Configurations," deleted reference-number rows 902 and 703.</p>
6	3/2006	<p>Section 2, "Electrical Characteristics," moved to second section and all other section, table, and figure numbering change accordingly.</p> <p>Table 7, "CLKIN AC Timing Specifications:" Changed max rise and fall time from 1.2 to 2.3.</p> <p>Table 22, "GMII Receive AC Timing Specifications:" Changed min t_{TTKHDX} from 0.5 to 1.0.</p> <p>Table 30, "MII Management AC Timing Specifications:" Changed max value of t_{MDKHDX} from 70 to 170.</p> <p>Table 34, "Local Bus General Timing Parameters—DLL on:" Changed min $t_{LBIVKH2}$ from 1.7 to 2.2.</p> <p>Table 36, "JTAG interface DC Electrical Characteristics:" Changed V_{IH} input high voltage min to 2.0.</p> <p>Table 54, "Operating Frequencies for TBGA:"</p> <ul style="list-style-type: none"> • Updated TBD values. • Changed maximum coherent system bus frequency for TBGA 667-MHz device to 333 MHz. <p>Table 55, "Operating Frequencies for PBGA:"</p> <ul style="list-style-type: none"> • Updated TBD values. • Changed PBGA maximum coherent system bus frequency to 266 MHz, and maximum DDR memory bus frequency to 133 MHz. <p>Table 60, "Suggested PLL Configurations": Removed some values from suggested PLL configurations for reference numbers 902, 922, 903, and 923.</p> <p>Table 67, "Part Numbering Nomenclature": Updated TBD values in note 1.</p> <p>Added Table 68, "SVR Settings."</p> <p>Added Section 23.2, "Part Marking."</p>
5	10/2005	In Table 57, updated AAVID 30x30x9.4 mm Pin Fin (natural convection) junction-to-ambient thermal resistance, from 11 to 10.
4	9/2005	Added Table 2, "MPC8347E Typical I/O Power Dissipation."
3	8/2005	Table 1: Updated values for power dissipation that were TBD in Revision 2.
2	5/2005	<p>Table 1: Typical values for power dissipation are changed to TBD.</p> <p>Table 48: Footnote numbering was wrong. THERM0 should have footnote 9 instead of 8.</p>

Table 66. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1	4/2005	Table 1: Addition of note 1 Table 48: Addition of Therm0 (K32) Table 49: Addition of Therm0 (B15)
0	4/2005	Initial release.

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