NXP USA Inc. - MPC8347EZUAGDB Datasheet

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347ezuagdb

1 Overview

This section provides a high-level overview of the MPC8347E features. Figure 1 shows the major functional units within the MPC8347E.

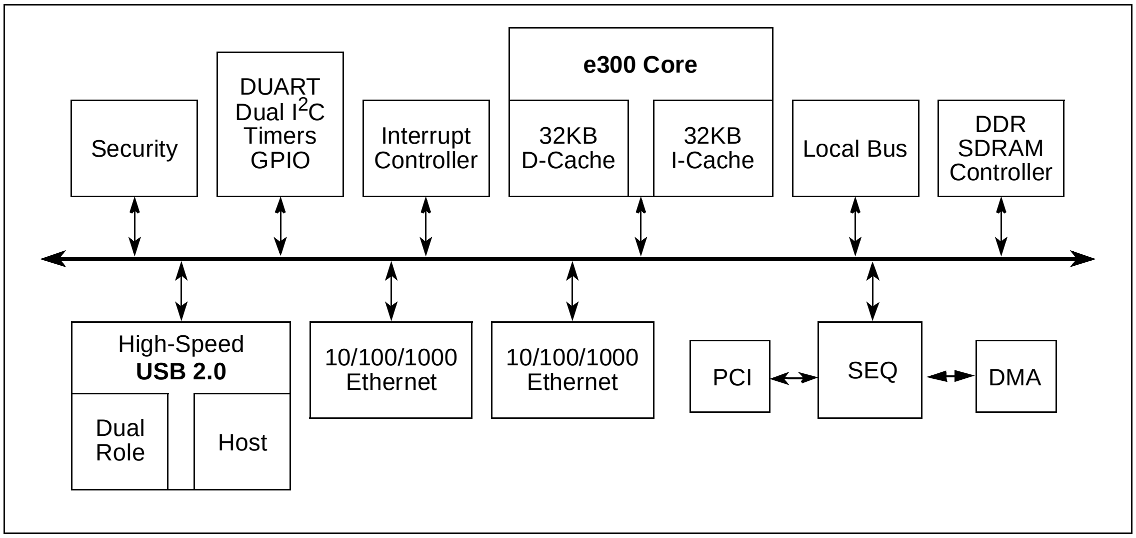

Figure 1. MPC8347E Block Diagram

Major features of the MPC8347E are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology
- Double data rate, DDR SDRAM memory controller
  - Programmable timing for DDR-1 SDRAM
  - 32- or 64-bit data interface, up to 333-MHz data rate for TBGA, 266 MHz for PBGA
  - Four banks of memory, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbit to 1 Gbit with x8/x16 data ports
  - Full error checking and correction (ECC) support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep mode for self-refresh SDRAM
  - Auto refresh

  - On-the-fly power management using CKE
  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3®, 802.3u®, 820.3x®, 802.3z®, 802.3ac® standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- PCI interface
  - Designed to comply with *PCI Specification Revision 2.2*
  - Data bus width:
    - 32-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities
  - PCI agent mode on PCI interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration supporting five masters on PCI
  - Accesses to all PCI address spaces
  - Parity supported
  - Selectable hardware-enforced coherency
  - Address translation units for address mapping between host and peripheral
  - Dual address cycle for target
  - Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
  - Public key execution unit (PKEU) :
    - RSA and Diffie-Hellman algorithms

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8347E.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8347E.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	$0\ V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	µA
PCI_SYNC_IN input current	$0\ V \le V_{IN} \le 0.5\ V$ or $OV_{DD} - 0.5\ V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	µA
PCI_SYNC_IN input current	$0.5\ V \le V_{IN} \le OV_{DD} - 0.5\ V$	I_{IN}	—	±50	µA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8347E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8347E.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency.

Table 9. RESET Initialization Timing Specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	
Time for the MPC8347E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8347E to turn on POR configuration signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*.
3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 lists the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, “Clocking.”

Table 16. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the MPC8347E timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 43. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

14.2 Timer AC Timing Specifications

Table 44 provides the timer input and output AC timing specifications.

Table 44. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the MPC8347E GPIO.

Table 45. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 46 provides the GPIO input and output AC timing specifications.

Table 46. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the external interrupt pins.

Table 47. IPIC DC Electrical Characteristics[1]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}		2.0	OV_{DD} + 0.3	V	
Input low voltage	V_{IL}		–0.3	0.8	V	
Input current	I_{IN}			±5	μA	
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V	2
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	2

Notes:

1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, and $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 48 provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PICWID}	20	ns

Notes:

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 49 provides the SPI DC electrical characteristics.

Table 49. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	µA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 50 provides the SPI input and output AC timing specifications.

Table 50. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

18.3 Package Parameters for the MPC8347E PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.60 mm

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LBCTL	AN26	O	OV_{DD}	
LALE	AK24	O	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV_{DD}	
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	AL25	I/O	OV_{DD}	
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	AJ24	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	AN27	I/O	OV_{DD}	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	AP28	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AL26	I/O	OV_{DD}	
LCKE	AM27	O	OV_{DD}	
LCLK[0:2]	AN28, AK26, AP29	O	OV_{DD}	
LSYNC_OUT	AM12	O	OV_{DD}	
LSYNC_IN	AJ10	I	OV_{DD}	
General Purpose I/O Timers				
GPIO1[0]/GTM1_TIN1/GTM2_TIN2	F24	I/O	OV_{DD}	
GPIO1[1]/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	E24	I/O	OV_{DD}	
GPIO1[2]/$\overline{\text{GTM1\_TOUT1}}$	B25	I/O	OV_{DD}	
GPIO1[3]/GTM1_TIN2/GTM2_TIN1	D24	I/O	OV_{DD}	
GPIO1[4]/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	A25	I/O	OV_{DD}	
GPIO1[5]/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	B24	I/O	OV_{DD}	
GPIO1[6]/GTM1_TIN3/GTM2_TIN4	A24	I/O	OV_{DD}	
GPIO1[7]/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	D23	I/O	OV_{DD}	
GPIO1[8]/$\overline{\text{GTM1\_TOUT3}}$	B23	I/O	OV_{DD}	
GPIO1[9]/GTM1_TIN4/GTM2_TIN3	A23	I/O	OV_{DD}	
GPIO1[10]/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	F22	I/O	OV_{DD}	
GPIO1[11]/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	E22	I/O	OV_{DD}	
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	A26	I/O	OV_{DD}	
MPH1_D1_SER_TXD/DR_D1_SER_TXD	B26	I/O	OV_{DD}	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	D25	I/O	OV_{DD}	
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV_{DD}	
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV_{DD}	
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV_{DD}	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	D26	I/O	OV_{DD}	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	E26	I/O	OV_{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
System Control				
$\overline{\text{PORESET}}$	C18	I	OV$_{DD}$	
$\overline{\text{HRESET}}$	B18	I/O	OV$_{DD}$	1
$\overline{\text{SRESET}}$	D18	I/O	OV$_{DD}$	2
Thermal Management				
THERM0	K32	I	—	9
Power and Ground Signals				
AV$_{DD}$1	L31	Power for e300 PLL (1.2 V)	AV$_{DD}$1	
AV$_{DD}$2	AP12	Power for system PLL (1.2 V)	AV$_{DD}$2	
AV$_{DD}$3	AE1	Power for DDR DLL (1.2 V)	AV$_{DD}$3	
AV$_{DD}$4	AJ13	Power for LBIU DLL (1.2 V)	AV$_{DD}$4	
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34	—	—	
GV$_{DD}$	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV$_{DD}$	
LV$_{DD}$1	C9, D11	Power for three-speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV$_{DD}$1	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connection				
NC	W32, AA31, AA32, AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30, AC32, AE32, AH31, AL32, AG34, AE33, AF32, AE34, AF34, AF33, AG33, AG32, AL11, AM11, AP10, Y32, Y34, Y31, Y33	—	—	

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be pulled up to OV_{DD}.
8. This pin must always be left not connected.
9. Thermal sensitive resistor.
10. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
11. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

Table 52 provides the pinout listing for the MPC8347E, 620 PBGA package.

Table 52. MPC8347E (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI1_INTA/IRQ_OUT	D20	O	OV_{DD}	2
PCI1_RESET_OUT	B21	O	OV_{DD}	
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV_{DD}	
PCI1_C/BE[3:0]	A17, A14, A11, B10	I/O	OV_{DD}	
PCI1_PAR	D13	I/O	OV_{DD}	
PCI1_FRAME	B14	I/O	OV_{DD}	5
PCI1_TRDY	A13	I/O	OV_{DD}	5

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCAS}}$	AG6	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	AE7, AH7, AH4, AF2	O	GV_{DD}	
MCKE[0:1]	AG23, AH23	O	GV_{DD}	3
MCK[0:5]	AH15, AE24, AE2, AF14, AE23, AD3	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	AG15, AD23, AE3, AG14, AF24, AD2	O	GV_{DD}	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
MODT[0:3]	AG5, AD4, AH6, AF4	—	—	
MBA[2]	AD22			
SPARE1	AF12	—	—	7
SPARE2	AG11	—	—	6
Local Bus Controller Interface				
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV_{DD}	
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	H1	I/O	OV_{DD}	
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	K5	I/O	OV_{DD}	
LDP[2]	H2	I/O	OV_{DD}	
LDP[3]	G1	I/O	OV_{DD}	
LA[27:31]	J4, H3, G2, F1, G3	O	OV_{DD}	
$\overline{\text{LCS}}$[0:3]	J5, H4, F2, E1	O	OV_{DD}	
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	F3, G4, D1, E2	O	OV_{DD}	
LBCTL	H5	O	OV_{DD}	
LALE	E3	O	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	F4	I/O	OV_{DD}	
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	D2	I/O	OV_{DD}	
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	C1	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	C2	I/O	OV_{DD}	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	B3	I/O	OV_{DD}	
LCKE	E4	O	OV_{DD}	
LCLK[0:2]	D4, A3, C4	O	OV_{DD}	
LSYNC_OUT	U3	O	OV_{DD}	
LSYNC_IN	Y2	I	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV_{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV_{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV_{DD}	
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV_{DD}	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV_{DD}	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV_{DD}	
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV_{DD}	
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV_{DD}	
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV_{DD}	
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV_{DD}	
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV_{DD}	
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV_{DD}	
MPH0_CLK/DR_RX_VALID	C21	I	OV_{DD}	
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E8	O	OV_{DD}	2
$\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12]	J28	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV_{DD}	
$\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV_{DD}	
Ethernet Management Interface				
EC_MDC	Y24	O	LV_{DD1}	
EC_MDIO	Y25	I/O	LV_{DD1}	2
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV_{DD1}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV_{DD}	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV_{DD1}	
TSEC1_GTX_CLK	V24	O	LV_{DD1}	3
TSEC1_RX_CLK	U26	I	LV_{DD1}	
TSEC1_RX_DV	U24	I	LV_{DD1}	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV_{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV_{DD}	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV_{DD1}	
TSEC1_TX_CLK	N25	I	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[7:4]/GPIO2[27:30]	N28, P25, P26, P27	I/O	OV_{DD}	
TSEC1_TXD[3:0]	V28, V27, V26, W28	O	LV_{DD1}	10
TSEC1_TX_EN	W27	O	LV_{DD1}	
TSEC1_TX_ER/GPIO2[31]	N24	I/O	OV_{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	P28	I/O	OV_{DD}	
TSEC2_CRS/GPIO1[22]	AC28	I/O	LV_{DD2}	
TSEC2_GTX_CLK	AC27	O	LV_{DD2}	
TSEC2_RX_CLK	AB25	I	LV_{DD2}	
TSEC2_RX_DV/GPIO1[23]	AC26	I/O	LV_{DD2}	
TSEC2_RXD[7:4]/GPIO1[26:29]	R28, T24, T25, T26	I/O	OV_{DD}	
TSEC2_RXD[3:0]/GPIO1[13:16]	AA25, AA26, AA27, AA28	I/O	LV_{DD2}	
TSEC2_RX_ER/GPIO1[25]	R25	I/O	OV_{DD}	
TSEC2_TXD[7]/GPIO1[31]	T27	I/O	OV_{DD}	
TSEC2_TXD[6]/DR_XCVR_TERM_SEL	T28	O	OV_{DD}	
TSEC2_TXD[5]/DR_UTMI_OPMODE1	U28	O	OV_{DD}	
TSEC2_TXD[4]/DR_UTMI_OPMODE0	U27	O	OV_{DD}	
TSEC2_TXD[3:0]/GPIO1[17:20]	AB26, AB27, AA24, AB28	I/O	LV_{DD2}	
TSEC2_TX_ER/GPIO1[24]	R27	I/O	OV_{DD}	
TSEC2_TX_EN/GPIO1[12]	AD28	I/O	LV_{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	R26	I/O	OV_{DD}	
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	B4, A4	O	OV_{DD}	
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	D5, C5	I/O	OV_{DD}	
$\overline{\text{UART\_CTS}}$[1]/MSRCID4/LSRCID4	B5	I/O	OV_{DD}	
$\overline{\text{UART\_CTS}}$[2]/MDVAL/LDVAL	A5	I/O	OV_{DD}	
$\overline{\text{UART\_RTS}}$[1:2]	D6, C6	O	OV_{DD}	
I^2C interface				
IIC1_SDA	E5	I/O	OV_{DD}	2
IIC1_SCL	A6	I/O	OV_{DD}	2
IIC2_SDA	B6	I/O	OV_{DD}	2
IIC2_SCL	E7	I/O	OV_{DD}	2
SPI				
SPIMOSI	D7	I/O	OV_{DD}	

Table 62. Package Thermal Characteristics for PBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{\theta JC}$	5	°C/W	5
Junction-to-package natural convection on top	ψ_{JT}	5	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

P_D = power dissipation (W)

22 Document Revision History

Table 66 provides a revision history of this document.

Table 66. Document Revision History

Revision	Date	Substantive Change(s)
11	2/2009	In Section 21.1, “System Clocking,” removed “(AVDD1)” and “(AVDD2”) from bulleted list. In Section 21.2, “PLL Power Supply Filtering,” in the second paragraph, changed “provide five independent filter circuits,” and “the five AVDD pins” to provide four independent filter circuits,” and “the four AVDD pins.” In Table 35, removed row for rise time (t_{I2CR}). Removed minimum value of t_{I2CF}. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the t_{I2CF} AC parameter. In Table 54, corrected the max csb_clk to 266 MHz. In Table 60, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz In Table 35, corrected t_{LBKHOV} parametr to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 21, Figure 23, and Figure 24 for output signals. Added Figure 1 and Figure 4. In Table 9.2, clarified that AC table is for ULPI only. Added footnote 4 to Table 67. In Table 67, updated note 1 to say the following: “For temperature range = C, processor frequency is up to 667(TBGA) with a platform frequency of 333 and limited to 400 (PBGA) with a platform frequency of 266.” Added footnote 10 and 11 to Table 51 and Table 52. In Table 51, Table 52, updated note 11 to say the following: “SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.” Added footnote 6 to Table 7. In Table 7, updated the note 6 to say the following: “The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency.” In 8.1.1, removed the note “The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver power supply (that is, a RGMII driver powered from a 3.6 V supply driving VOH into a RGMII receiver powered from a 2.5-V supply). Tolerance for dissimilar RGMII driver and receiver supply potentials is implicit in these specifications.”
10	4/2007	In Table 3, “Output Drive Capability,” changed the values in the Output Impedance column and added USB to the seventh row. In Table 54, “Operating Frequencies for TBGA,” added column for 400 MHz. In Section 21.7, “Pull-Up Resistor Requirements,” deleted last two paragraphs and after first paragraph, added a new paragraph. Deleted Section 21.8, “JTAG Configuration Signals,” and Figure 43, “JTAG Interface Connection.”
9	3/2007	In Table 54, “Operating Frequencies for TBGA,” in the ‘Coherent system bus frequency (*csb_clk*)’ row, changed the value in the 533 MHz column to 100–333. In Table 60, “Suggested PLL Configurations,” under the subhead, ‘33 MHz CLKIN/PCI_CLK Options,’ added row A03 between Ref. No. 724 and 804. Under the subhead ‘66 MHz CLKIN/PCI_CLK Options,’ added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. In Section 23, “Ordering Information,” replaced first paragraph and added a note. In Section 23.1, “Part Numbers Fully Addressed by This Document,” replaced first paragraph.

Table 66. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1	4/2005	Table 1: Addition of note 1 Table 48: Addition of Therm0 (K32) Table 49: Addition of Therm0 (B15)
0	4/2005	Initial release.