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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347vvagd

  - Programmable field size up to 2048 bits
  - Elliptic curve cryptography
  - F2m and F(p) modes
  - Programmable field size up to 511 bits
- Data encryption standard (DES) execution unit (DEU)
  - DES and 3DES algorithms
  - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
  - ECB and CBC modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rijndael symmetric-key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, and counter (CTR) modes
- ARC four execution unit (AFEU)
  - Stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
  - Static and/or dynamic assignment of crypto-execution units through an integrated controller
  - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

- Universal serial bus (USB) dual role controller
  - USB on-the-go mode with both device and host functionality
  - Complies with USB specification Rev. 2.0
  - Can operate as a stand-alone USB device
    - One upstream facing port
    - Six programmable USB endpoints
  - Can operate as a stand-alone USB host controller
    - USB root hub with one downstream-facing port
    - Enhanced host controller interface (EHCI) compatible
    - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
  - Can operate as a stand-alone USB host controller
    - USB root hub with one or two downstream-facing ports

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8347E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

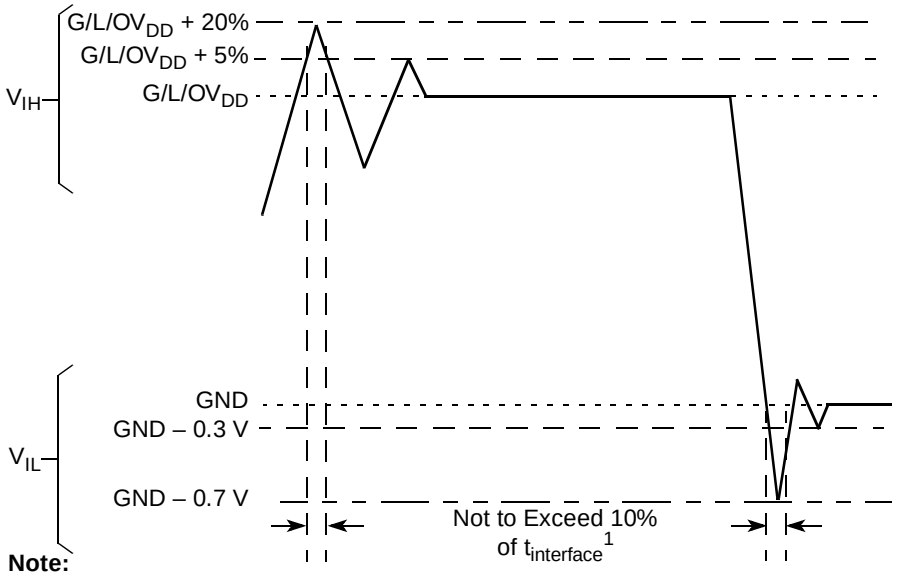
Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR DRAM I/O supply voltage	GV_{DD}	2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	LV_{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	LV_{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	3.3 V ± 330 mV	V	

Note:

1 GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8347E.



Note:

1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8347E.

7.1 DUART DC Electrical Characteristics

Table 17 provides the DC electrical characteristics for the DUART interface of the MPC8347E.

Table 17. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (0.8 V ≤ V_{IN} ≤ 2 V)	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 18 provides the AC timing parameters for the DUART interface of the MPC8347E.

Table 18. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

Figure 10 shows the MII transmit AC timing diagram.

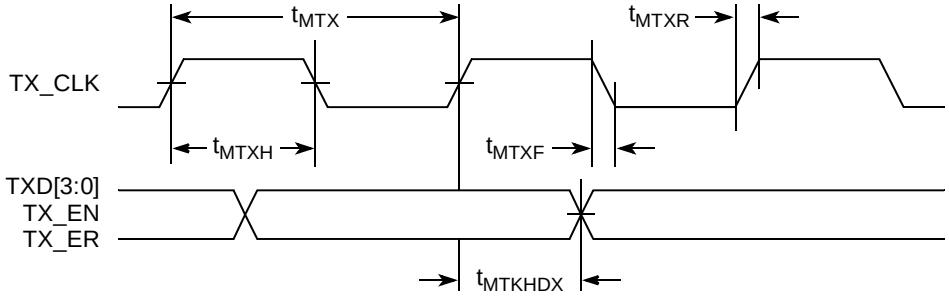


Figure 10. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular functionl. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 provides the AC test load for TSEC.

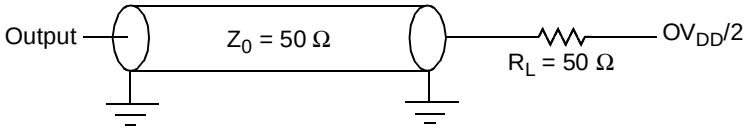


Figure 11. TSEC AC Test Load

Figure 15 shows the RBMII and RTBI AC timing and multiplexing diagrams.

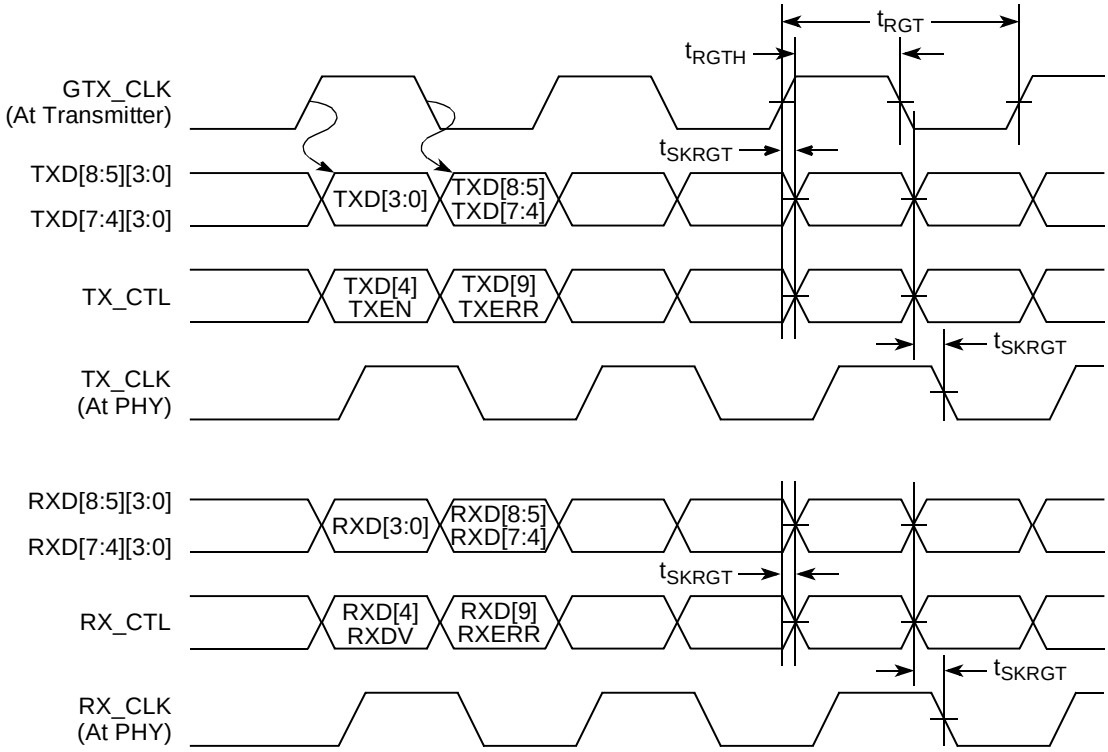


Figure 15. RGMII and RTBI AC Timing and Multiplexing Diagrams

Figure 17 and Figure 18 provide the AC test load and signals for the USB, respectively.

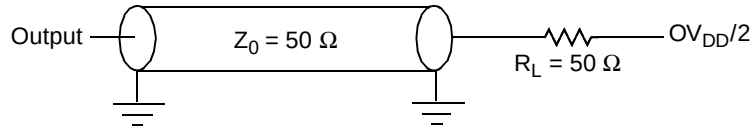


Figure 17. USB AC Test Load

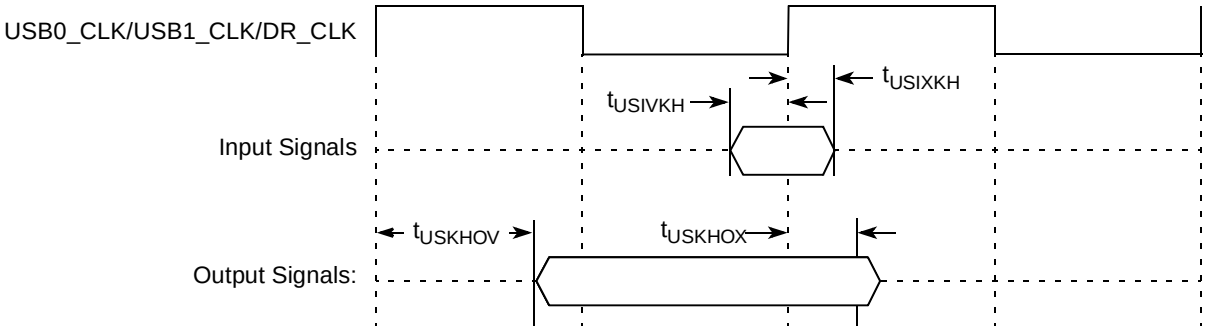


Figure 18. USB Signals

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E

11.1 JTAG DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E.

Table 36. JTAG interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		OV_{DD} – 0.3	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E. Table 37 provides the JTAG AC timing specifications as defined in Figure 27 through Figure 30.

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8347E.

12.1 I²C DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the I²C interface of the MPC8347E.

Table 38. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	4
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8349E Integrated Host Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 39 provides the AC timing parameters for the I²C interface of the MPC8347E. Note that all values refer to V_{IH}(min) and V_{IL}(max) levels (see Table 38).

Table 39. I²C AC Electrical Specifications

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	µs
High period of the SCL clock	t_{I2CH}	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	µs

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the MPC8347E timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 43. Timer DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

14.2 Timer AC Timing Specifications

Table 44 provides the timer input and output AC timing specifications.

Table 44. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Figure 36 provides the AC test load for the SPI.

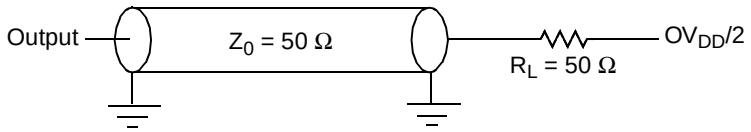
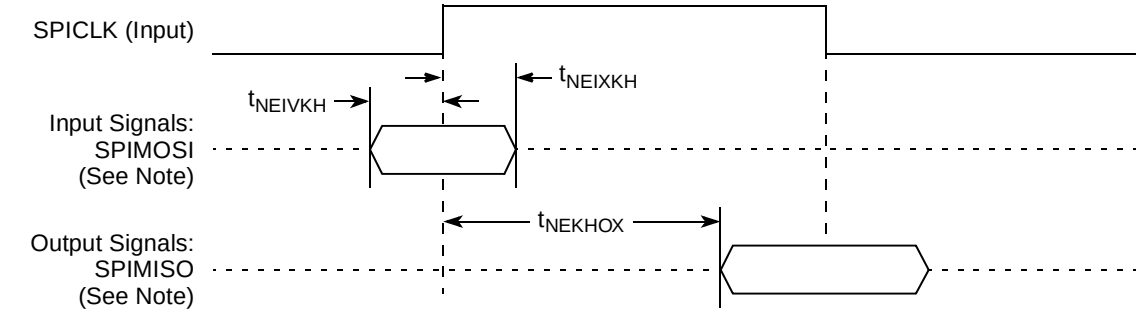


Figure 36. SPI AC Test Load

Figure 37 and Figure 38 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

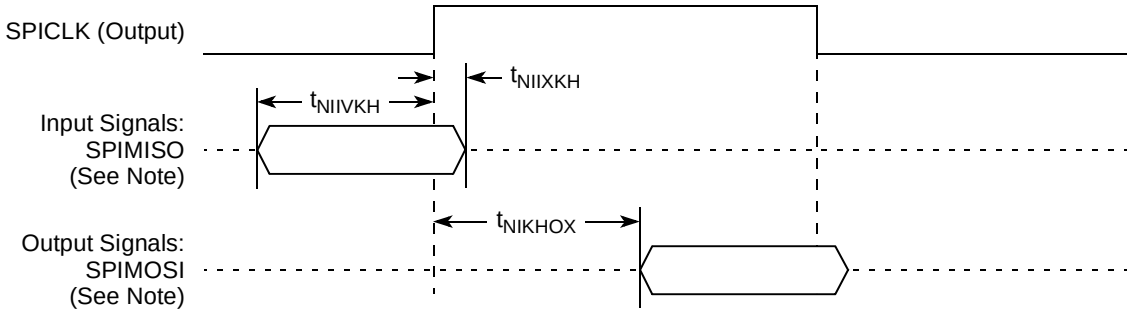
Figure 37 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 37. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 38 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 38. SPI AC Timing in Master Mode (Internal Clock) Diagram

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV_{DD}	
MECC[5]/MDVAL	U1	I/O	GV_{DD}	
MECC[6:7]	Y1, Y6	I/O	GV_{DD}	
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	O	GV_{DD}	
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV_{DD}	
MBA[0:1]	AD1, AA5	O	GV_{DD}	
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	O	GV_{DD}	
$\overline{\text{MWE}}$	AF1	O	GV_{DD}	
$\overline{\text{MRAS}}$	AF4	O	GV_{DD}	
$\overline{\text{MCAS}}$	AG3	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	AG2, AG1, AK1, AL4	O	GV_{DD}	
MCKE[0:1]	H3, G1	O	GV_{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	U3, E3, AN2, V4, E1, AM4	O	GV_{DD}	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
MODT[0:3]	AH3, AJ5, AH1, AJ4	—	—	
MBA[2]	H4	—	—	
SPARE1	AA1	—	—	8
SPARE2	AB1	—	—	6
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV_{DD}	
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	AM21	I/O	OV_{DD}	
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	AP22	I/O	OV_{DD}	
LDP[2]	AN22	I/O	OV_{DD}	
LDP[3]	AM22	I/O	OV_{DD}	
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV_{DD}	
$\overline{\text{LCS}}$[0:3]	AN24, AL23, AP25, AN25	O	OV_{DD}	
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	AK23, AP26, AL24, AM25	O	OV_{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$LV_{DD}2$	C6, D9	Power for three-speed Ethernet #2 I/O (2.5 V, 3.3 V)	$LV_{DD}2$	
V_{DD}	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V)	V_{DD}	
OV_{DD}	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	
MVREF1	M3	I	DDR reference voltage	
MVREF2	AD2	I	DDR reference voltage	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCAS}}$	AG6	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	AE7, AH7, AH4, AF2	O	GV_{DD}	
MCKE[0:1]	AG23, AH23	O	GV_{DD}	3
MCK[0:5]	AH15, AE24, AE2, AF14, AE23, AD3	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	AG15, AD23, AE3, AG14, AF24, AD2	O	GV_{DD}	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
MODT[0:3]	AG5, AD4, AH6, AF4	—	—	
MBA[2]	AD22			
SPARE1	AF12	—	—	7
SPARE2	AG11	—	—	6
Local Bus Controller Interface				
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV_{DD}	
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	H1	I/O	OV_{DD}	
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	K5	I/O	OV_{DD}	
LDP[2]	H2	I/O	OV_{DD}	
LDP[3]	G1	I/O	OV_{DD}	
LA[27:31]	J4, H3, G2, F1, G3	O	OV_{DD}	
$\overline{\text{LCS}}$[0:3]	J5, H4, F2, E1	O	OV_{DD}	
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	F3, G4, D1, E2	O	OV_{DD}	
LBCTL	H5	O	OV_{DD}	
LALE	E3	O	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	F4	I/O	OV_{DD}	
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	D2	I/O	OV_{DD}	
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	C1	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	C2	I/O	OV_{DD}	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	B3	I/O	OV_{DD}	
LCKE	E4	O	OV_{DD}	
LCLK[0:2]	D4, A3, C4	O	OV_{DD}	
LSYNC_OUT	U3	O	OV_{DD}	
LSYNC_IN	Y2	I	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
General Purpose I/O Timers				
GPIO1[0]/GTM1_TIN1/GTM2_TIN2	D27	I/O	OV_{DD}	
GPIO1[1]/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	E26	I/O	OV_{DD}	
GPIO1[2]/$\overline{\text{GTM1\_TOUT1}}$	D28	I/O	OV_{DD}	
GPIO1[3]/GTM1_TIN2/GTM2_TIN1	G25	I/O	OV_{DD}	
GPIO1[4]/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	J24	I/O	OV_{DD}	
GPIO1[5]/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	F26	I/O	OV_{DD}	
GPIO1[6]/GTM1_TIN3/GTM2_TIN4	E27	I/O	OV_{DD}	
GPIO1[7]/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	E28	I/O	OV_{DD}	
GPIO1[8]/$\overline{\text{GTM1\_TOUT3}}$	H25	I/O	OV_{DD}	
GPIO1[9]/GTM1_TIN4/GTM2_TIN3	F27	I/O	OV_{DD}	
GPIO1[10]/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	K24	I/O	OV_{DD}	
GPIO1[11]/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	G26	I/O	OV_{DD}	
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	C28	I/O	OV_{DD}	
MPH1_D1_SER_TXD/DR_D1_SER_TXD	F25	I/O	OV_{DD}	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	B28	I/O	OV_{DD}	
MPH1_D3_SPEED/DR_D3_SPEED	C27	I/O	OV_{DD}	
MPH1_D4_DP/DR_D4_DP	D26	I/O	OV_{DD}	
MPH1_D5_DM/DR_D5_DM	E25	I/O	OV_{DD}	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	C26	I/O	OV_{DD}	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	D25	I/O	OV_{DD}	
MPH1_NXT/DR_SESS_VLD_NXT	B26	I	OV_{DD}	
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	E24	I/O	OV_{DD}	
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	A27	O	OV_{DD}	
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	C25	I	OV_{DD}	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A26	O	OV_{DD}	
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	B25	O	OV_{DD}	
MPH1_CLK/DR_CLK	A25	I	OV_{DD}	
USB Port 0				
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	D24	I/O	OV_{DD}	
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	C24	I/O	OV_{DD}	

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 56 shows the multiplication factor encodings for the system PLL.

Table 56. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

As described in Section 19, “Clocking,” the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 57 and Table 58 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

20 Thermal

This section describes the thermal specifications of the MPC8347E.

20.1 Thermal Characteristics

Table 61 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8347E.

Table 61. Package Thermal Characteristics for TBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	3.8	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.7	°C/W	5
Junction-to-package natural convection on top	Ψ_{JT}	1	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 62 provides the package thermal characteristics for the 620 29 × 29 mm PBGA of the MPC8347E.

Table 62. Package Thermal Characteristics for PBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	17	°C/W	1, 3
Junction-to-ambient (@ 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	12	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	6	°C/W	4

Table 64. Heat Sink and Thermal Resistance of MPC8347E (PBGA) (continued)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	8.8
AAVID 31 × 35 × 23 mm pin fin	Natural convection	11.3
AAVID 31 × 35 × 23 mm pin fin	1 m/s	8.1
AAVID 31 × 35 × 23 mm pin fin	2 m/s	7.5
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	9.1
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	7.1
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	6.5
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	10.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	7.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	6.6
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	6.9

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

22 Document Revision History

Table 66 provides a revision history of this document.

Table 66. Document Revision History

Revision	Date	Substantive Change(s)
11	2/2009	In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list. In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." In Table 35, removed row for rise time (t_{I2CR}). Removed minimum value of t_{I2CF}. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the t_{I2CF} AC parameter. In Table 54, corrected the max csb_clk to 266 MHz. In Table 60, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz In Table 35, corrected t_{LBKHOV} parametr to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 21, Figure 23, and Figure 24 for output signals. Added Figure 1 and Figure 4. In Table 9.2, clarified that AC table is for ULPI only. Added footnote 4 to Table 67. In Table 67, updated note 1 to say the following: "For temperature range = C, processor frequency is up to 667(TBGA) with a platform frequency of 333 and limited to 400 (PBGA) with a platform frequency of 266." Added footnote 10 and 11 to Table 51 and Table 52. In Table 51, Table 52, updated note 11 to say the following: "SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net." Added footnote 6 to Table 7. In Table 7, updated the note 6 to say the following: "The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency." In 8.1.1, removed the note "The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver power supply (that is, a RGMII driver powered from a 3.6 V supply driving VOH into a RGMII receiver powered from a 2.5-V supply). Tolerance for dissimilar RGMII driver and receiver supply potentials is implicit in these specifications."
10	4/2007	In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. In Table 54, "Operating Frequencies for TBGA," added column for 400 MHz. In Section 21.7, "Pull-Up Resistor Requirements," deleted last two paragraphs and after first paragraph, added a new paragraph. Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
9	3/2007	In Table 54, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (*csb_clk*)' row, changed the value in the 533 MHz column to 100–333. In Table 60, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. In Section 23, "Ordering Information," replaced first paragraph and added a note. In Section 23.1, "Part Numbers Fully Addressed by This Document," replaced first paragraph.

23 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

NOTE

The information in this document is accurate for revision 1.1 silicon and earlier. For information on revision 3.0 silicon and later versions (orderable part numbers ending with A or B), see the *MPC8347EA PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8347EAEC).

23.1 Part Numbers Fully Addressed by This Document

Table 67 shows an analysis of the Freescale part numbering nomenclature for the MPC8347E. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration parts including extended temperatures, refer to the MPC8347E product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 67. Part Numbering Nomenclature

MPC	*nnnn*	*e*	*t*	*pp*	*aa*	*a*	*r*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature[1] Range**	**Package[2]**	**Processor Frequency[3]**	**Platform Frequency**	**Revision Level**
MPC	8347	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	ZU =TBGA VV = PB free TBGA ZQ = PBGA VR = PB Free PBGA	e300 core speed AD = 266 AG = 400 AJ = 533 AL = 667	D = 266 F = 333[4]	Blank = 1.1 or 1.0

Notes:

1. For temperature range = C, processor frequency is limited to 400 (PBGA) with a platform frequency of 266 and up to 667(TBGA)with a platform frequency of 333
2. See Section 18, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. ALF marked parts support DDR1 up to 333 MHz (at 333 MHz CSB as the 'F' marking implies) and DDR2 up to 400 MHz (at 200 MHz CSB). AJF marked parts support DDR1 and DDR2 up to 333 MHz (at a CSB of 333 MHz), but DDR2 at 400 MHz (CSB at 200 MHz) is NOT guaranteed.

Table 68 shows the SVR settings by device and package type.

Table 68. SVR Settings

Device	Package	SVR (Rev. 1.0)
MPC8347E	TBGA	8052_0010
MPC8347	TBGA	8053_0010

Table 68. SVR Settings (continued)

MPC8347E	PBGA	8054_0010
MPC8347	PBGA	8055_0010

23.2 Part Marking

Parts are marked as in the example shown in Figure 44.

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA or PBGA Devices