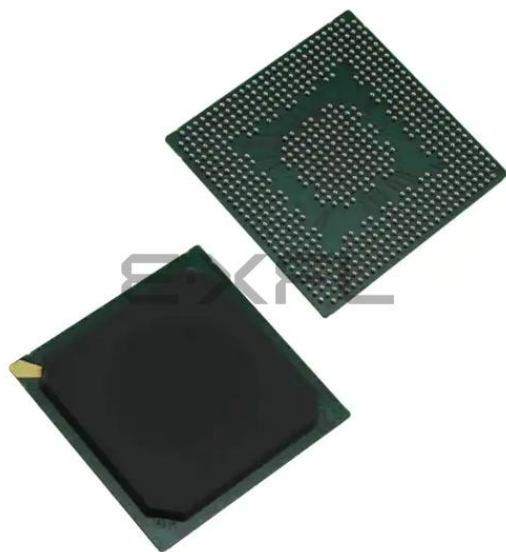




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347zqagd

- Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
- Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
- ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality
 - Complies with USB specification Rev. 2.0
 - Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints
 - Can operate as a stand-alone USB host controller
 - USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
 - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
 - Can operate as a stand-alone USB host controller
 - USB root hub with one or two downstream-facing ports

- Data chaining and direct mode
- Interrupt on completed segment and chain
- DUART
 - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
 - 52 parallel I/O pins multiplexed on various chip interfaces
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

Table 13. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	$GV_{DD} + 0.3$	V	
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz	t_{DISKEW}	—	750 1125	ps	1

Note:

- Maximum possible skew between a data strobe ($MDQS[n]$) and any corresponding bit of data ($MDQ[8n + \{0...7\}]$ if $0 \leq n \leq 7$) or ECC ($MECC[\{0...7\}]$ if $n = 8$).

Figure 4 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

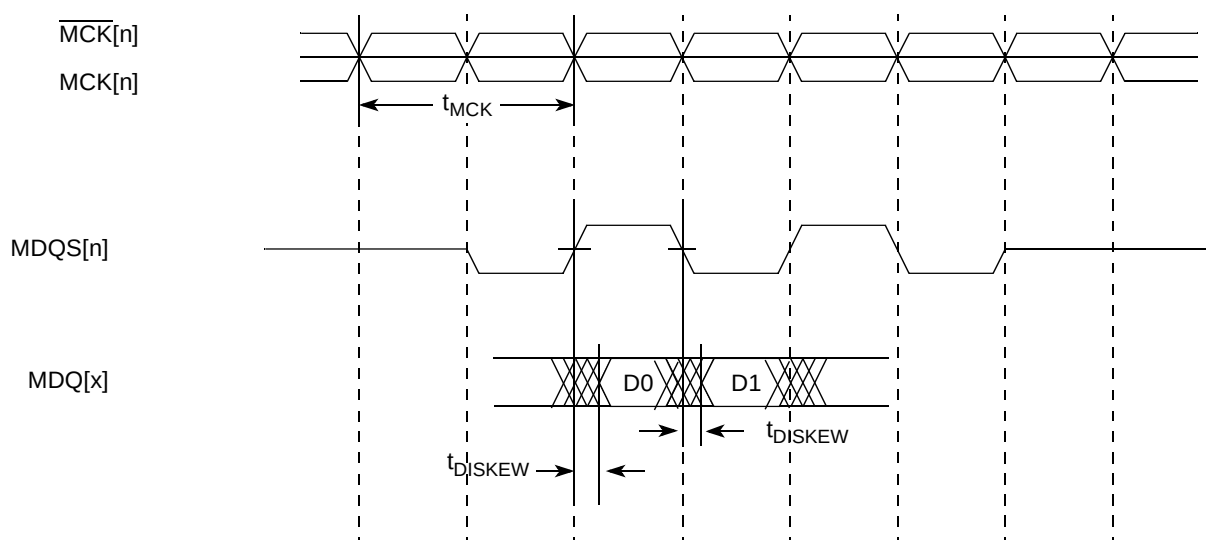


Figure 4. DDR Input Timing Diagram

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKLME}	-0.9	0.3	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKL DX}$ symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ $\overline{MCK}$ referenced measurements are made from the crossing of the two signals $\pm 0.1\text{ V}$.
- In the source synchronous mode, MCK/ $\overline{MCK}$ can be shifted in 1/4 applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
- Note that $t_{DDKHM H}$ follows the symbol conventions described in note 1. For example, $t_{DDKHM H}$ describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). $t_{DDKHM H}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*, for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8347E.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8347E. Note that $t_{DDKHM P}$ follows the symbol conventions described in note 1.

Figure 5 shows the DDR SDRAM output timing for address skew with respect to any MCK.

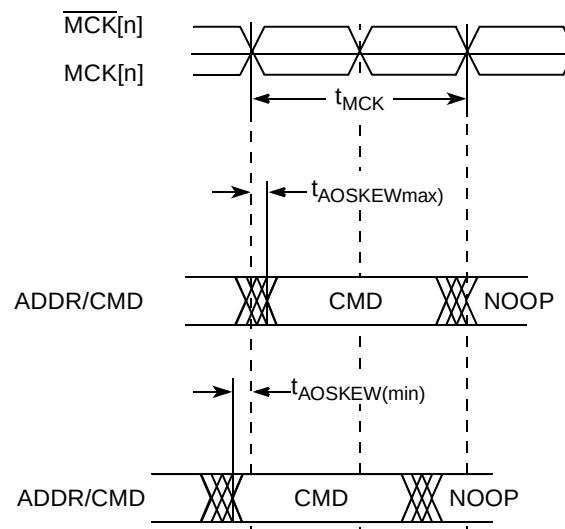
**Figure 5. Timing Diagram for t_{AOSKEW} Measurement**

Figure 6 provides the AC test load for the DDR bus.

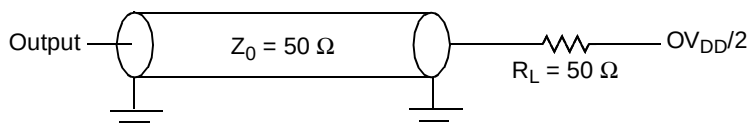


Figure 6. DDR AC Test Load

Table 15 shows the DDR SDRAM measurement conditions.

Table 15. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	$MV_{REF} \pm 0.31 V$	V	1
V_{OUT}	$0.5 \times GV_{DD}$	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Figure 7 shows the DDR SDRAM output timing diagram for source synchronous mode.

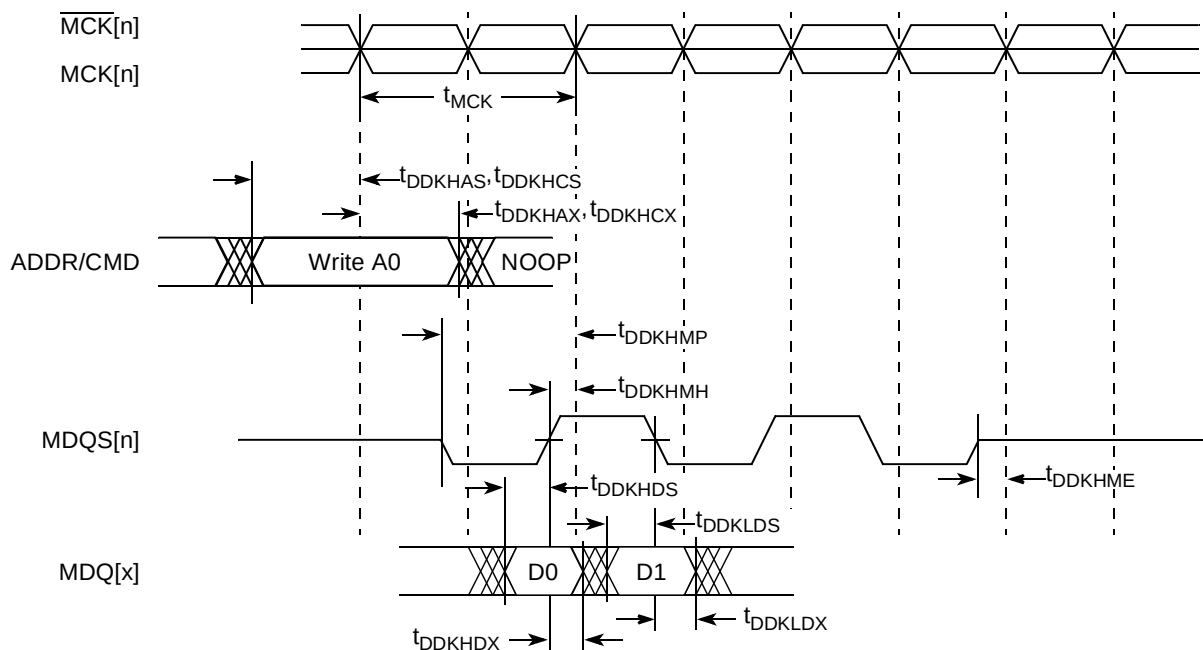


Figure 7. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

Table 16 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings, which can be useful for a system utilizing the DLL. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

Table 20. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	$\text{GND} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$LV_{DD} = \text{Min}$	1.7	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	$LV_{DD} = \text{Min}$	-0.3	0.70	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.1.1 GMII Transmit AC Timing Specifications

[Table 21](#) provides the GMII transmit AC timing specifications.

Table 21. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3 \text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK clock rise time, $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{GTXR}	—	—	1.0	ns
GTX_CLK clock fall time, $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{GTXF}	—	—	1.0	ns
GTX_CLK125 clock period	t_{G125}^2	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle measured at $LV_{DD}/2$	t_{G125H}/t_{G125}	45	—	55	%

Notes:

- The symbols for timing specifications follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This symbol represents the external GTX_CLK125 signal and does not follow the original symbol naming convention.

Figure 8 shows the GMII transmit AC timing diagram.

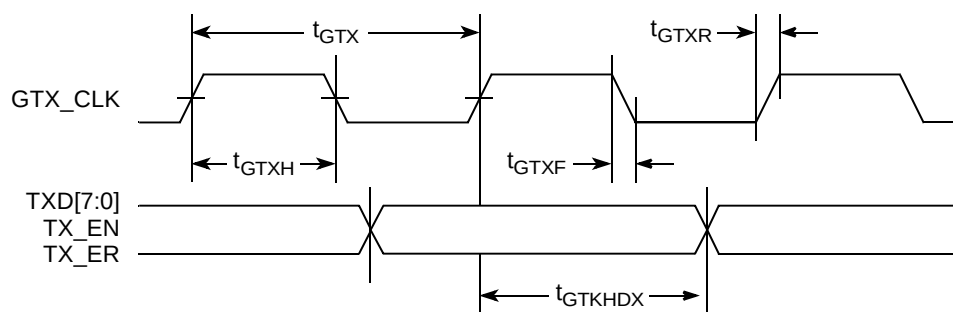


Figure 8. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 22 provides the GMII receive AC timing specifications.

Table 22. GMII Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise, $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time, $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{GRXF}	—	—	1.0	ns

Note:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 13 shows the TBI transmit AC timing diagram.

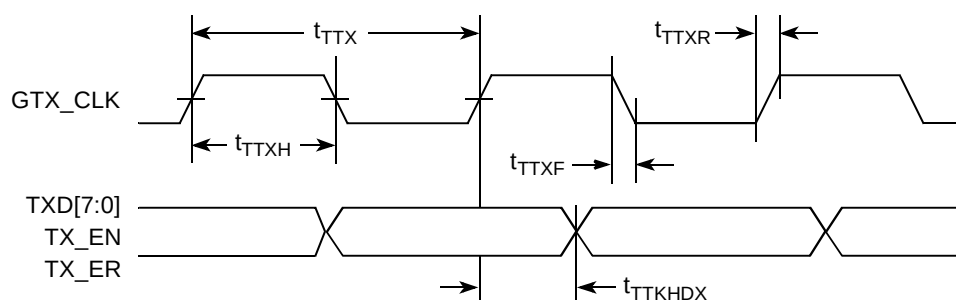


Figure 13. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 26 provides the TBI receive AC timing specifications.

Table 26. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
PMA_RX_CLK clock period	t_{TRX}		16.0		ns
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t_{TRDVKH}^2	2.5	—	—	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t_{TRDXKH}^2	1.5	—	—	ns
RX_CLK clock rise time $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{TRXF}	0.7	—	2.4	ns

Notes:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
- Setup and hold time of even numbered RCG are measured from the rising edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the rising edge of PMA_RX_CLK0.

Figure 15 shows the RBMII and RTBI AC timing and multiplexing diagrams.

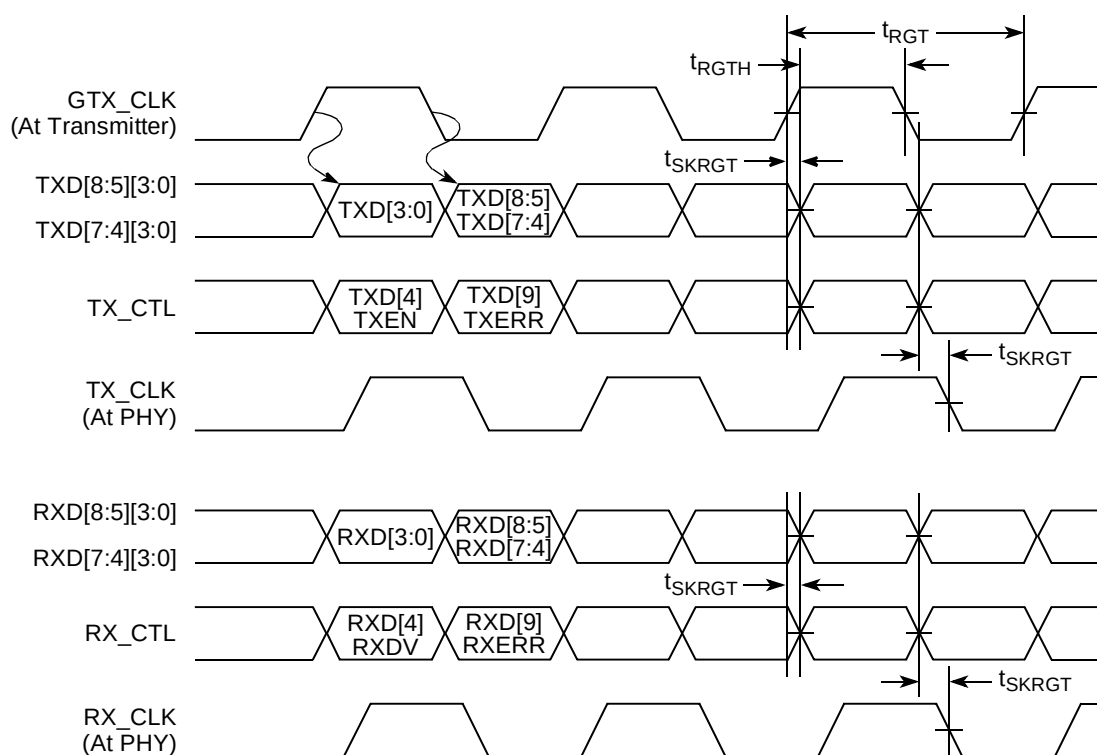


Figure 15. RGMII and RTBI AC Timing and Multiplexing Diagrams

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8347E.

10.1 Local Bus DC Electrical Characteristics

Table 33 provides the DC electrical characteristics for the local bus interface.

Table 33. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current	I_{IN}	—	± 5	μA
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V

10.2 Local Bus AC Electrical Specification

Table 34 and Table 35 describe the general timing parameters of the local bus interface of the MPC8347E.

Table 34. Local Bus General Timing Parameters—DLL On

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8347E.

12.1 I²C DC Electrical Characteristics

Table 38 provides the DC electrical characteristics for the I²C interface of the MPC8347E.

Table 38. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{2KLV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{2KHL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}(\text{max})$)	I_I	-10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8349E Integrated Host Processor Family Reference Manual*, for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 39 provides the AC timing parameters for the I²C interface of the MPC8347E. Note that all values refer to $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ levels (see Table 38).

Table 39. I²C AC Electrical Specifications

Parameter	Symbol ¹	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I ² C bus devices	t_{I2DXKL}	— 0 ²	— 0.9 ³	μs

Table 39. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μ s
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μ s
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

- The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8347E provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.
- The MPC8347E does not follow the "I²C-BUS Specifications" version 2.1 regarding the t_{I2CF} AC parameter.

Figure 31 provides the AC test load for the I²C.

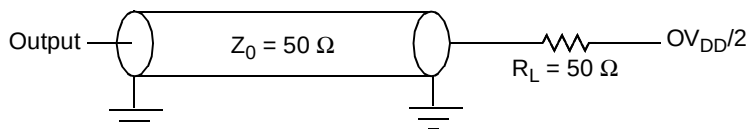
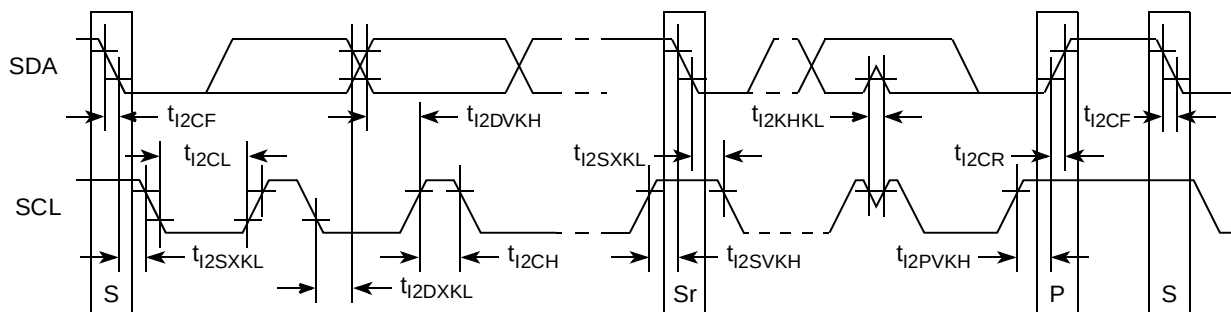
Figure 31. I²C AC Test Load

Figure 32 shows the AC timing diagram for the I²C bus.

Figure 32. I²C Bus AC Timing Diagram

18.3 Package Parameters for the MPC8347E PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.60 mm

18.5 Pinout Listings

Table 51 provides the pinout listing for the MPC8347E, 672 TBGA package.

Table 51. MPC8347E (TBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_INTA/IRQ_OUT	B34	O	OV _{DD}	2
PCI_RESET_OUT	C33	O	OV _{DD}	
PCI_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV _{DD}	
PCI_C/BE[3:0]	J30, M31, P33, T34	I/O	OV _{DD}	
PCI_PAR	P32	I/O	OV _{DD}	
PCI_FRAME	M32	I/O	OV _{DD}	5
PCI_TRDY	N29	I/O	OV _{DD}	5
PCI_IRDY	M34	I/O	OV _{DD}	5
PCI_STOP	N31	I/O	OV _{DD}	5
PCI_DEVSEL	N30	I/O	OV _{DD}	5
PCI_IDSEL	J31	I	OV _{DD}	
PCI_SERR	N34	I/O	OV _{DD}	5
PCI_PERR	N33	I/O	OV _{DD}	5
PCI_REQ[0]	D32	I/O	OV _{DD}	
PCI_REQ[1]/CPCI1_HS_ES	D34	I	OV _{DD}	
PCI_REQ[2:4]	E34, F32, G29	I	OV _{DD}	
PCI_GNT0	C34	I/O	OV _{DD}	
PCI_GNT1/CPCI1_HS_LED	D33	O	OV _{DD}	
PCI_GNT2/CPCI1_HS_ENUM	E33	O	OV _{DD}	
PCI_GNT[3:4]	F31, F33	O	OV _{DD}	
M66EN	A19	I	OV _{DD}	
DDR SDRAM Memory Interface				
MDQ[0:63]	D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8	I/O	GV _{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Gigabit Reference Clock				
EC_GTX_CLK125	C8	I	LV _{DD1}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	A17	I/O	OV _{DD}	
TSEC1_CRS/GPIO2[21]	F12	I/O	LV _{DD1}	
TSEC1_GTX_CLK	D10	O	LV _{DD1}	3
TSEC1_RX_CLK	A11	I	LV _{DD1}	
TSEC1_RX_DV	B11	I	LV _{DD1}	
TSEC1_RX_ER/GPIO2[26]	B17	I/O	OV _{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	B16, D16, E16, F16	I/O	OV _{DD}	
TSEC1_RXD[3:0]	E10, A8, F10, B8	I	LV _{DD1}	
TSEC1_TX_CLK	D17	I	OV _{DD}	
TSEC1_TXD[7:4]/GPIO2[27:30]	A15, B15, A14, B14	I/O	OV _{DD}	
TSEC1_TXD[3:0]	A10, E11, B10, A9	O	LV _{DD1}	11
TSEC1_TX_EN	B9	O	LV _{DD1}	
TSEC1_TX_ER/GPIO2[31]	A16	I/O	OV _{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	C14	I/O	OV _{DD}	
TSEC2_CRS/GPIO1[22]	D6	I/O	LV _{DD2}	
TSEC2_GTX_CLK	A4	O	LV _{DD2}	
TSEC2_RX_CLK	B4	I	LV _{DD2}	
TSEC2_RX_DV/GPIO1[23]	E6	I/O	LV _{DD2}	
TSEC2_RXD[7:4]/GPIO1[26:29]	A13, B13, C13, A12	I/O	OV _{DD}	
TSEC2_RXD[3:0]/GPIO1[13:16]	D7, A6, E8, B7	I/O	LV _{DD2}	
TSEC2_RX_ER/GPIO1[25]	D14	I/O	OV _{DD}	
TSEC2_TXD[7]/GPIO1[31]	B12	I/O	OV _{DD}	
TSEC2_TXD[6]/DR_XCVR_TERM_SEL	C12	O	OV _{DD}	
TSEC2_TXD[5]/DR_UTMI_OPMODE1	D12	O	OV _{DD}	
TSEC2_TXD[4]/DR_UTMI_OPMODE0	E12	O	OV _{DD}	
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV _{DD2}	
TSEC2_TX_ER/GPIO1[24]	F14	I/O	OV _{DD}	
TSEC2_TX_EN/GPIO1[12]	C5	I/O	LV _{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	E14	I/O	OV _{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[7:4]/GPIO2[27:30]	N28, P25, P26, P27	I/O	OV _{DD}	
TSEC1_TXD[3:0]	V28, V27, V26, W28	O	LV _{DD1}	10
TSEC1_TX_EN	W27	O	LV _{DD1}	
TSEC1_TX_ER/GPIO2[31]	N24	I/O	OV _{DD}	
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	P28	I/O	OV _{DD}	
TSEC2_CRS/GPIO1[22]	AC28	I/O	LV _{DD2}	
TSEC2_GTX_CLK	AC27	O	LV _{DD2}	
TSEC2_RX_CLK	AB25	I	LV _{DD2}	
TSEC2_RX_DV/GPIO1[23]	AC26	I/O	LV _{DD2}	
TSEC2_RXD[7:4]/GPIO1[26:29]	R28, T24, T25, T26	I/O	OV _{DD}	
TSEC2_RXD[3:0]/GPIO1[13:16]	AA25, AA26, AA27, AA28	I/O	LV _{DD2}	
TSEC2_RX_ER/GPIO1[25]	R25	I/O	OV _{DD}	
TSEC2_TXD[7]/GPIO1[31]	T27	I/O	OV _{DD}	
TSEC2_TXD[6]/DR_XCVR_TERM_SEL	T28	O	OV _{DD}	
TSEC2_TXD[5]/DR_UTMI_OPMODE1	U28	O	OV _{DD}	
TSEC2_TXD[4]/DR_UTMI_OPMODE0	U27	O	OV _{DD}	
TSEC2_TXD[3:0]/GPIO1[17:20]	AB26, AB27, AA24, AB28	I/O	LV _{DD2}	
TSEC2_TX_ER/GPIO1[24]	R27	I/O	OV _{DD}	
TSEC2_TX_EN/GPIO1[12]	AD28	I/O	LV _{DD2}	3
TSEC2_TX_CLK/GPIO1[30]	R26	I/O	OV _{DD}	
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	B4, A4	O	OV _{DD}	
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	D5, C5	I/O	OV _{DD}	
UART_CTS[1]/MSRCID4/LSRCID4	B5	I/O	OV _{DD}	
UART_CTS[2]/MDVAL/LDVAL	A5	I/O	OV _{DD}	
UART_RTS[1:2]	D6, C6	O	OV _{DD}	
I²C interface				
IIC1_SDA	E5	I/O	OV _{DD}	2
IIC1_SCL	A6	I/O	OV _{DD}	2
IIC2_SDA	B6	I/O	OV _{DD}	2
IIC2_SCL	E7	I/O	OV _{DD}	2
SPI				
SPIMOSI	D7	I/O	OV _{DD}	

Table 60. Suggested PLL Configurations

Ref No. ¹	RCWL		400 MHz Device			533 MHz Device			667 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)
33 MHz CLKIN/PCI_CLK Options											
922	1001	0100010	—	—	—	—	—	f300	33	300	300
723	0111	0100011	33	233	350	33	233	350	33	233	350
604	0110	0000100	33	200	400	33	200	400	33	200	400
624	0110	0100100	33	200	400	33	200	400	33	200	400
803	1000	0000011	33	266	400	33	266	400	33	266	400
823	1000	0100011	33	266	400	33	266	400	33	266	400
903	1001	0000011	—			33	300	450	33	300	450
923	1001	0100011	—			33	300	450	33	300	450
704	0111	0000011	—			33	233	466	33	233	466
724	0111	0100011	—			33	233	466	33	233	466
A03	1010	0000011	—			33	333	500	33	333	500
804	1000	0000100	—			33	266	533	33	266	533
705	0111	0000101	—			—			33	233	583
606	0110	0000110	—			—			33	200	600
904	1001	0000100	—			—			33	300	600
805	1000	0000101	—			—			33	266	667
A04	1010	0000100	—			—			33	333	667
66 MHz CLKIN/PCI_CLK Options											
304	0011	0000100	66	200	400	66	200	400	66	200	400
324	0011	0100100	66	200	400	66	200	400	66	200	400
403	0100	0000011	66	266	400	66	266	400	66	266	400
423	0100	0100011	66	266	400	66	266	400	66	266	400
305	0011	0000101	—			66	200	500	66	200	500
503	0101	0000011	—			66	333	500	66	333	500
404	0100	0000100	—			66	266	533	66	266	533
306	0011	0000110	—			—			66	200	600
405	0100	0000101	—			—			66	266	667
504	0101	0000100	—			—			66	333	667

¹ The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

² The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

Table 62. Package Thermal Characteristics for PBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{\theta JC}$	5	°C/W	5
Junction-to-package natural convection on top	Ψ_{JT}	5	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For

Table 64. Heat Sink and Thermal Resistance of MPC8347E (PBGA) (continued)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	8.8
AAVID 31 × 35 × 23 mm pin fin	Natural convection	11.3
AAVID 31 × 35 × 23 mm pin fin	1 m/s	8.1
AAVID 31 × 35 × 23 mm pin fin	2 m/s	7.5
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	9.1
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	7.1
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	6.5
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	10.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	7.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	6.6
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	6.9

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770

Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally