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**Applications of Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

## Details

| | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 533MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 672-LBGA |
| Supplier Device Package | 672-LBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347zuajd |

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8347E.

## 4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8347E.

**Table 6. CLKIN DC Timing Specifications**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.7 | $OV_{DD} + 0.3$ | V |
| Input low voltage | — | $V_{IL}$ | −0.3 | 0.4 | V |
| CLKIN input current | $0\ V \leq V_{IN} \leq OV_{DD}$ | $I_{IN}$ | — | ±10 | μA |
| PCI_SYNC_IN input current | $0\ V \leq V_{IN} \leq 0.5\ V$ or $OV_{DD} - 0.5\ V \leq V_{IN} \leq OV_{DD}$ | $I_{IN}$ | — | ±10 | μA |
| PCI_SYNC_IN input current | $0.5\ V \leq V_{IN} \leq OV_{DD} - 0.5\ V$ | $I_{IN}$ | — | ±50 | μA |

## 4.2 AC Electrical Characteristics

The primary clock source for the MPC8347E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8347E.

**Table 7. CLKIN AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| CLKIN/PCI_CLK frequency | $f_{CLKIN}$ | — | — | 66 | MHz | 1, 6 |
| CLKIN/PCI_CLK cycle time | $t_{CLKIN}$ | 15 | — | — | ns | — |
| CLKIN/PCI_CLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 2.3 | ns | 2 |
| CLKIN/PCI_CLK duty cycle | $t_{KHK}/t_{CLKIN}$ | 40 | — | 60 | % | 3 |
| CLKIN/PCI_CLK jitter | — | — | — | ±150 | ps | 4, 5 |

**Notes:**

1. **Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at −20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency.

### Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with $GV_{DD}$ of 2.5 V ± 5%.

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MDQS epilogue end | $t_{DDKLME}$ | -0.9 | 0.3 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2. All MCK/$\overline{MCK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.

3. In the source synchronous mode, MCK/$\overline{MCK}$ can be shifted in 1/4 applied cycle increments through the clock control register. For the skew measurements referenced for $t_{AOSKEW}$ it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.

4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

5. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*, for a description and understanding of the timing modifications enabled by use of these bits.

6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8347E.

7. All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8347E. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.

Figure 5 shows the DDR SDRAM output timing for address skew with respect to any MCK.
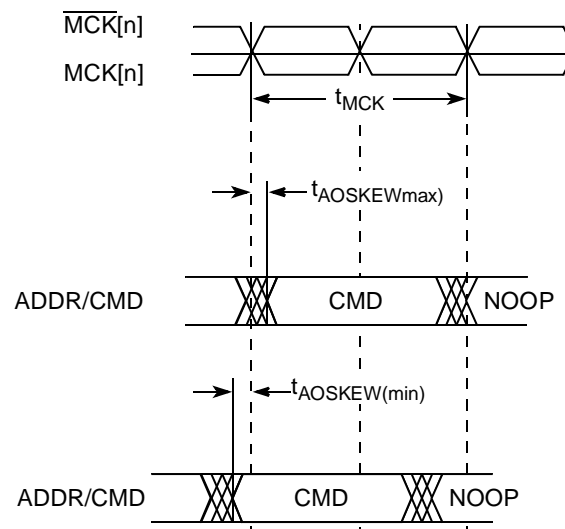


**Figure 5. Timing Diagram for $t_{AOSKEW}$ Measurement**

Figure 6 provides the AC test load for the DDR bus.

**Table 34. Local Bus General Timing Parameters—DLL On (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 1 | — | ns | 3 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ}$ | — | 3.8 | ns | 8 |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to the rising edge of LSYNC_IN.

3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.

4. Input timings are measured at the pin.

5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.

6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.

7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.

8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

**Table 35. Local Bus General Timing Parameters—DLL Bypass[9]**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 15 | — | ns | 2 |
| Input setup to local bus clock | $t_{LBIVKH}$ | 7 | — | ns | 3, 4 |
| Input hold from local bus clock | $t_{LBIXKH}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |
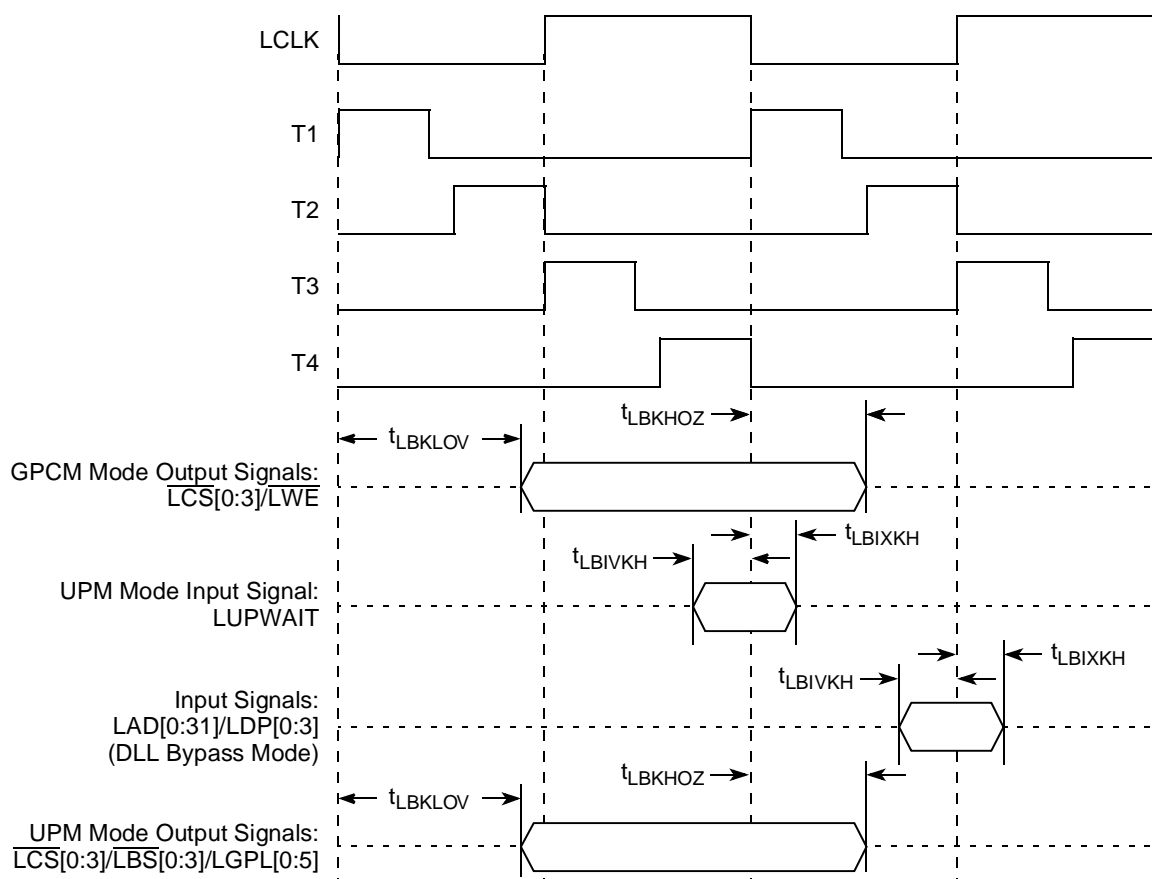
**Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)**

# 11  JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E

## 11.1  JTAG DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E.

**Table 36. JTAG interface DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | | $OV_{DD} - 0.3$ | $OV_{DD} + 0.3$ | V |
| Input low voltage | $V_{IL}$ | | −0.3 | 0.8 | V |
| Input current | $I_{IN}$ | | | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH} = -8.0$ mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL} = 8.0$ mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL} = 3.2$ mA | — | 0.4 | V |

## 11.2  JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E. Table 37 provides the JTAG AC timing specifications as defined in Figure 27 through Figure 30.

**Table 37. JTAG AC Timing Specifications (Independent of CLKIN)[1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | |
| JTAG external clock rise and fall times | $t_{JTGR}$, $t_{JTGF}$ | 0 | 2 | ns | |
| $\overline{TRST}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times: <br> Boundary-scan data <br> TMS, TDI | <br> $t_{JTDVKH}$ <br> $t_{JTIVKH}$ | <br> 4 <br> 4 | ns <br> — <br> — | | 4 |
| Input hold times: <br> Boundary-scan data <br> TMS, TDI | <br> $t_{JTDXKH}$ <br> $t_{JTIXKH}$ | <br> 10 <br> 10 | ns <br> — <br> — | | 4 |
| Valid times: <br> Boundary-scan data <br> TDO | <br> $t_{JTKLDV}$ <br> $t_{JTKLOV}$ | <br> 2 <br> 2 | ns <br> 11 <br> 11 | | 5 |

**Table 41. PCI AC Timing Specifications at 66 MHz[1] (continued)**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 3, 5 |

**Notes:**

1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.

2. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.

3. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.

4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

5. Input timings are measured at the pin.

Table 42 provides the PCI AC timing specifications at 33 MHz.

**Table 42. PCI AC Timing Specifications at 33 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 11 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 2 | — | ns | 2 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 2, 3 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 2, 4 |
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 2, 4 |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.

2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.

3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4. Input timings are measured at the pin.
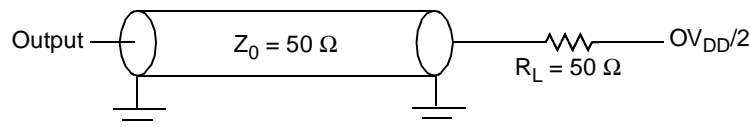
Figure 33 provides the AC test load for PCI.



**Figure 33. PCI AC Test Load**
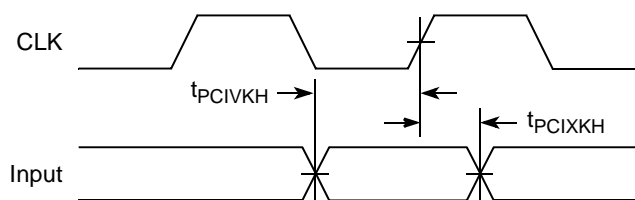
Figure 34 shows the PCI input AC timing diagram.



**Figure 34. PCI Input AC Timing Diagram**
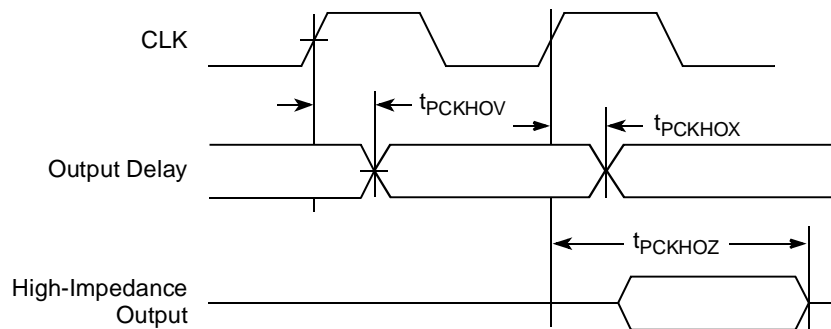
Figure 35 shows the PCI output AC timing diagram.



**Figure 35. PCI Output AC Timing Diagram**

# 15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

## 15.1 GPIO DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the MPC8347E GPIO.

**Table 45. GPIO DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | | −0.3 | 0.8 | V |
| Input current | $I_{IN}$ | | | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = −8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

## 15.2 GPIO AC Timing Specifications

Table 46 provides the GPIO input and output AC timing specifications.

**Table 46. GPIO Input AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Unit |
|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns |

**Notes:**
1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least $t_{PIWID}$ ns to ensure proper operation.
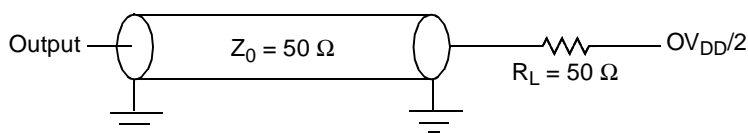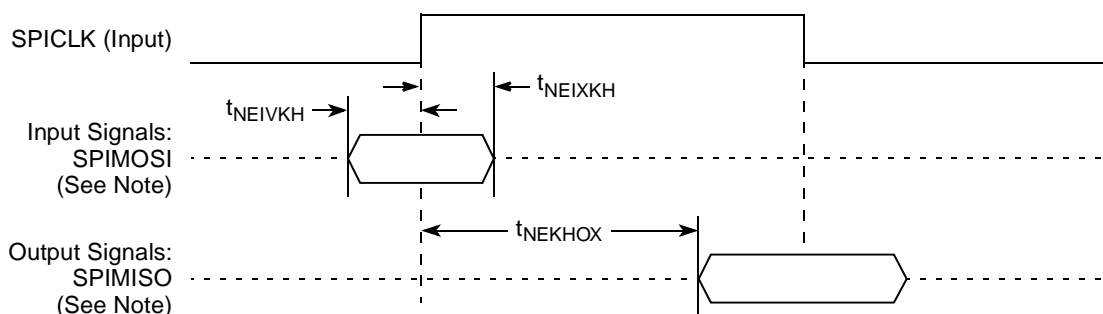
Figure 36 provides the AC test load for the SPI.



**Figure 36. SPI AC Test Load**

Figure 37 and Figure 38 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.
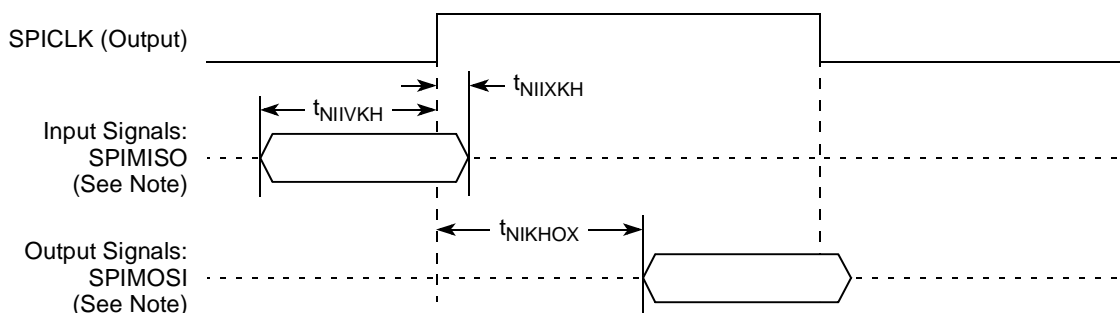
Figure 37 shows the SPI timings in slave mode (external clock).



**Note:** The clock edge is selectable on SPI.

**Figure 37. SPI AC Timing in Slave Mode (External Clock) Diagram**

Figure 38 shows the SPI timings in master mode (internal clock).



**Note:** The clock edge is selectable on SPI.

**Figure 38. SPI AC Timing in Master Mode (Internal Clock) Diagram**

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | C8 | I | $LV_{DD1}$ | |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_COL/GPIO2[20] | A17 | I/O | $OV_{DD}$ | |
| TSEC1_CRS/GPIO2[21] | F12 | I/O | $LV_{DD1}$ | |
| TSEC1_GTX_CLK | D10 | O | $LV_{DD1}$ | 3 |
| TSEC1_RX_CLK | A11 | I | $LV_{DD1}$ | |
| TSEC1_RX_DV | B11 | I | $LV_{DD1}$ | |
| TSEC1_RX_ER/GPIO2[26] | B17 | I/O | $OV_{DD}$ | |
| TSEC1_RXD[7:4]/GPIO2[22:25] | B16, D16, E16, F16 | I/O | $OV_{DD}$ | |
| TSEC1_RXD[3:0] | E10, A8, F10, B8 | I | $LV_{DD1}$ | |
| TSEC1_TX_CLK | D17 | I | $OV_{DD}$ | |
| TSEC1_TXD[7:4]/GPIO2[27:30] | A15, B15, A14, B14 | I/O | $OV_{DD}$ | |
| TSEC1_TXD[3:0] | A10, E11, B10, A9 | O | $LV_{DD1}$ | 11 |
| TSEC1_TX_EN | B9 | O | $LV_{DD1}$ | |
| TSEC1_TX_ER/GPIO2[31] | A16 | I/O | $OV_{DD}$ | |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 2)** | | | | |
| TSEC2_COL/GPIO1[21] | C14 | I/O | $OV_{DD}$ | |
| TSEC2_CRS/GPIO1[22] | D6 | I/O | $LV_{DD2}$ | |
| TSEC2_GTX_CLK | A4 | O | $LV_{DD2}$ | |
| TSEC2_RX_CLK | B4 | I | $LV_{DD2}$ | |
| TSEC2_RX_DV/GPIO1[23] | E6 | I/O | $LV_{DD2}$ | |
| TSEC2_RXD[7:4]/GPIO1[26:29] | A13, B13, C13, A12 | I/O | $OV_{DD}$ | |
| TSEC2_RXD[3:0]/GPIO1[13:16] | D7, A6, E8, B7 | I/O | $LV_{DD2}$ | |
| TSEC2_RX_ER/GPIO1[25] | D14 | I/O | $OV_{DD}$ | |
| TSEC2_TXD[7]/GPIO1[31] | B12 | I/O | $OV_{DD}$ | |
| TSEC2_TXD[6]/DR_XCVR_TERM_SEL | C12 | O | $OV_{DD}$ | |
| TSEC2_TXD[5]/DR_UTMI_OPMODE1 | D12 | O | $OV_{DD}$ | |
| TSEC2_TXD[4]/DR_UTMI_OPMODE0 | E12 | O | $OV_{DD}$ | |
| TSEC2_TXD[3:0]/GPIO1[17:20] | B5, A5, F8, B6 | I/O | $LV_{DD2}$ | |
| TSEC2_TX_ER/GPIO1[24] | F14 | I/O | $OV_{DD}$ | |
| TSEC2_TX_EN/GPIO1[12] | C5 | I/O | $LV_{DD2}$ | 3 |
| TSEC2_TX_CLK/GPIO1[30] | E14 | I/O | $OV_{DD}$ | |

**Table 51. MPC8347E (TBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **System Control** | | | | |
| $\overline{PORESET}$ | C18 | I | $OV_{DD}$ | |
| $\overline{HRESET}$ | B18 | I/O | $OV_{DD}$ | 1 |
| $\overline{SRESET}$ | D18 | I/O | $OV_{DD}$ | 2 |
| **Thermal Management** | | | | |
| THERM0 | K32 | I | — | 9 |
| **Power and Ground Signals** | | | | |
| $AV_{DD}1$ | L31 | Power for e300 PLL (1.2 V) | $AV_{DD}1$ | |
| $AV_{DD}2$ | AP12 | Power for system PLL (1.2 V) | $AV_{DD}2$ | |
| $AV_{DD}3$ | AE1 | Power for DDR DLL (1.2 V) | $AV_{DD}3$ | |
| $AV_{DD}4$ | AJ13 | Power for LBIU DLL (1.2 V) | $AV_{DD}4$ | |
| GND | A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34 | — | — | |
| $GV_{DD}$ | A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6 | Power for DDR DRAM I/O voltage (2.5 V) | $GV_{DD}$ | |
| $LV_{DD}1$ | C9, D11 | Power for three-speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V) | $LV_{DD}1$ | |

**Table 52. MPC8347E (PBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| SPIMISO | C7 | I/O | $OV_{DD}$ | |
| SPICLK | B7 | I/O | $OV_{DD}$ | |
| SPISEL | A7 | I | $OV_{DD}$ | |
| **Clocks** | | | | |
| PCI_CLK_OUT[0:2] | Y1, W3, W2 | O | $OV_{DD}$ | |
| PCI_CLK_OUT[3]/$\overline{LCS}$[6] | W1 | O | $OV_{DD}$ | |
| PCI_CLK_OUT[4]/$\overline{LCS}$[7] | V3 | O | $OV_{DD}$ | |
| PCI_SYNC_IN/PCI_CLOCK | U4 | I | $OV_{DD}$ | |
| PCI_SYNC_OUT | U5 | O | $OV_{DD}$ | 3 |
| RTC/PIT_CLOCK | E9 | I | $OV_{DD}$ | |
| CLKIN | W5 | I | $OV_{DD}$ | |
| **JTAG** | | | | |
| TCK | H27 | I | $OV_{DD}$ | |
| TDI | H28 | I | $OV_{DD}$ | 4 |
| TDO | M24 | O | $OV_{DD}$ | 3 |
| TMS | J27 | I | $OV_{DD}$ | 4 |
| $\overline{TRST}$ | K26 | I | $OV_{DD}$ | 4 |
| **Test** | | | | |
| TEST | F28 | I | $OV_{DD}$ | 6 |
| TEST_SEL | T3 | I | $OV_{DD}$ | 6 |
| **PMC** | | | | |
| $\overline{QUIESCE}$ | K27 | O | $OV_{DD}$ | |
| **System Control** | | | | |
| $\overline{PORESET}$ | K28 | I | $OV_{DD}$ | |
| $\overline{HRESET}$ | M25 | I/O | $OV_{DD}$ | 1 |
| $\overline{SRESET}$ | L27 | I/O | $OV_{DD}$ | 2 |
| **Thermal Management** | | | | |
| THERM0 | B15 | I | — | 8 |
| **Power and Ground Signals** | | | | |
| $AV_{DD}1$ | C15 | Power for e300 PLL (1.2 V) | $AV_{DD}1$ | |
| $AV_{DD}2$ | U1 | Power for system PLL (1.2 V) | $AV_{DD}2$ | |

As shown in Figure 41, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349E Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + RCWL[DDRCM])$$

*ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{MCK}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + RCWL[LBIUCM])$$

*lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 53 specifies which units have a configurable clock frequency.

**Table 53. Configurable Clock Units**

| Unit | Default Frequency | Options |
|------|-------------------|---------|
| TSEC1 | *csb_clk/3* | Off, *csb_clk, csb_clk/2, csb_clk/3* |
| TSEC2, I$^2$C1 | *csb_clk/3* | Off, *csb_clk, csb_clk/2, csb_clk/3* |
| Security core | *csb_clk/3* | Off, *csb_clk,* csb_clk/2, *csb_clk/3* |
| USB DR, USB MPH | *csb_clk/3* | Off, csb_clk, csb_clk/2, *csb_clk/3* |
| PCI and DMA complex | *csb_clk* | Off, *csb_clk* |

Table 54 provides the operating frequencies for the MPC8347E TBGA under recommended operating conditions (see Table 2).

**Table 54. Operating Frequencies for TBGA**

| Characteristic[1] | 400 MHz | 533 MHz | 667 MHz | Unit |
|---|---|---|---|---|
| e300 core frequency (*core_clk*) | 266–400 | 266–533 | 266–667 | MHz |
| Coherent system bus frequency (*csb_clk*) | 100–266 | 100–266 | 100–333 | MHz |
| DDR and memory bus frequency (MCLK)[2] | 100–133 | 100–133 | 100–166.67 | MHz |
| Local bus frequency (LCLK*n*)[3] | 16.67–133 | 16.67–133 | 16.67–133 | MHz |
| PCI input frequency (CLKIN or PCI_CLK) | 25–66 | 25–66 | 25–66 | MHz |
| Security core maximum internal operating frequency | 133 | 133 | 166 | MHz |
| USB_DR, USB_MPH maximum internal operating frequency | 133 | 133 | 166 | MHz |

[1] The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

[2] The DDR data rate is 2x the DDR memory bus frequency.

[3] The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

Table 55 provides the operating frequencies for the MPC8347E PBGA under recommended operating conditions.

**Table 55. Operating Frequencies for PBGA**

| Characteristic[1] | 266 MHz | 333 MHz | 400 MHz | Unit |
|---|---|---|---|---|
| e300 core frequency (*core_clk*) | 200–266 | 200–333 | 200–400 | MHz |
| Coherent system bus frequency (*csb_clk*) | 100–266 | | | MHz |
| Local bus frequency (LCLK*n*)[2] | 16.67–133 | | | MHz |
| PCI input frequency (CLKIN or PCI_CLK) | 25–66 | | | MHz |
| Security core maximum internal operating frequency | 133 | | | MHz |
| USB_DR, USB_MPH maximum internal operating frequency | 133 | | | MHz |

[1] The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

[2] The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

# 19.1   System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 56 shows the multiplication factor encodings for the system PLL.

**Table 56. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|:---:|:---:|
| 0000 | × 16 |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |
| 0111 | × 7 |
| 1000 | × 8 |
| 1001 | × 9 |
| 1010 | × 10 |
| 1011 | × 11 |
| 1100 | × 12 |
| 1101 | × 13 |
| 1110 | × 14 |
| 1111 | × 15 |

As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 57 and Table 58 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

**Table 57. CSB Frequency Options for Host Mode**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0010 | 2 : 1 | | | | 133 |
| Low | 0011 | 3 : 1 | | | 100 | 200 |
| Low | 0100 | 4 : 1 | | 100 | 133 | 266 |
| Low | 0101 | 5 : 1 | | 125 | 166 | 333 |
| Low | 0110 | 6 : 1 | 100 | 150 | 200 | |
| Low | 0111 | 7 : 1 | 116 | 175 | 233 | |
| Low | 1000 | 8 : 1 | 133 | 200 | 266 | |
| Low | 1001 | 9 : 1 | 150 | 225 | 300 | |
| Low | 1010 | 10 : 1 | 166 | 250 | 333 | |
| Low | 1011 | 11 : 1 | 183 | 275 | | |
| Low | 1100 | 12 : 1 | 200 | 300 | | |
| Low | 1101 | 13 : 1 | 216 | 325 | | |
| Low | 1110 | 14 : 1 | 233 | | | |
| Low | 1111 | 15 : 1 | 250 | | | |
| Low | 0000 | 16 : 1 | 266 | | | |
| High | 0010 | 2 : 1 | | | | 133 |
| High | 0011 | 3 : 1 | | | 100 | 200 |
| High | 0100 | 4 : 1 | | | 133 | 266 |
| High | 0101 | 5 : 1 | | | 166 | 333 |
| High | 0110 | 6 : 1 | | | 200 | |
| High | 0111 | 7 : 1 | | | 233 | |
| High | 1000 | 8 : 1 | | | | |

[1] CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

[2] CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 63 and Table 64 show heat sink thermal resistance for TBGA and PBGA of the MPC8347E.

**Table 63. Heat Sink and Thermal Resistance of MPC8347E (TBGA)**

| Heat Sink Assuming Thermal Grease | Air Flow | 35 × 35 mm TBGA |
|---|---|---|
| | | Thermal Resistance |
| AAVID 30 × 30 × 9.4 mm pin fin | Natural convection | 10 |
| AAVID 30 × 30 × 9.4 mm pin fin | 1 m/s | 6.5 |
| AAVID 30 × 30 × 9.4 mm pin fin | 2 m/s | 5.6 |
| AAVID 31 × 35 × 23 mm pin fin | Natural convection | 8.4 |
| AAVID 31 × 35 × 23 mm pin fin | 1 m/s | 4.7 |
| AAVID 31 × 35 × 23 mm pin fin | 2 m/s | 4 |
| Wakefield, 53 × 53 × 25 mm pin fin | Natural convection | 5.7 |
| Wakefield, 53 × 53 × 25 mm pin fin | 1 m/s | 3.5 |
| Wakefield, 53 × 53 × 25 mm pin fin | 2 m/s | 2.7 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | Natural convection | 6.7 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 1 m/s | 4.1 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 2 m/s | 2.8 |
| MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass | 1 m/s | 3.1 |

**Table 64. Heat Sink and Thermal Resistance of MPC8347E (PBGA)**

| Heat Sink Assuming Thermal Grease | Air Flow | 29 × 29 mm PBGA |
|---|---|---|
| | | Thermal Resistance |
| AAVID 30 × 30 × 9.4 mm pin fin | Natural convection | 13.5 |
| AAVID 30 × 30 × 9.4 mm pin fin | 1 m/s | 9.6 |

Tyco Electronics                                    800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering                               603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc.                                     781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation                             800-248-2481
Dow-Corning Electronic Materials
P.O. Box 994
Midland, MI 48686-0997
Internet: www.dowcorning.com

Shin-Etsu MicroSi, Inc.                             888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company                               800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

## 20.3   Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

### 20.3.1   Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally
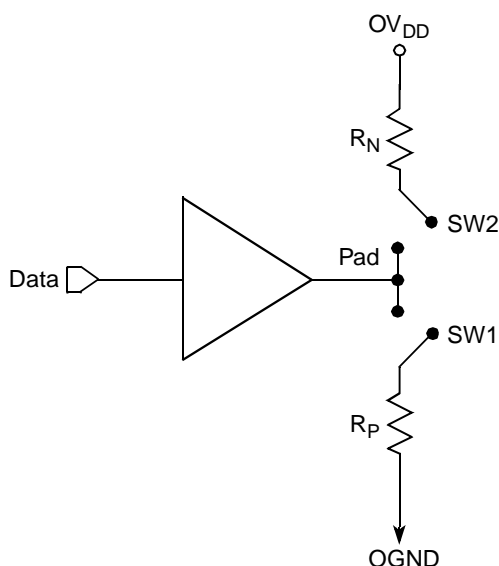
**Figure 43. Driver Impedance Measurement**

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value $R_{term}$. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 65. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI Signals (Not Including PCI Output Clocks) | PCI Output Clocks (Including PCI_SYNC_OUT) | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|---|
| $R_N$ | 42 Target | 25 Target | 42 Target | 20 Target | $Z_0$ | Ω |
| $R_P$ | 42 Target | 25 Target | 42 Target | 20 Target | $Z_0$ | Ω |
| Differential | NA | NA | NA | NA | $Z_{DIFF}$ | Ω |

**Note:** Nominal supply voltages. See Table 1, $T_j$ = 105°C.

## 21.6  Configuration Pin Multiplexing

The MPC8347E power-on configuration options can be set through external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see the customer-visible configuration pins). These pins are used as output only pins in normal operation.

However, while $\overline{\text{HRESET}}$ is asserted, these pins are treated as inputs, and the value on these pins is latched when $\overline{\text{PORESET}}$ deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with

**Table 66. Document Revision History (continued)**

| Revision | Date | Substantive Change(s) |
|----------|------|----------------------|
| 8 | 2/2007 | Page 1, updated first paragraph to reflect PowerQUICC II information. Updated note after second paragraph.<br>In the features list in Section 1, "Overview," corrected DDR data rate to show:<br>• 266 MHz for PBGA parts for all silicon revisions<br>• 333 MHz for DDR for TBGA parts for silicon Rev. 1.x<br>In Table 5, "MPC8347E Typical I/O Power Dissipation," added $GV_{DD}$ 1.8-V values for DDR2; added table footnote to designate rates that apply only to the TBGA package.<br>In Figure 43, "JTAG Interface Connection," updated with new figure.<br>In Section 23, "Ordering Information," replicated note from document introduction.<br>In Section 23.1, "Part Numbers Fully Addressed by This Document," replaced third sentence of first paragraph directing customer to product summary page for available frequency configuration parts.<br>Updated back page information. |
| 7 | 8/2006 | Changed all references to revision 2.0 silicon to revision 3.0 silicon.<br>Changed $V_{IH}$ minimum value in Table 36, "JTAG Interface DC Electrical Characteristics," to $OV_{DD} - 0.3$.<br>In Table 60, "Suggested PLL Configurations," deleted reference-number rows 902 and 703. |
| 6 | 3/2006 | Section 2, "Electrical Characteristics," moved to second section and all other section, table, and figure numbering change accordingly.<br>Table 7, "CLKIN AC Timing Specifications:" Changed max rise and fall time from 1.2 to 2.3.<br>Table 22, "GMII Receive AC Timing Specifications:" Changed min $t_{TTKHDX}$ from 0.5 to 1.0.<br>Table 30, "MII Management AC Timing Specifications:" Changed max value of $t_{MDKHDX}$ from 70 to 170.<br>Table 34, "Local Bus General Timing Parameters—DLL on:" Changed min $t_{LBIVKH2}$ from 1.7 to 2.2.<br>Table 36, "JTAG interface DC Electrical Characteristics:" Changed $V_{IH}$ input high voltage min to 2.0.<br>Table 54, "Operating Frequencies for TBGA:"<br>• Updated TBD values.<br>• Changed maximum coherent system bus frequency for TBGA 667-MHz device to 333 MHz.<br>Table 55, "Operating Frequencies for PBGA:"<br>• Updated TBD values.<br>• Changed PBGA maximum coherent system bus frequency to 266 MHz, and maximum DDR memory bus frequency to 133 MHz.<br>Table 60, "Suggested PLL Configurations": Removed some values from suggested PLL configurations for reference numbers 902, 922, 903, and 923.<br>Table 67, "Part Numbering Nomenclature": Updated TBD values in note 1.<br>Added Table 68, "SVR Settings."<br>Added Section 23.2, "Part Marking." |
| 5 | 10/2005 | In Table 57, updated AAVID 30x30x9.4 mm Pin Fin (natural convection) junction-to-ambient thermal resistance, from 11 to 10. |
| 4 | 9/2005 | Added Table 2, "MPC8347E Typical I/O Power Dissipation." |
| 3 | 8/2005 | Table 1: Updated values for power dissipation that were TBD in Revision 2. |
| 2 | 5/2005 | Table 1: Typical values for power dissipation are changed to TBD.<br>Table 48: Footnote numbering was wrong. THERM0 should have footnote 9 instead of 8. |