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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I ² S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151ret6tr

Contents

1	Introduction	9
2	Description	10
2.1	Device overview	11
2.2	Ultra-low-power device continuum	12
2.2.1	Performance	12
2.2.2	Shared peripherals	12
2.2.3	Common system strategy	12
2.2.4	Features	12
3	Functional overview	13
3.1	Low-power modes	14
3.2	ARM® Cortex®-M3 core with MPU	18
3.3	Reset and supply management	19
3.3.1	Power supply schemes	19
3.3.2	Power supply supervisor	19
3.3.3	Voltage regulator	20
3.3.4	Boot modes	20
3.4	Clock management	21
3.5	Low-power real-time clock and backup registers	23
3.6	GPIOs (general-purpose inputs/outputs)	23
3.7	Memories	24
3.8	DMA (direct memory access)	24
3.9	LCD (liquid crystal display)	25
3.10	ADC (analog-to-digital converter)	25
3.10.1	Temperature sensor	25
3.10.2	Internal voltage reference (V_{REFINT})	26
3.11	DAC (digital-to-analog converter)	26
3.12	Operational amplifier	26
3.13	Ultra-low-power comparators and reference voltage	27
3.14	System configuration controller and routing interface	27
3.15	Touch sensing	27

3.16	Timers and watchdogs	28
3.16.1	General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)	28
3.16.2	Basic timers (TIM6 and TIM7)	29
3.16.3	SysTick timer	29
3.16.4	Independent watchdog (IWDG)	29
3.16.5	Window watchdog (WWDG)	29
3.17	Communication interfaces	29
3.17.1	I ² C bus	29
3.17.2	Universal synchronous/asynchronous receiver transmitter (USART)	29
3.17.3	Serial peripheral interface (SPI)	30
3.17.4	Inter-integrated sound (I2S)	30
3.17.5	Universal serial bus (USB)	30
3.18	CRC (cyclic redundancy check) calculation unit	30
3.19	Development support	31
3.19.1	Serial wire JTAG debug port (SWJ-DP)	31
3.19.2	Embedded Trace Macrocell™	31
4	Pin descriptions	32
5	Memory mapping	55
6	Electrical characteristics	56
6.1	Parameter conditions	56
6.1.1	Minimum and maximum values	56
6.1.2	Typical values	56
6.1.3	Typical curves	56
6.1.4	Loading capacitor	56
6.1.5	Pin input voltage	56
6.1.6	Power supply scheme	57
6.1.7	Optional LCD power supply scheme	58
6.1.8	Current consumption measurement	58
6.2	Absolute maximum ratings	59
6.3	Operating conditions	60
6.3.1	General operating conditions	60
6.3.2	Embedded reset and power control block characteristics	61
6.3.3	Embedded internal reference voltage	63

6.3.4	Supply current characteristics	64
6.3.5	Wakeup time from low-power mode	75
6.3.6	External clock source characteristics	76
6.3.7	Internal clock source characteristics	81
6.3.8	PLL characteristics	84
6.3.9	Memory characteristics	84
6.3.10	EMC characteristics	86
6.3.11	Electrical sensitivity characteristics	87
6.3.12	I/O current injection characteristics	88
6.3.13	I/O port characteristics	89
6.3.14	NRST pin characteristics	92
6.3.15	TIM timer characteristics	93
6.3.16	Communications interfaces	94
6.3.17	12-bit ADC characteristics	102
6.3.18	DAC electrical specifications	107
6.3.19	Operational amplifier characteristics	109
6.3.20	Temperature sensor characteristics	111
6.3.21	Comparator	111
6.3.22	LCD controller	113
7	Package information	114
7.1	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package information	114
7.2	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information	117
7.3	LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package information	120
7.4	UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package information	123
7.5	WLCSP104, 0.4 mm pitch wafer level chip scale package information	126
7.6	Thermal characteristics	129
7.6.1	Reference document	130
8	Part numbering	131
9	Revision History	132

List of figures

Figure 1.	Ultra-low-power STM32L151xE and STM32L152xE block diagram.	13
Figure 2.	Clock tree	22
Figure 3.	STM32L15xZE LQFP144 pinout.	32
Figure 4.	STM32L15xQE UFBGA132 ballout	33
Figure 5.	STM32L15xVE LQFP100 pinout	34
Figure 6.	STM32L15xRE LQFP64 pinout	35
Figure 7.	STM32L15xVEY WLCSP104 ballout	36
Figure 8.	Memory map	55
Figure 9.	Pin loading conditions	56
Figure 10.	Pin input voltage	56
Figure 11.	Power supply scheme	57
Figure 12.	Optional LCD power supply scheme	58
Figure 13.	Current consumption measurement scheme	58
Figure 14.	High-speed external clock source AC timing diagram	76
Figure 15.	Low-speed external clock source AC timing diagram	77
Figure 16.	HSE oscillator circuit diagram	79
Figure 17.	Typical application with a 32.768 kHz crystal	80
Figure 18.	I/O AC characteristics definition	92
Figure 19.	Recommended NRST pin protection	93
Figure 20.	I ² C bus AC waveforms and measurement circuit	95
Figure 21.	SPI timing diagram - slave mode and CPHA = 0	97
Figure 22.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	97
Figure 23.	SPI timing diagram - master mode ⁽¹⁾	98
Figure 24.	USB timings: definition of data signal rise and fall time	99
Figure 25.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	101
Figure 26.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	101
Figure 27.	ADC accuracy characteristics	105
Figure 28.	Typical connection diagram using the ADC	105
Figure 29.	Maximum dynamic current consumption on V _{REF+} supply pin during ADC conversion	106
Figure 30.	12-bit buffered /non-buffered DAC	109
Figure 31.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline	114
Figure 32.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint.	116
Figure 33.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package top view example	116
Figure 34.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline	117
Figure 35.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint.	118
Figure 36.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example	119
Figure 37.	LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline	120
Figure 38.	LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint.	121
Figure 39.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example	122
Figure 40.	UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package outline	123
Figure 41.	UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package recommended footprint.	124
Figure 42.	UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package top view example	125

Figure 43. WLCSP104, 0.4 mm pitch wafer level chip scale package outline 126

Figure 44. WLCSP104, 0.4 mm pitch wafer level chip scale package recommended footprint. . . . 127

Figure 45. WLCSP104, 0.4 mm pitch wafer level chip scale package top view example 128

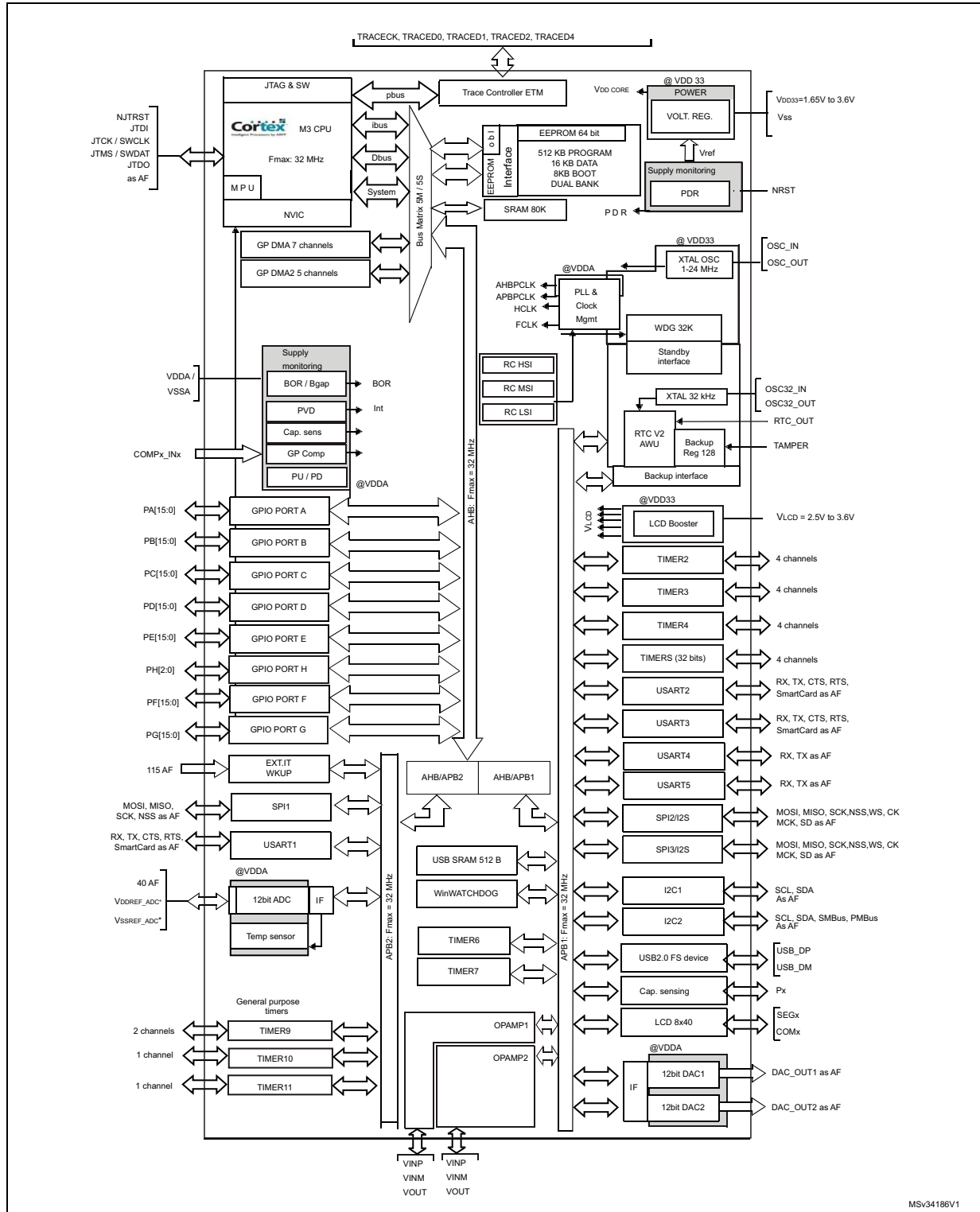
Figure 46. Thermal resistance suffix 6 130

Figure 47. Thermal resistance suffix 7 130



3 Functional overview

Figure 1. Ultra-low-power STM32L151xE and STM32L152xE block diagram



MSv34186V1

Table 3. Functionalities depending on the operating power supply range (continued)

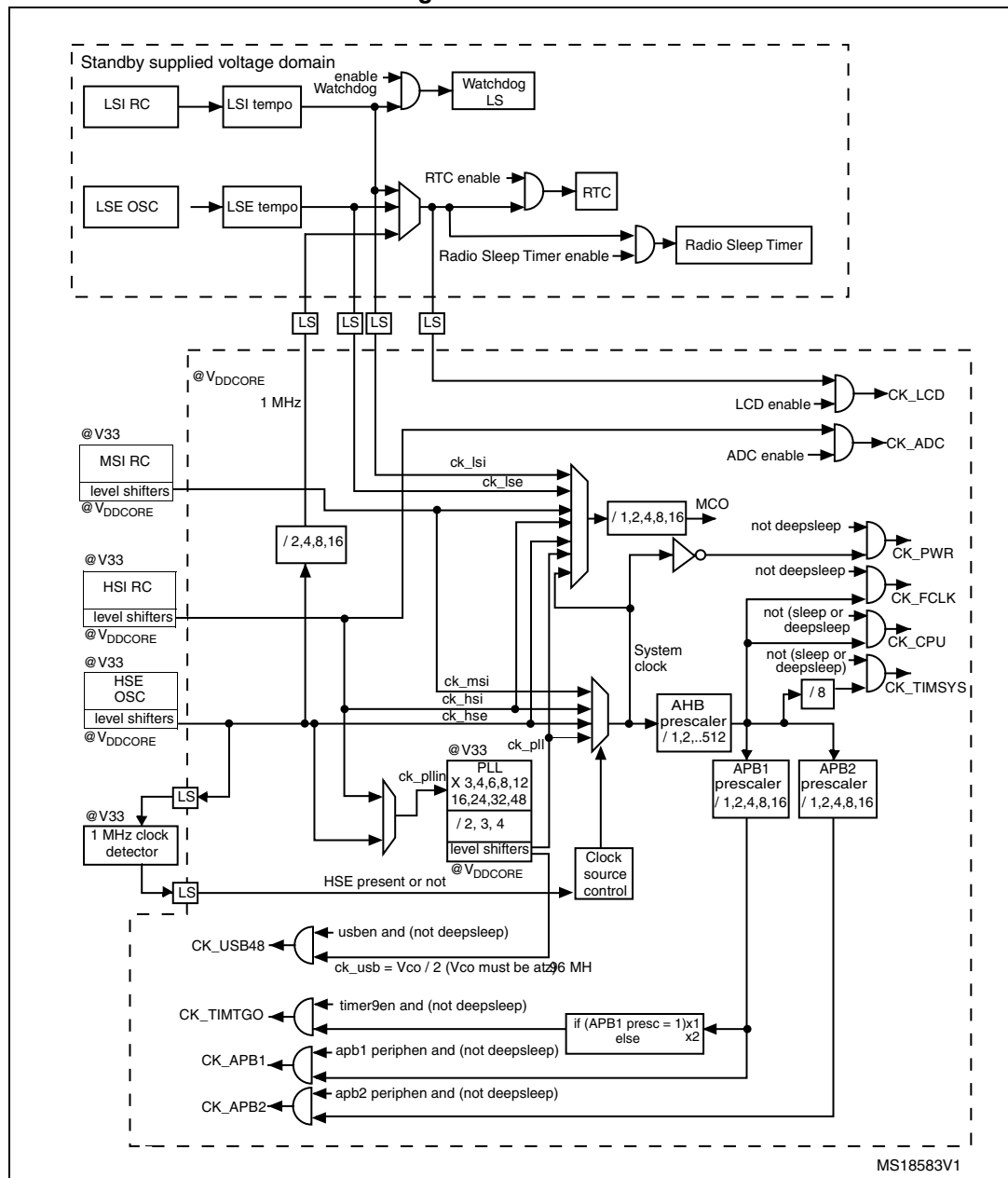
Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
$V_{DD}=V_{DDA} = 2.0 \text{ to } 2.4 \text{ V}$	Conversion time up to 500 Ksps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation
$V_{DD}=V_{DDA} = 2.4 \text{ to } 3.6 \text{ V}$	Conversion time up to 1 Msps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation

1. CPU frequency changes from initial to final must respect " $F_{CPU \text{ initial}} < 4 * F_{CPU \text{ final}}$ " to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 μs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, the user can switch from 4.2 MHz to 16 MHz, wait 5 μs , then switch from 16 MHz to 32 MHz.
2. Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Figure 2. Clock tree



1. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 24 MHz or 32 MHz.

3.19 Development support

3.19.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

3.19.2 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151xE and STM32L152xE device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number											
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	AFIO11	AFIO14	AFIO15
	Alternate function											
	SYSTEM	TIM2	TIM3/4/ 5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/ 3	UART4/ 5	LCD	CPRI	SYSTEM
PF14	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF15	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG0	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG1	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG2	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG3	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG4	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG5	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG6	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG7	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG8	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG9	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG10	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG11	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.6\text{ V}$ (for the $1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 9](#).

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 10](#).

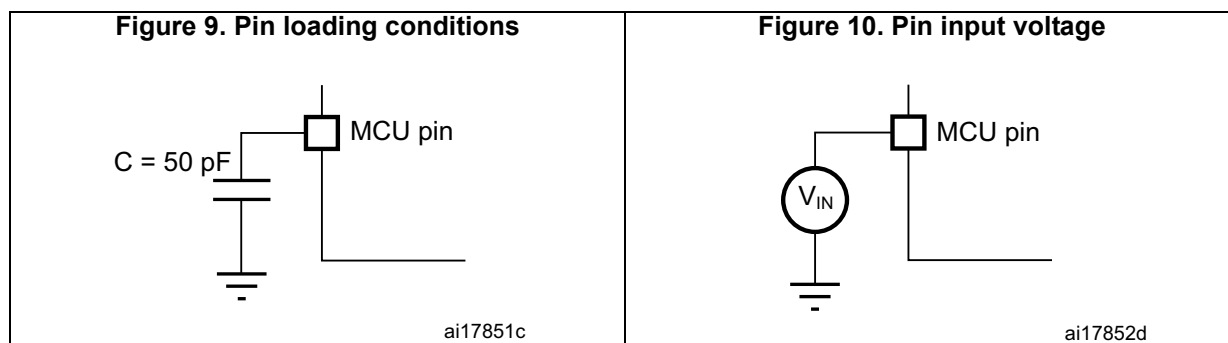


Table 20. Current consumption in Low-power run mode

Symbol	Parameter	Conditions			Typ	Max ⁽¹⁾	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	11	16	μA
				$T_A = 85\text{ }^{\circ}\text{C}$	36.2	40	
				$T_A = 105\text{ }^{\circ}\text{C}$	65.4	102	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	16.5	23	
				$T_A = 85\text{ }^{\circ}\text{C}$	41.9	48	
				$T_A = 105\text{ }^{\circ}\text{C}$	72.1	108	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	30	45	
				$T_A = 55\text{ }^{\circ}\text{C}$	36.1	48	
				$T_A = 85\text{ }^{\circ}\text{C}$	55.7	66	
				$T_A = 105\text{ }^{\circ}\text{C}$	86.6	125	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz $f_{HCLK} = 32$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	26	40.5	
				$T_A = 85\text{ }^{\circ}\text{C}$	53.2	67	
				$T_A = 105\text{ }^{\circ}\text{C}$	92.1	120	
			MSI clock, 65 kHz $f_{HCLK} = 65$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	33	49	
				$T_A = 85\text{ }^{\circ}\text{C}$	60.2	75	
				$T_A = 105\text{ }^{\circ}\text{C}$	95.6	130	
			MSI clock, 131 kHz $f_{HCLK} = 131$ kHz	$T_A = -40\text{ }^{\circ}\text{C}$ to $25\text{ }^{\circ}\text{C}$	48.5	71	
				$T_A = 55\text{ }^{\circ}\text{C}$	54.7	75	
				$T_A = 85\text{ }^{\circ}\text{C}$	76.1	95	
				$T_A = 105\text{ }^{\circ}\text{C}$	112	140	
$I_{DD\text{ max}}$ (LP Run)	Max allowed current in Low-power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 22. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
I_{DD} (Stop)	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	$T_A = -40^{\circ}\text{C}$ to 25°C	1.8	2.2
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	$T_A = -40^{\circ}\text{C}$ to 25°C	0.560	1.5
			$T_A = 55^{\circ}\text{C}$	2.18	4
			$T_A = 85^{\circ}\text{C}$	6.6	12
			$T_A = 105^{\circ}\text{C}$	14.9	26
I_{DD} (WU from Stop)	Supply current during wakeup from Stop mode	MSI = 4.2 MHz	$T_A = -40^{\circ}\text{C}$ to 25°C	2	-
		MSI = 1.05 MHz		1.45	-
		MSI = 65 kHz ⁽⁵⁾		1.45	-

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
3. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
5. When MSI = 64 kHz, the RMS current is measured over the first 15 μs following the wakeup event. For the remaining part of the wakeup period, the current corresponds the Run mode current.

6.3.16 Communications interfaces

I²C interface characteristics

The device I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: SDA and SCL are not “true” open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in [Table 47](#). Refer also to [Section 6.3.13: I/O port characteristics](#) for more details on the input/output cation characteristics (SDA and SCL).

Table 47. I²C characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾⁽²⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
t _w (SCLL)	SCL clock low time	4.7	-	1.3	-	μs
t _w (SCLH)	SCL clock high time	4.0	-	0.6	-	
t _{su} (SDA)	SDA setup time	250	-	100	-	ns
t _h (SDA)	SDA data hold time	-	3450 ⁽³⁾	-	900 ⁽³⁾	
t _r (SDA) t _r (SCL)	SDA and SCL rise time	-	1000	-	300	
t _f (SDA) t _f (SCL)	SDA and SCL fall time	-	300	-	300	
t _h (STA)	Start condition hold time	4.0	-	0.6	-	μs
t _{su} (STA)	Repeated Start condition setup time	4.7	-	0.6	-	
t _{su} (STO)	Stop condition setup time	4.0	-	0.6	-	μs
t _w (STO:STA)	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C _b	Capacitive load for each bus line	-	400	-	400	pF
t _{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50 ⁽⁴⁾	0	50 ⁽⁴⁾	ns

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The minimum width of the spikes filtered by the analog filter is above t_{SP(max)}.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the conditions summarized in [Table 13](#).

Refer to [Section 6.3.12: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

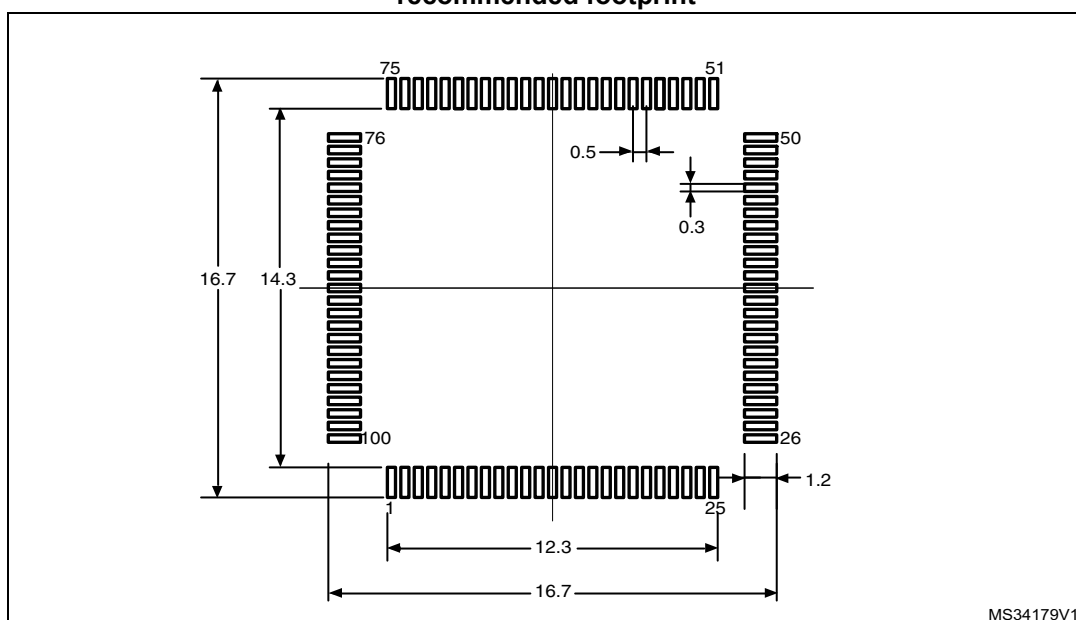
Table 49. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12 ⁽³⁾	
$t_{r(SCK)}^{(2)}$ $t_{f(SCK)}^{(2)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}^{(2)}$ $t_{w(SCKL)}^{(2)}$	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}^{(2)}$	Data input setup time	Master mode	5	-	
$t_{su(SI)}^{(2)}$		Slave mode	6	-	
$t_{h(MI)}^{(2)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}^{(2)}$		Slave mode	5	-	
$t_{a(SO)}^{(4)}$	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}^{(2)}$	Data output valid time	Slave mode	-	33	
$t_{v(MO)}^{(2)}$	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}^{(2)}$	Data output hold time	Slave mode	17	-	
$t_{h(MO)}^{(2)}$		Master mode	0.5	-	

1. The characteristics above are given for voltage range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

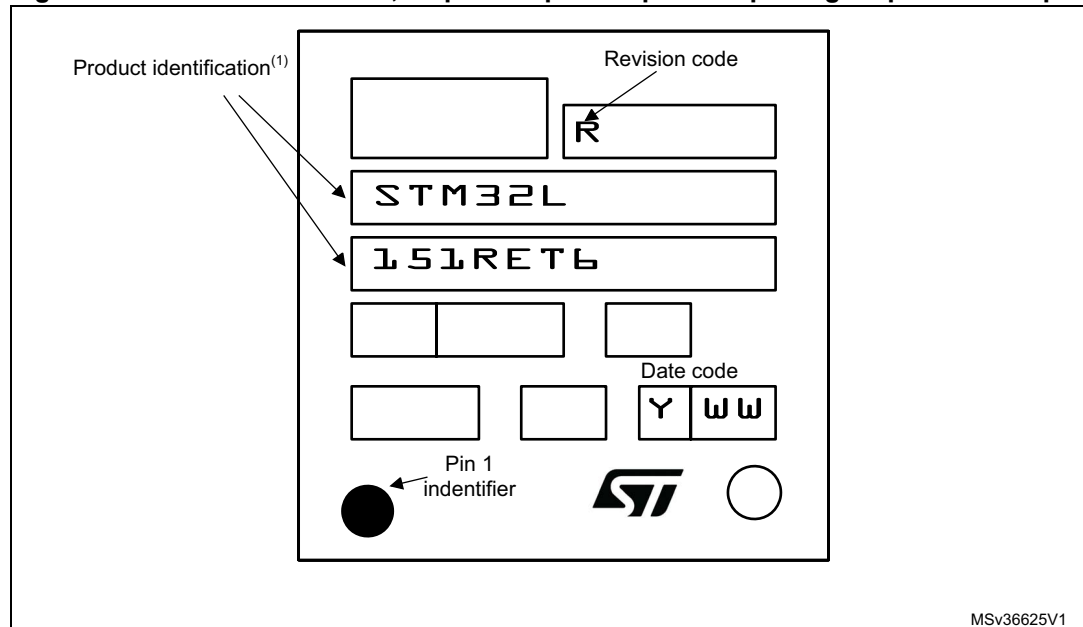
Figure 35. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint



Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

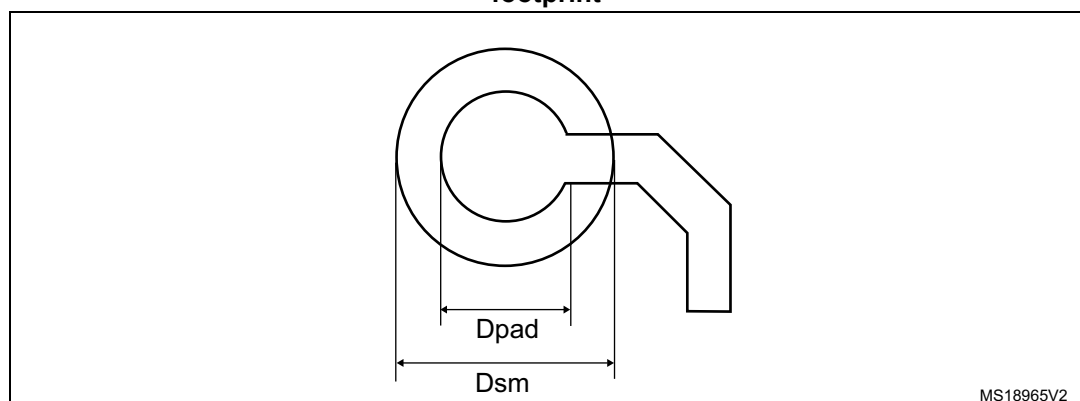
Table 69. WLCSP104, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.023
A1	-	0.175	-	-	0.0069	-
A2	-	0.38	-	-	0.015	-
A3 ⁽²⁾	-	0.025	-	-	0.001	-
ø b ⁽³⁾	0.22	0.25	0.28	0.0087	0.0098	0.011
D	4.06	4.095	4.13	0.1598	0.1612	0.1626
E	5.059	5.094	5.129	0.1992	0.2006	0.2019
e	-	0.4	-	-	0.0157	-
e1	-	3.2	-	-	0.126	-
e2	-	4.4	-	-	0.1732	-
F	-	0.447	-	-	0.0176	-
G	-	0.347	-	-	0.0137	-
aaa	-	-	0.1	-	-	0.0039
bbb	-	-	0.1	-	-	0.0039
ccc	-	-	0.1	-	-	0.0039
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating.

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 44. WLCSP104, 0.4 mm pitch wafer level chip scale package recommended footprint

7.6 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 71. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP144 - 20 x 20 mm / 0.5 mm pitch	40	°C/W
	Thermal resistance junction-ambient UFBGA132 - 7 x 7 mm	60	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	43	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient WLCSP104 - 0.400 mm pitch	46	

8 Part numbering

Table 72. STM32L151xE and STM32L152xE Ordering information scheme

Example:	STM32	L	151	R	E	T	6	D	TR
Device family STM32 = ARM-based 32-bit microcontroller									
Product type L = Low-power									
Device subfamily 151: Devices without LCD 152: Devices with LCD									
Pin count R = 64 pins V = 100/104 pins Z = 144 pins Q = 132 pins									
Flash memory size E = 512 Kbytes of Flash memory									
Package H = BGA T = LQFP Y = WLCSP104									
Temperature range 6 = Industrial temperature range, –40 to 85 °C 7 = Industrial temperature range, –40 to 105 °C									
Options No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled D = V_{DD} range: 1.65 to 3.6 V and BOR disabled									
Packing TR = tape and reel No character = tray or tube									

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.