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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	104-UFBGA, WLCSP
Supplier Device Package	104-WLCSP (5.09x4.1)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151vey6tr

2 Description

The ultra-low-power STM32L151xE and STM32L152xE devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 512 Kbytes and RAM up to 80 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32L151xE and STM32L152xE devices offer two operational amplifiers, one 12-bit ADC, two DACs, two ultra-low-power comparators, one general-purpose 32-bit timer, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151xE and STM32L152xE devices contain standard and advanced communication interfaces: up to two I2Cs, three SPIs, two I2S, three USARTs, two UARTs and an USB. The STM32L151xE and STM32L152xE devices offer up to 34 capacitive sensing channels to simply add a touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151xE devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with the contrast independent of the supply voltage.

The ultra-low-power STM32L151xE and STM32L152xE devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105 °C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.

stored by ST in the system memory area, accessible in read-only mode. See *Table 60: Temperature sensor calibration values*.

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, VREF+, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode. See *Table 15: Embedded internal reference voltage calibration values*.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels, independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151xE and STM32L152xE devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Operational amplifier

The STM32L151xE and STM32L152xE devices embed two operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

The operational amplifiers feature:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)

Pins					Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP104					Alternate functions	Additional functions
34	L2	23	14	K9	PA0-WKUP1	I/O	FT	PA0	TIM2_CH1_ETR/ TIM5_CH1/ USART2_CTS	WKUP1/RTC_TAMP2/ADC_IN0/ COMP1_INP
35	M2	24	15	L9	PA1	I/O	FT	PA1	TIM2_CH2/TIM5_CH2/ USART2_RTS/ LCD_SEG0	ADC_IN1/ COMP1_INP/ OPAMP1_VINP
36	-	25	16	J8	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1	ADC_IN2/ COMP1_INP/ OPAMP1_VINM
-	K3	-	-	-	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1	ADC_IN2/ COMP1_INP
-	M3	-	-		OPAMP1_VINM	I	TC	OPAMP1_ VINM	-	-
37	L3	26	17	H7	PA3	I/O	TC	PA3	TIM2_CH4/TIM5_CH4/ TIM9_CH2/ USART2_RX/LCD_SEG2	ADC_IN3/ COMP1_INP/ OPAMP1_VOUT
38	-	27	18	K8	V_{SS_4}	S	-	V_{SS_4}	-	-
39	-	28	19	L8, M9	V_{DD_4}	S	-	V_{DD_4}	-	-
40	J4	29	20	J7	PA4	I/O	TC	PA4	SPI1_NSS/SPI3_NSS/ I2S3_WS/ USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
41	K4	30	21	M8	PA5	I/O	TC	PA5	TIM2_CH1_ETR/ SPI1_SCK	ADC_IN5/ DAC_OUT2/ COMP1_INP
42	L4	31	22	H6	PA6	I/O	FT	PA6	TIM3_CH1/TIM10_CH1/SPI1_MISO/ LCD_SEG3	ADC_IN6/ COMP1_INP/ OPAMP2_VINP
43	-	32	23	K7	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4	ADC_IN7/ COMP1_INP/ OPAMP2_VINM
-	J5	-	-	-	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4	ADC_IN7/ COMP1_INP

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)

Pins					Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP104					Alternate functions	Additional functions
-	M4	-	-	-	OPAMP2_VINM	I	TC	OPAMP2_VINM	-	-
44	K5	33	24	L7	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
45	L5	34	25	M7	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP
46	M5	35	26	J6	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ OPAMP2_VOUT/ VREF_OUT
47	M6	36	27	K6	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
48	L6	37	28	M6	PB2	I/O	FT	PB2/ BOOT1	BOOT1	ADC_IN0b
49	K6	-	-	-	PF11	I/O	FT	PF11	-	ADC_IN1b
50	J7	-	-	-	PF12	I/O	FT	PF12	-	ADC_IN2b
51	E3	-	-	-	V_{SS_6}	S		V_{SS_6}	-	-
52	H3	-	-	-	V_{DD_6}	S		V_{DD_6}	-	-
53	K7	-	-	-	PF13	I/O	FT	PF13	-	ADC_IN3b
54	J8	-	-	-	PF14	I/O	FT	PF14	-	ADC_IN6b
55	J9	-	-	-	PF15	I/O	FT	PF15	-	ADC_IN7b
56	H9	-	-	-	PG0	I/O	FT	PG0	-	ADC_IN8b
57	G9	-	-	-	PG1	I/O	FT	PG1	-	ADC_IN9b
58	M7	38	-	L6	PE7	I/O	TC	PE7	-	ADC_IN22/ COMP1_INP
59	L7	39	-	M5	PE8	I/O	TC	PE8	-	ADC_IN23/ COMP1_INP
60	M8	40	-	M4	PE9	I/O	TC	PE9	TIM2_CH1_ETR	ADC_IN24/ COMP1_INP
61	-	-	-	-	V_{SS_7}	S	-	V_{SS_7}	-	-
62	-	-	-	-	V_{DD_7}	S	-	V_{DD_7}	-	-

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)

Pins					Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP104					Alternate functions	Additional functions
116	C8	83	54	C3	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX/ LCD_SEG31/ LCD_SEG43/LCD_COM7	-
117	B8	84	-	C4	PD3	I/O	FT	PD3	SPI2_MISO/ USART2_CTS	-
118	B7	85	-	A3	PD4	I/O	FT	PD4	SPI2_MOSI/I2S2_SD/ USART2_RTS	-
119	A6	86	-	B3	PD5	I/O	FT	PD5	USART2_TX	-
120	F7	-	-	-	V_{SS_10}	S	-	V_{SS_10}	-	-
121	G7	-	-	-	V_{DD_10}	S	-	V_{DD_10}	-	-
122	B6	87	-	B4	PD6	I/O	FT	PD6	USART2_RX	-
123	A5	88	-	A4	PD7	I/O	FT	PD7	TIM9_CH2/USART2_CK	-
124	D9	-	-	-	PG9	I/O	FT	PG9	-	-
125	D8	-	-	-	PG10	I/O	FT	PG10	-	-
126	-	-	-	-	PG11	I/O	FT	PG11	-	-
127	D7	-	-	-	PG12	I/O	FT	PG12	-	-
128	C7	-	-	-	PG13	I/O	FT	PG13	-	-
129	C6	-	-	-	PG14	I/O	FT	PG14	-	-
130	-	-	-	-	V_{SS_11}	S	-	V_{SS_11}	-	-
131	-	-	-	-	V_{DD_11}	S	-	V_{DD_11}	-	-
132	-	-	-	-	PG15	I/O	FT	PG15	-	-
133	A8	89	55	B5	PB3	I/O	FT	JTDO	TIM2_CH2/SPI1_SCK/ SPI3_SCK/ I2S3_CK/ LCD_SEG7/JTDO	COMP2_INM
134	A7	90	56	A5	PB4	I/O	FT	NJTRST	TIM3_CH1/SPI1_MISO/ SPI3_MISO/ LCD_SEG8/NJTRST	COMP2_INP
135	C5	91	57	A6	PB5	I/O	FT	PB5	TIM3_CH2/I2C1_SMBA/ SPI1_MOSI/ SPI3_MOSI/I2S3_SD/ LCD_SEG9	COMP2_INP

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)

Pins					Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP104					Alternate functions	Additional functions
136	B5	92	58	C5	PB6	I/O	FT	PB6	TIM4_CH1/I2C1_SCL/ USART1_TX	COMP2_INP
137	B4	93	59	B6	PB7	I/O	FT	PB7	TIM4_CH2/I2C1_SDA/ USART1_RX	COMP2_INP/ PVD_IN
138	A4	94	60	A7	BOOT0	I	B	BOOT0	-	-
139	A3	95	61	D5	PB8	I/O	FT	PB8	TIM4_CH3/TIM10_CH1/ I2C1_SCL/ LCD_SEG16	-
140	B3	96	62	C6	PB9	I/O	FT	PB9	TIM4_CH4/ TIM11_CH1/I2C1_SDA/ LCD_COM3	-
141	C3	97	-	B7	PE0	I/O	FT	PE0	TIM4_ETR/TIM10_CH1/ LCD_SEG36	-
142	A2	98	-	A8	PE1	I/O	FT	PE1	TIM11_CH1/LCD_SEG37	-
143	D3	99	63	C7	V_{SS_3}	S	-	V_{SS_3}	-	-
144	C4	100	64	B8, A9	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device.
3. Applicable to STM32L152xE devices only. In STM32L151xE devices, this pin should be connected to V_{DD}.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is ON (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L151xx, STM32L152xx and STM32L162xx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is ON (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.

Alternate functions

Table 9. Alternate function input/output

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	...	AFIO11	...	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
NRST	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-
PA0-WKUP1	-	TIM2_CH1_ETR	TIM5_CH1	-	-	-	-	USART2_CTS	-	-	-	-	TIMx_IC1	EVENT OUT
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	-	-	SEG0	-	TIMx_IC2	EVENT OUT
PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-	-	SEG1	-	TIMx_IC3	EVENT OUT
PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	-	SEG2	-	TIMx_IC4	EVENT OUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-	-	-	-	TIMx_IC1	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-	-	SEG3	-	TIMx_IC3	EVENT OUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-	-	SEG4	-	TIMx_IC4	EVENT OUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-	-	COM0	-	TIMx_IC1	EVENT OUT
PA9	-	-	-	-	-	-	-	USART1_TX	-	-	COM1	-	TIMx_IC2	EVENT OUT
PA10	-	-	-	-	-	-	-	USART1_RX	-	-	COM2	-	TIMx_IC3	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	-	TIMx_IC4	EVENT OUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	TIMx_IC1	EVENT OUT
PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVEN TOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	-	-	-	SEG17	-	TIMx_IC4	EVEN TOUT
PB0	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG5	-	-	EVEN TOUT
PB1	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG6	-	-	EVENT OUT
PB2	BOOT1	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK I2S3_CK	-	-	-	SEG7	-	-	EVENT OUT
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	-	-	-	SEG8	-	-	EVENT OUT
PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI I2S3_SD	-	-	-	SEG9	-	-	EVENT OUT
PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	EVENT OUT
PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-		EVENT OUT
PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	-	SEG16	-	-	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PF14	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF15	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG0	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG2	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG3	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG4	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG5	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG7	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG8	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG9	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG10	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG11	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 17. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	225	500	µA
				2 MHz	420	750	
				4 MHz	780	1200	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.98	1.6	mA
				8 MHz	1.85	2.9	
				16 MHz	3.6	5.2	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2.2	3.5	
				16 MHz	4.4	6.5	
				32 MHz	8.6	12	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	3.6	5.2	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	8.7	12.3	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	42	145	µA
		MSI clock, 524 kHz		524 kHz	135	250	
		MSI clock, 4.2 MHz		4.2 MHz	820	1200	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 19. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	51	220	µA
				2 MHz	81	300	
				4 MHz	140	380	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	175	500	
				8 MHz	330	700	
				16 MHz	625	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	395	800	
				16 MHz	760	1250	
				32 MHz	1700	2700	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	670	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1750	2700	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	19	92	
		MSI clock, 524 kHz		524 kHz	33	110	
		MSI clock, 4.2 MHz		4.2 MHz	150	273	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	63	250	
				2 MHz	93	300	
				4 MHz	155	380	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	190	500	
				8 MHz	340	700	
				16 MHz	640	1120	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	410	800	
				16 MHz	770	1300	
				32 MHz	1750	2700	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	690	1160	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1750	2800	
	Supply current in Sleep mode, Flash ON	MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	31	105	
		MSI clock, 524 kHz		524 kHz	45	125	
		MSI clock, 4.2 MHz		4.2 MHz	160	290	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

Table 22. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (Stop with RTC)	Supply current in Stop mode with RTC enabled	RTC clocked by LSI or LSE external clock (32.768kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	T_A = -40°C to 25°C V_{DD} = 1.8 V	1.18	-	µA
				T_A = -40°C to 25°C	1.4	4	
				T_A = 55°C	3.02	6	
				T_A= 85°C	7.44	11	
				T_A = 105°C	15.5	27	
			LCD ON (static duty)(2)	T_A = -40°C to 25°C	1.5	6	
				T_A = 55°C	4.65	7	
				T_A= 85°C	9.07	13	
				T_A = 105°C	15.6	31	
			LCD ON (1/8 duty)(3)	T_A = -40°C to 25°C	3.9	10	
				T_A = 55°C	5.19	11	
				T_A= 85°C	9.8	17	
				T_A = 105°C	18.4	48	
		RTC clocked by LSE external quartz (32.768kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog(4)	LCD OFF	T_A = -40°C to 25°C	1.65	-	
				T_A = 55°C	3.32	-	
				T_A= 85°C	7.83	-	
				T_A = 105°C	16	-	
			LCD ON (static duty)(2)	T_A = -40°C to 25°C	1.75	-	
				T_A = 55°C	4.9	-	
				T_A= 85°C	9.41	-	
				T_A = 105°C	15.8	-	
			LCD ON (1/8 duty)(3)	T_A = -40°C to 25°C	4.1	-	
				T_A = 55°C	5.53	-	
				T_A= 85°C	10	-	
				T_A = 105°C	18.5	-	
			LCD OFF	T_A = -40°C to 25°C V_{DD} = 1.8V	1.33	-	
				T_A = -40°C to 25°C V_{DD} = 3.0V	1.62	-	
				T_A = -40°C to 25°C V_{DD} = 3.6V	1.87	-	

Table 24. Peripheral current consumption(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	TIM2	12.0	10.0	8.0	10.0	µA/MHz (f_{HCLK})
	TIM3	10.5	8.8	7.0	8.8	
	TIM4	10.4	8.8	7.0	8.8	
	TIM5	13.8	11.5	9.1	11.5	
	TIM6	3.9	3.0	2.5	3.0	
	TIM7	3.8	3.3	2.6	3.3	
	LCD	4.2	3.6	2.8	3.6	
	WWDG	2.9	2.5	2.1	2.5	
	SPI2	5.4	4.4	3.5	4.4	
	SPI3	5.5	4.6	3.7	4.6	
	USART2	7.6	6.2	4.9	6.2	
	USART3	7.6	6.2	5.0	6.2	
	USART4	7.3	6.1	4.8	6.1	
	USART5	7.6	6.3	5.0	6.3	
	I2C1	7.3	6.1	4.8	6.1	
	I2C2	7.2	5.9	4.7	5.9	
	USB	13.0	11.2	8.9	11.2	
	PWR	2.6	2.3	1.9	2.3	
	DAC	5.9	5.0	4.0	5.0	
	COMP	3.9	3.3	2.6	3.3	

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

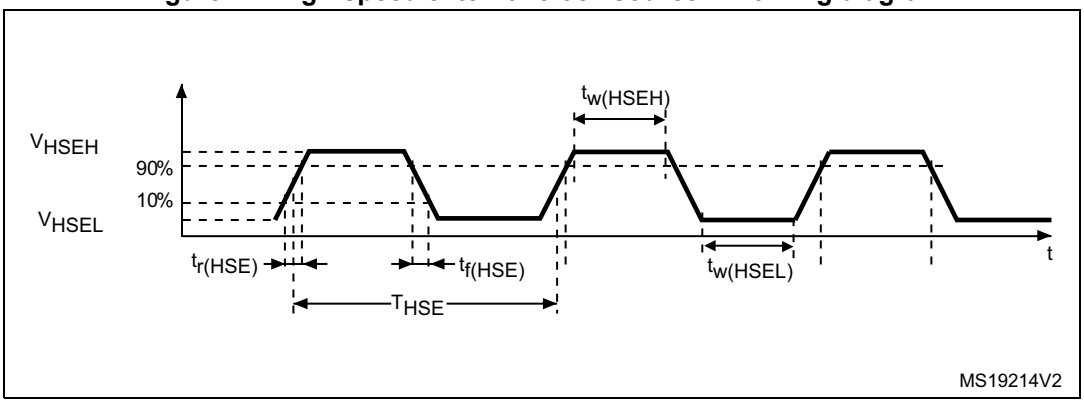
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 14*.

Table 26. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance		-	2.6	-	pF

1. Guaranteed by design.

Figure 14. High-speed external clock source AC timing diagram



Flash memory and data EEPROM

Table 35. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming/ erasing time for byte / word / double word / half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	600	-	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 36. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{CYC}(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	-	-	kcycles
	Cycling (erase / write) EEPROM data memory		300	-	-	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	T_{RET} = +85 °C	30	-	-	years
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 85 °C		30	-	-	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	T_{RET} = +105 °C	10	-	-	
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 105 °C		10	-	-	

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

Table 42. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC and FT I/O	-	-	0.3 V_{DD}(1)(2)	V
		BOOT0	-	-	0.14 V_{DD}(2)	
V_{IH}	Input high level voltage	TC I/O	0.45 V_{DD}+0.38(2)	-	-	
		FT I/O	0.39 V_{DD}+0.59(2)	-	-	
		BOOT0	0.15 V_{DD}+0.56(2)	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	TC and FT I/O	-	10% V_{DD}(3)	-	
		BOOT0	-	0.01	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB	-	-	±250	
		$V_{SS} \le V_{IN} \le V_{DD}$ TC and FT I/Os	-	-	±50	
		FT I/O $V_{DD} \le V_{IN} \le 5V$	-	-	±10	µA
R_{PU}	Weak pull-up equivalent resistor(5)(1)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by test in production
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

6.3.16 Communications interfaces

I^2C interface characteristics

The device I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: SDA and SCL are not “true” open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 47*. Refer also to *Section 6.3.13: I/O port characteristics* for more details on the input/output ction characteristics (SDA and SCL).

Table 47. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50(4)	0	50(4)	ns

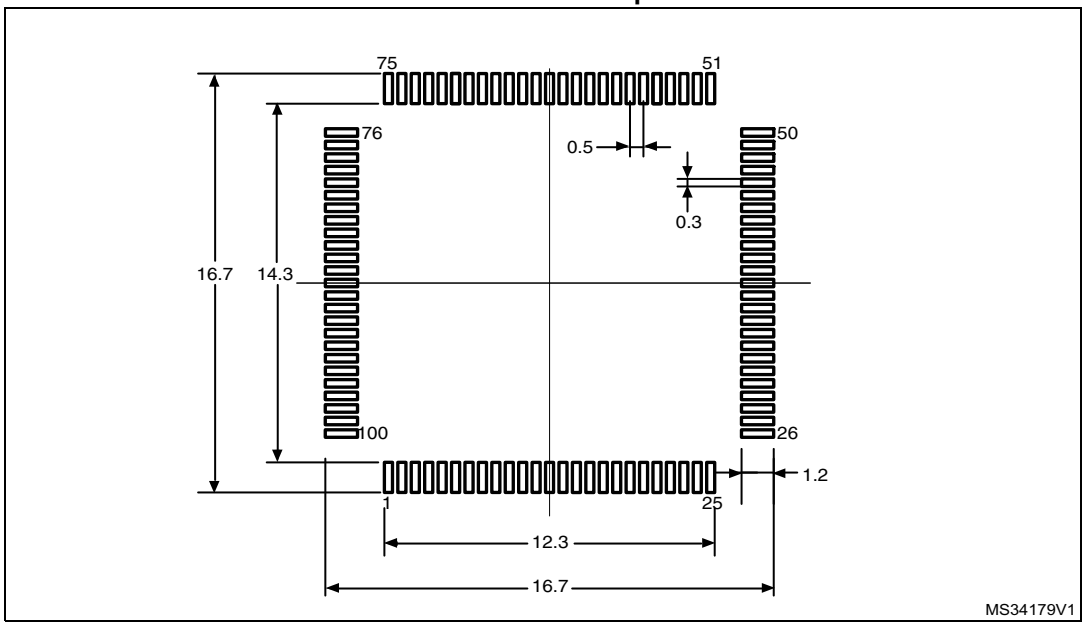
1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$.

Table 66. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint

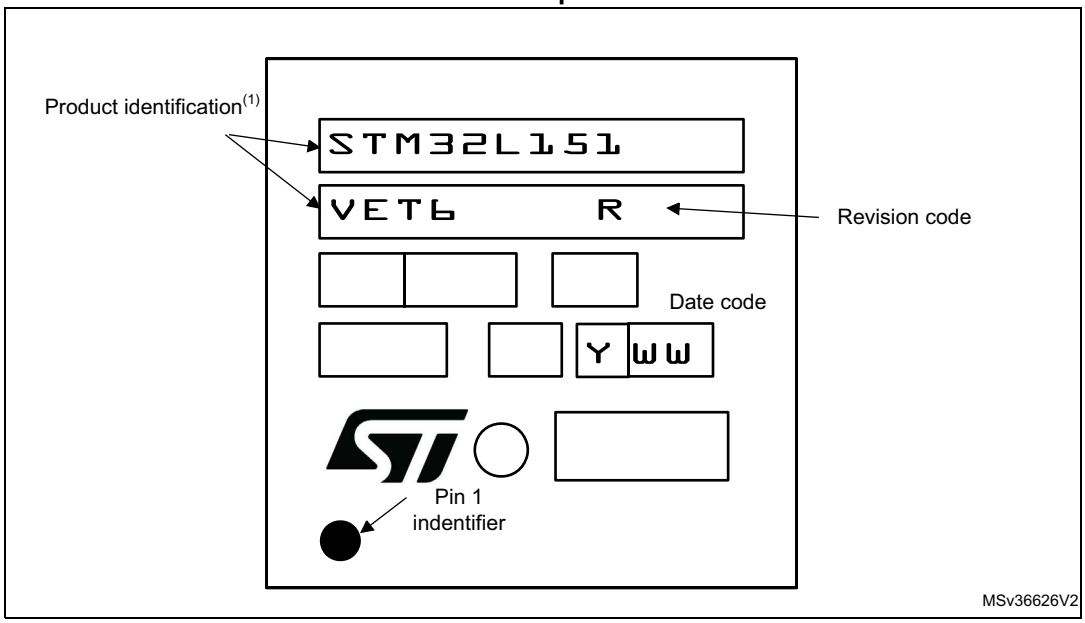


1. Dimensions are in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 36. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example



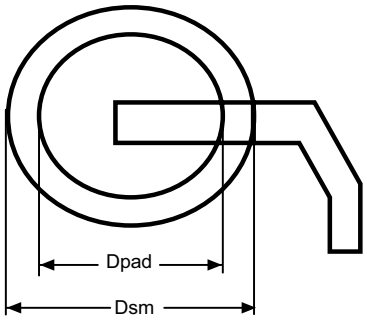
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

Table 68. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package recommended footprint



Pitch	0.5 mm
D pad	0.27 mm
Dsm	0.35 mm typ (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter

ai15495