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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	109
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16К х 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152qeh6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the startup time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot from Flash usually boots at the beginning of the Flash (bank 1). An additional boot mechanism is available through user option byte, to allow booting from bank 2 when bank 2 contains valid code. This dual boot capability can be used to easily implement a secure field software update mechanism.

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USART1, USART2 or USB. See Application note "STM32 microcontroller system memory boot mode" (AN2606) for details.

3.13 Ultra-low-power comparators and reference voltage

The STM32L151xE and STM32L152xE devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
 - DAC output
 - External I/O
 - Internal reference voltage (V_{REFINT}) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT} .

3.15 Touch sensing

The STM32L151xE and STM32L152xE devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 34 capacitive sensing channels distributed over 11 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see Section 3.14: System configuration controller and routing interface).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.



3.16 Timers and watchdogs

The ultra-low-power STM32L151xE and STM32L152xE devices include seven generalpurpose timers, two basic timers, and two watchdog timers.

Table 6 compares the features of the general-purpose and basic timers.

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Table 6. Timer feature comparison

3.16.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L151xE and STM32L152xE devices (see *Table 6* for differences).

TIM2, TIM3, TIM4, TIM5

TIM2, TIM3, TIM4 are based on 16-bit auto-reload up/down counter. TIM5 is based on a 32bit auto-reload up/down counter. They include a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures/output compares/PWMs on the largest packages.

TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

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3.17.3 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

3.17.4 Inter-integrated sound (I²S)

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The I2Ss can be served by the DMA controller.

3.17.5 Universal serial bus (USB)

The STM32L151xE and STM32L152xE devices embed a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.18 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.



4 Pin descriptions







Figure 5. STM32L15xVE LQFP100 pinout

1. This figure shows the package top view.



	I	Pins							Pin functio	ons
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP104	Pin name	Pin Type ⁽¹⁾	I / O structure	Main function ⁽²⁾ (after reset)	Alternate functions	Additional functions
-	M4	-	-	-	OPAMP2_VINM	Ι	тс	OPAMP2_ VINM	-	-
44	K5	33	24	L7	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
45	L5	34	25	M7	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP
46	M5	35	26	J6	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ OPAMP2_VOUT/ VREF_OUT
47	M6	36	27	K6	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
48	L6	37	28	M6	PB2	I/O	FT	PB2/ BOOT1	BOOT1	ADC_IN0b
49	K6	-	-	-	PF11	I/O	FT	PF11	-	ADC_IN1b
50	J7	-	-	-	PF12	I/O	FT	PF12	-	ADC_IN2b
51	E3	-	-	-	V _{SS_6}	S		V _{SS_6}	-	-
52	H3	-	-	-	V _{DD_6}	S		V _{DD_6}	-	-
53	K7	-	-	-	PF13	I/O	FT	PF13	-	ADC_IN3b
54	J8	-	-	1	PF14	I/O	FT	PF14	-	ADC_IN6b
55	J9	-	-	-	PF15	I/O	FT	PF15	-	ADC_IN7b
56	H9	-	-	-	PG0	I/O	FT	PG0	-	ADC_IN8b
57	G9	-	-	-	PG1	I/O	FT	PG1	-	ADC_IN9b
58	M7	38	-	L6	PE7	I/O	тс	PE7	-	ADC_IN22/ COMP1_INP
59	L7	39	-	M5	PE8	I/O	тс	PE8	-	ADC_IN23/ COMP1_INP
60	M8	40	-	M4	PE9	I/O	тс	PE9	TIM2_CH1_ETR	ADC_IN24/ COMP1_INP
61	-	-	-	-	V _{SS_7}	S	-	V _{SS_7}	-	-
62	-	-	-	-	V _{DD_7}	S	-	V _{DD_7}	-	-

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)



6.3.3 Embedded internal reference voltage

The parameters given in *Table 16* are based on characterization results, unless otherwise specified.

Table 15. Embedde	ed internal reference voltage	calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C V _{DDA} = 3 V ±10 mV	0x1FF8 00F8 - 0x1FF8 00F9

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
V _{REFINT out} ⁽¹⁾	Internal reference voltage	– 40 °C < T _J < +110 °C	1.202	1.224	1.242	V
I _{REFINT}	Internal reference current consumption	-	-	1.4	2.3	μΑ
T _{VREFINT}	Internal reference startup time	-	-	2	3	ms
V _{VREF_MEAS}	V _{DDA} and V _{REF+} voltage during V _{REFINT} factory measure	-	2.99	3	3.01	V
A _{VREF_MEAS}	Accuracy of factory-measured V_{REF} value ⁽²⁾	Including uncertainties due to ADC and V _{DDA} /V _{REF+} values	-	-	±5	mV
$T_{Coeff}^{(3)}$	Temperature coefficient	–40 °C < T _J < +110 °C	-	25	100	ppm/° C
A _{Coeff} ⁽³⁾	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
V _{DDCoeff} ⁽³⁾	Voltage coefficient	3.0 V < V _{DDA} < 3.6 V	-	-	2000	ppm/V
T _{S_vrefint} ⁽³⁾	ADC sampling time when reading the internal reference voltage	-	4	-	-	μs
T _{ADC_BUF} ⁽³⁾	Startup time of reference voltage buffer for ADC	-	-	-	10	μs
I _{BUF_ADC} ⁽³⁾	Consumption of reference voltage buffer for ADC	-	-	13.5	25	μA
I _{VREF_OUT} ⁽³⁾	VREF_OUT output current ⁽⁴⁾	-	-	-	1	μA
C _{VREF_OUT} ⁽³⁾	VREF_OUT output load	-	-	-	50	pF
I _{LPBUF} ⁽³⁾	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V _{REFINT_DIV1} ⁽³⁾	1/4 reference voltage	-	24	25	26	%
V _{REFINT_DIV2} ⁽³⁾	1/2 reference voltage	-	49	50	51	V _{REFIN}
V _{REFINT_DIV3} ⁽³⁾	3/4 reference voltage	-	74	75	76	Т

Table 16. Embedded internal reference voltage

1. Guaranteed by test in production.

2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

3. Guaranteed by characterization results.

4. To guarantee less than 1% VREF_OUT deviation.



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		Туріса				
Perip	bheral	Range 1, V _{CORE} = 1.8 V VOS[1:0] = 01	Range 2, V _{CORE} = 1.5 V VOS[1:0] = 10	Range 3, V _{CORE} = 1.2 V VOS[1:0] = 11	Low-power sleep and run	Unit
	SYSCFG & RI	2.9	2.4	2.0	2.4	
APB2	TIM9	8.2	6.9	5.5	6.9	
	TIM10	6.2	5.1	4.1	5.1	
	TIM11	6.2	5.1	4.1	5.1	
APBZ	ADC ⁽²⁾	9.5	7.9	6.2	7.9	
	SPI1	4.8	3.9	3.2	3.9	
	USART1	8.2	6.9	5.4	6.9	
	GPIOA	6.3	5.3	4.1	5.3	
	GPIOB	6.3	5.3	4.1	5.3	
	GPIOC	6.3	5.2	4.1	5.2	
	GPIOD	8.1	6.8	5.4	6.8	
	GPIOE	6.7	5.7	4.5	5.7	µA/MHz
	GPIOF	5.9	4.9	3.9	4.9	(f _{HCLK})
	GPIOG	7.2	6.1	4.9	6.1	
АПЬ	GPIOH	1.7	1.4	1.1	1.4	
	CRC	0.8	0.7	0.5	0.7	
	FLASH	21.6	18.1	16.0	-(6)	
	DMA1	16.8	14.5	11.5	14.5	
	DMA2	15.7	13.6	10.8	13.6	
All enabled		222	184	160	165.9	
I _{DD (RTC)}			0	.4		
I _{DD (LCD)}			3	.1		
I _{DD (ADC)} ⁽³⁾			14	50		
I _{DD (DAC)} ⁽⁴⁾						
I _{DD (COMP1)}			0.	16		μA
1	Slow mode		:	2		
'DD (COMP2)	Fast mode		:	5		
I _{DD (PVD / BOR)} (5	5)		2	.6		
I _{DD (IWDG)}			0.	25		

Table 24. Periphe	al current consum	ption ⁽¹⁾ (continued)
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 Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Lowpower run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.

2. HSI oscillator is OFF for this measure.



6.3.7 Internal clock source characteristics

The parameters given in *Table 30* are derived from tests performed under the conditions summarized in *Table 13*.

High-speed internal (HSI) RC oscillator

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
f _{HSI}	Frequency	V _{DD} = 3.0 V	-	16	-	MHz
TRIM ⁽¹⁾⁽²⁾	HSI user-trimmed	Trimming code is not a multiple of 16	-	±0.4	0.7	%
	resolution	Trimming code is a multiple of 16	-	-	±1.5	%
		V _{DDA} = 3.0 V, T _A = 25 °C	-1 ⁽³⁾	-	1 ⁽³⁾	%
	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
ACC _{HSI} ⁽²⁾		V _{DDA} = 3.0 V, T _A = -10 to 85 °C	-2.5	-	2	%
		V _{DDA} = 3.0 V, T _A = -10 to 105 °C	-4	-	2	%
		V _{DDA} = 1.65 V to 3.6 V T _A = -40 to 105 °C	-4	-	3	%
t _{SU(HSI)} ⁽²⁾	HSI oscillator startup time	-	-	3.7	6	μs
I _{DD(HSI)} ⁽²⁾	HSI oscillator power consumption	-	-	100	140	μΑ

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

2. Guaranteed by characterization results.

3. Guaranteed by test in production.

Low-speed internal (LSI) RC oscillator

Table 31. LSI oscillator characteristics

Symbol	Parameter	Min	Тур	Max	Unit
f _{LSI} ⁽¹⁾	LSI frequency	26	38	56	kHz
D _{LSI} ⁽²⁾	LSI oscillator frequency drift $0^{\circ}C \leq T_{A} \leq 105^{\circ}C$	-10	-	4	%
t _{su(LSI)} ⁽³⁾	LSI oscillator startup time	-	-	200	μs
I _{DD(LSI)} ⁽³⁾	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.

2. This is a deviation for an individual part, once the initial frequency has been measured.

3. Guaranteed by design.



Symbol	Parameter	Condition	Тур	Max	Unit
		MSI range 0	-	40	
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
t _{stab(MSI)} ⁽²⁾	MSI oscillator stabilization time	MSI range 4	-	2.5	μs
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
£	MSL oscillator frequency overshoot	Any range to range 5	-	4	MHz
'OVER(MSI)		Any range to range 6	-	6	

Table 32. MSI oscillator characteristics (continued)

1. This is a deviation for an individual part, once the initial frequency has been measured.

2. Guaranteed by characterization results.



6.3.8 PLL characteristics

The parameters given in *Table 33* are derived from tests performed under the conditions summarized in *Table 13*.

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Symbol	Paramotor		Unit			
Symbol	Falanetei	Min	Тур	Max ⁽¹⁾	0.int	
f	PLL input clock ⁽²⁾	2	-	24	MHz	
'PLL_IN	PLL input clock duty cycle	45	-	55	%	
f _{PLL_OUT}	PLL output clock	2	-	32	MHz	
t _{LOCK}	PLL lock time PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	μs	
Jitter	Cycle-to-cycle jitter	-	-	±600	ps	
I _{DDA} (PLL)	Current consumption on V _{DDA}	-	220	450		
I _{DD} (PLL)	PLL) Current consumption on V _{DD}		120	150	μΑ	

Table 33. P	LL characteristics
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1. Guaranteed by characterization results.

2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT} .

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
VRM	Data retention mode ⁽¹⁾	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).





Figure 20. I²C bus AC waveforms and measurement circuit

- 1. R_S = series protection resistor.
- 2. R_P = external pull-up resistor.
- 3. V_{DD_12C} is the I2C bus power supply.
- 4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

face (kHz)	I2C_CCR value
	R _P = 4.7 kΩ
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

Table 48. SCL frequency (f_{PCLK1} = 32 MHz, $V_{DD} = V_{DD_{12C}} = 3.3 V$)⁽¹⁾⁽²⁾

1. R_P = External pull-up resistance, f_{SCL} = I^2C speed.

For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.





Figure 21. SPI timing diagram - slave mode and CPHA = 0





1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.



Driver characteristics ⁽¹⁾					
Symbol	Parameter Conditions Min Max				Unit
t _{rfm}	Rise/ fall time matching	t _r /t _f	90	110	%
V _{CRS}	Output signal crossover voltage		1.3	2.0	V

Table 52. USB: full speed electrical characteristics (continued)

1. Guaranteed by design.

2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

I2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit	
f _{MCK}	I2S Main Clock Output		256 x 8K	256xFs ⁽¹⁾	MHz	
f	128 clock frequency	Master data: 32 bits	-	64xFs		
'CK	125 Clock frequency	Slave data: 32 bits	-	64xFs	WI⊓Z	
D _{CK}	I2S clock frequency duty cycle	Slave receiver, 48KHz	30	70	%	
t _{r(CK)}	I2S clock rise time	Capacitive lead CL =20pE		8		
t _{f(CK)}	I2S clock fall time		-	8		
t _{v(WS)}	WS valid time	Master mode	4	24		
t _{h(WS)}	WS hold time	Master mode	0	-		
t _{su(WS)}	WS setup time	Slave mode	15	-		
t _{h(WS)}	WS hold time	Slave mode	0	-		
t _{su(SD_MR)}	Data input setup time	Master receiver	8	-		
$t_{su(SD_SR)}$	Data input setup time	Slave receiver	9	-		
t _{h(SD_MR)}	Data input hold time	Master receiver	5	-	ns	
t _{h(SD_SR)}		Slave receiver	4	-		
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	64		
t _{h(SD_ST)}	Data output hold time	Slave transmitter (after enable edge)	22	-		
t _{v(SD_MT)}	Data output valid time	Master transmitter (after enable edge)	-	12		
t _{h(SD_MT)}	Data output hold time	Master transmitter (after enable edge)	8	-		

Table 53. I2S characteristics

1. The maximum for 256xFs is 8 MHz

Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK} , f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the

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ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.



Figure 25. I²S slave timing diagram (Philips protocol)⁽¹⁾

- 1. Measurement points are done at CMOS levels: 0.3 × V_{DD} and 0.7 × $V_{DD}.$
- 2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



Figure 26. I²S master timing diagram (Philips protocol)⁽¹⁾

- 1. Guaranteed by characterization results.
- 2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.



Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.





 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity



Dimension	Recommended values	
Pitch	0.4	
Doad	260 μm max. (circular)	
Dpau	220 µm recommended	
Dsm	300 μm min. (for 260 μm diameter pad)	
PCB pad design	Non-solder mask defined via underbump allowed.	

 Table 70. WLCSP104, 0.4 mm pitch recommended PCB design rules

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.



Figure 45. WLCSP104, 0.4 mm pitch wafer level chip scale package top view example

 Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.



7.6 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

 $T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- P_D max is the sum of P_{INT} max and P_{I/O} max (P_D max = P_{INT} max + P_{I/O}max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

 $P_{I/O}$ max represents the maximum power dissipation on output pins where:

 $\mathsf{P}_{\mathsf{I}/\mathsf{O}} \max = \Sigma \; (\mathsf{V}_{\mathsf{OL}} \times \mathsf{I}_{\mathsf{OL}}) + \Sigma ((\mathsf{V}_{\mathsf{DD}} - \mathsf{V}_{\mathsf{OH}}) \times \mathsf{I}_{\mathsf{OH}}),$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit
ΘյΑ	Thermal resistance junction-ambient LQFP144 - 20 x 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient UFBGA132 - 7 x 7 mm	60	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient WLCSP104 - 0.400 mm pitch	46	

Table 71. Thermal characteristics



Date	Revision	Changes
10-Feb-2015	6	Updated Section : In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark. with new package device marking. Updated Figure 8: Memory map.
27-Apr-2015	7	Updated Section 7: Package information structure: Paragraph titles and paragraph heading level. Updated Section 7.1: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package information removing gate mark in Figure 33 and adding text for device orientation versus pin1 identifier. Updated Section 7.2: LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information removing gate mark in Figure 36 and adding note for device orientation versus pin 1 identifier. Updated Section 7: Package information for all other package device marking adding text in for device orientation versus pin 1 or ball A1 identifier. Added Figure 44: WLCSP104, 0.4 mm pitch wafer level chip scale package recommended footprint and Table 70: WLCSP104, 0.4 mm pitch recommended PCB design rules. Updated Table 8: STM32L151xE and STM32L152xE pin definitions ADC inputs. Updated Table 16: Embedded internal reference voltage temperature coefficient at 100ppm/°C. and table footnote 3: "guaranteed by design" changed by "guaranteed by characterization results". Updated Table 63: Comparator 2 characteristics new maximum threshold voltage temperature coefficient at 100ppm/°C.
09-Feb-2016	8	Updated cover page putting eight SPIs in the peripheral communication interface list. Updated <i>Table 2: Ultra-low-power STM32L151xE and STM32L152xE</i> <i>device features and peripheral counts</i> SPI and I2S lines. Updated <i>Table 39: ESD absolute maximum ratings</i> CDM class II by class C3 and C4 depending of the package. Updated all the notes, removing 'not tested in production'. Updated <i>Table 10: Voltage characteristics</i> adding note about V _{REF} - pin. Updated <i>Table 5: Functionalities depending on the working mode (from</i> <i>Run/active down to standby)</i> LSI and LSE functionalities putting "Y" in Standby mode.

Table 73. Document revision history (continued)

