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**Applications of "Embedded - Microcontrollers"**

## Details

| | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 16K x 8 |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 21x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152ret6 |

# 1       Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151xE and STM32L152xE ultra-low-power ARM$^®$ Cortex$^®$-M3 based microcontroller product line. STM32L151xE and STM32L152xE devices are microcontrollers with a Flash memory density of 512 Kbytes.

The ultra-low-power STM32L151xE and STM32L152xE family includes devices in 5 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151xE and STM32L152xE microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, video intercom
- Utility metering

This STM32L151xE and STM32L152xE datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The application note "Getting started with STM32L1xxxx hardware development" (AN3216) gives a hardware implementation overview. Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM$^®$ Cortex$^®$-M3 core please refer to the ARM$^®$ Cortex$^®$-M3 technical reference manual, available from the www.arm.com website. *Figure 1* shows the general block diagram of the device family.

## 3.4      Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.

- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.

- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.

- **System clock source**: three different clock sources can be used to drive the master clock SYSCLK:
    - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
    - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
    - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.

- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
    - 32.768 kHz low-speed external crystal (LSE)
    - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.

- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.

- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.

- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

## 3.13 Ultra-low-power comparators and reference voltage

The STM32L151xE and STM32L152xE devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  – DAC output
  – External I/O
  – Internal reference voltage ($V_{REFINT}$) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

## 3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage $V_{REFINT}$.

## 3.15 Touch sensing

The STM32L151xE and STM32L152xE devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 34 capacitive sensing channels distributed over 11 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.14: System configuration controller and routing interface*).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

## 3.16 Timers and watchdogs

The ultra-low-power STM32L151xE and STM32L152xE devices include seven general-purpose timers, two basic timers, and two watchdog timers.

*Table 6* compares the features of the general-purpose and basic timers.

**Table 6. Timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|-------|--------------------|--------------|------------------|------------------------|--------------------------|-----------------------|
| TIM2, TIM3, TIM4 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM5 | 32-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM9 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | No | 2 | No |
| TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No |
| TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

### 3.16.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L151xE and STM32L152xE devices (see *Table 6* for differences).

#### TIM2, TIM3, TIM4, TIM5

TIM2, TIM3, TIM4 are based on 16-bit auto-reload up/down counter. TIM5 is based on a 32-bit auto-reload up/down counter. They include a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures/output compares/PWMs on the largest packages.

TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

#### TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

### 3.16.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

### 3.16.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

### 3.16.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

### 3.16.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

## 3.17 Communication interfaces

### 3.17.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

### 3.17.2 Universal synchronous/asynchronous receiver transmitter (USART)

The three USART and two UART interfaces are able to communicate at speeds of up to 4 Mbit/s. They support IrDA SIR ENDEC and have LIN Master/Slave capability. The three USARTs provide hardware management of the CTS and RTS signals and are ISO 7816 compliant.

All USART/UART interfaces can be served by the DMA controller.

**Table 8. STM32L151xE and STM32L152xE pin definitions (continued)**

| Pins | | | | | | | | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP104 | Pin name | Pin Type[1] | I / O structure | Main function[2] (after reset) | Alternate functions | Additional functions |
| 34 | L2 | 23 | 14 | K9 | PA0-WKUP1 | I/O | FT | PA0 | TIM2_CH1_ETR/ TIM5_CH1/ USART2_CTS | WKUP1/RTC_TA MP2/ADC_IN0/ COMP1_INP |
| 35 | M2 | 24 | 15 | L9 | PA1 | I/O | FT | PA1 | TIM2_CH2/TIM5_CH2/ USART2_RTS/ LCD_SEG0 | ADC_IN1/ COMP1_INP/ OPAMP1_VINP |
| 36 | - | 25 | 16 | J8 | PA2 | I/O | FT | PA2 | TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1 | ADC_IN2/ COMP1_INP/ OPAMP1_VINM |
| - | K3 | - | - | - | PA2 | I/O | FT | PA2 | TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1 | ADC_IN2/ COMP1_INP |
| - | M3 | - | - | | OPAMP1_VINM | I | TC | OPAMP1_ VINM | - | - |
| 37 | L3 | 26 | 17 | H7 | PA3 | I/O | TC | PA3 | TIM2_CH4/TIM5_CH4/ TIM9_CH2/ USART2_RX/LCD_SEG2 | ADC_IN3/ COMP1_INP/ OPAMP1_VOUT |
| 38 | - | 27 | 18 | K8 | $V_{SS\_4}$ | S | - | $V_{SS\_4}$ | - | - |
| 39 | - | 28 | 19 | L8, M9 | $V_{DD\_4}$ | S | - | $V_{DD\_4}$ | - | - |
| 40 | J4 | 29 | 20 | J7 | PA4 | I/O | TC | PA4 | SPI1_NSS/SPI3_NSS/ I2S3_WS/ USART2_CK | ADC_IN4/ DAC_OUT1/ COMP1_INP |
| 41 | K4 | 30 | 21 | M8 | PA5 | I/O | TC | PA5 | TIM2_CH1_ETR/ SPI1_SCK | ADC_IN5/ DAC_OUT2/ COMP1_INP |
| 42 | L4 | 31 | 22 | H6 | PA6 | I/O | FT | PA6 | TIM3_CH1/TIM10_CH1/S PI1_MISO/ LCD_SEG3 | ADC_IN6/ COMP1_INP/ OPAMP2_VINP |
| 43 | - | 32 | 23 | K7 | PA7 | I/O | FT | PA7 | TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4 | ADC_IN7/ COMP1_INP/ OPAMP2_VINM |
| - | J5 | - | - | - | PA7 | I/O | FT | PA7 | TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4 | ADC_IN7/ COMP1_INP |

**Table 9. Alternate function input/output (continued)**

| Port name | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFIO6 | AFIO7 | AFIO8 | : | AFIO11 | : | AFIO14 | AFIO15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Digital alternate function number | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4/5 | TIM9/10/11 | I2C1/2 | SPI1/2 | SPI3 | USART1/2/3 | UART4/5 | - | LCD | - | CPRI | SYSTEM |
| PB9 | - | - | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | - | - | - | - | - | COM3 | - | - | EVENT OUT |
| PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | - | - | USART3_TX | - | - | SEG10 | - | - | EVENT OUT |
| PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | - | USART3_RX | - | - | SEG11 | - | - | EVENT OUT |
| PB12 | - | - | - | TIM10_CH1 | I2C2_SMBA | SPI2_NSS I2S2_WS | - | USART3_CK | - | - | SEG12 | - | - | EVENT OUT |
| PB13 | - | - | - | TIM9_CH1 | - | SPI2_SCK I2S2_CK | - | USART3_CTS | - | - | SEG13 | - | - | EVENT OUT |
| PB14 | - | - | - | TIM9_CH2 | - | SPI2_MISO | - | USART3_RTS | - | - | SEG14 | - | - | EVENT OUT |
| PB15 | - | - | - | TIM11_CH1 | - | SPI2_MOSI I2S2_SD | - | - | - | - | SEG15 | - | - | EVENT OUT |
| PC0 | - | - | - | - | - | - | - | - | - | - | SEG18 | - | TIMx_IC1 | EVENT OUT |
| PC1 | - | - | - | - | - | - | - | - | - | - | SEG19 | - | TIMx_IC2 | EVENT OUT |
| PC2 | - | - | - | - | - | - | - | - | - | - | SEG20 | - | TIMx_IC3 | EVENT OUT |
| PC3 | - | - | - | - | - | - | - | - | - | - | SEG21 | - | TIMx_IC4 | EVENT OUT |
| PC4 | - | - | - | - | - | - | - | - | - | - | SEG22 | - | TIMx_IC1 | EVENT OUT |
| PC5 | - | - | - | - | - | - | - | - | - | - | SEG23 | - | TIMx_IC2 | EVENT OUT |
| PC6 | - | - | TIM3_CH1 | - | - | I2S2_MCK | - | - | - | - | SEG24 | - | TIMx_IC3 | EVENT OUT |

**Table 13. General operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|-----------|-----|-----|------|
| $T_J$ | Junction temperature range | 6 suffix version | –40 | 105 | °C |
| | | 7 suffix version | –40 | 110 | |

1. When the ADC is used, refer to *Table 55: ADC characteristics*.

2. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up .

3. To sustain a voltage higher than VDD+0.3V, the internal pull-up/pull-down resistors must be disabled.

4. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_J$ max (see *Table 71: Thermal characteristics on page 129*).

5. In low-power dissipation state, $T_A$ can be extended to -40°C to 105°C temperature range as long as $T_J$ does not exceed $T_J$ max (see *Table 71: Thermal characteristics on page 129*).

### 6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the conditions summarized in *Table 13*.

**Table 14. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| $t_{VDD}$[1] | $V_{DD}$ rise time rate | BOR detector enabled | 0 | - | ∞ | µs/V |
| | | BOR detector disabled | 0 | - | 1000 | |
| | $V_{DD}$ fall time rate | BOR detector enabled | 20 | - | ∞ | |
| | | BOR detector disabled | 0 | - | 1000 | |
| $T_{RSTTEMPO}$[1] | Reset temporization | $V_{DD}$ rising, BOR enabled | - | 2 | 3.3 | ms |
| | | $V_{DD}$ rising, BOR disabled[2] | 0.4 | 0.7 | 1.6 | |
| $V_{POR/PDR}$ | Power on/power down reset threshold | Falling edge | 1 | 1.5 | 1.65 | V |
| | | Rising edge | 1.3 | 1.5 | 1.65 | |
| $V_{BOR0}$ | Brown-out reset threshold 0 | Falling edge | 1.67 | 1.7 | 1.74 | |
| | | Rising edge | 1.69 | 1.76 | 1.8 | |
| $V_{BOR1}$ | Brown-out reset threshold 1 | Falling edge | 1.87 | 1.93 | 1.97 | |
| | | Rising edge | 1.96 | 2.03 | 2.07 | |
| $V_{BOR2}$ | Brown-out reset threshold 2 | Falling edge | 2.22 | 2.30 | 2.35 | |
| | | Rising edge | 2.31 | 2.41 | 2.44 | |

## 6.3.3 Embedded internal reference voltage

The parameters given in *Table 16* are based on characterization results, unless otherwise specified.

**Table 15. Embedded internal reference voltage calibration values**

| Calibration value name | Description | Memory address |
|---|---|---|
| VREFINT_CAL | Raw data acquired at temperature of 30 °C ±5 °C $V_{DDA}$= 3 V ±10 mV | 0x1FF8 00F8 - 0x1FF8 00F9 |

**Table 16. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\,out}$ [1] | Internal reference voltage | $-40\ ^\circ C < T_J < +110\ ^\circ C$ | 1.202 | 1.224 | 1.242 | V |
| $I_{REFINT}$ | Internal reference current consumption | - | - | 1.4 | 2.3 | μA |
| $T_{VREFINT}$ | Internal reference startup time | - | - | 2 | 3 | ms |
| $V_{VREF\_MEAS}$ | $V_{DDA}$ and $V_{REF+}$ voltage during $V_{REFINT}$ factory measure | - | 2.99 | 3 | 3.01 | V |
| $A_{VREF\_MEAS}$ | Accuracy of factory-measured $V_{REF}$ value[2] | Including uncertainties due to ADC and $V_{DDA}/V_{REF+}$ values | - | - | ±5 | mV |
| $T_{Coeff}$ [3] | Temperature coefficient | $-40\ ^\circ C < T_J < +110\ ^\circ C$ | - | 25 | 100 | ppm/°C |
| $A_{Coeff}$ [3] | Long-term stability | 1000 hours, T= 25 °C | - | - | 1000 | ppm |
| $V_{DDCoeff}$ [3] | Voltage coefficient | $3.0\ V < V_{DDA} < 3.6\ V$ | - | - | 2000 | ppm/V |
| $T_{S\_vrefint}$ [3] | ADC sampling time when reading the internal reference voltage | - | 4 | - | - | μs |
| $T_{ADC\_BUF}$ [3] | Startup time of reference voltage buffer for ADC | - | - | - | 10 | μs |
| $I_{BUF\_ADC}$ [3] | Consumption of reference voltage buffer for ADC | - | - | 13.5 | 25 | μA |
| $I_{VREF\_OUT}$ [3] | VREF_OUT output current [4] | - | - | - | 1 | μA |
| $C_{VREF\_OUT}$ [3] | VREF_OUT output load | - | - | - | 50 | pF |
| $I_{LPBUF}$ [3] | Consumption of reference voltage buffer for VREF_OUT and COMP | - | - | 730 | 1200 | nA |
| $V_{REFINT\_DIV1}$ [3] | 1/4 reference voltage | - | 24 | 25 | 26 | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$ [3] | 1/2 reference voltage | - | 49 | 50 | 51 | |
| $V_{REFINT\_DIV3}$ [3] | 3/4 reference voltage | - | 74 | 75 | 76 | |

1. Guaranteed by test in production.

2. The internal $V_{REF}$ value is individually measured in production and stored in dedicated EEPROM bytes.

3. Guaranteed by characterization results.

4. To guarantee less than 1% VREF_OUT deviation.

**Table 24. Peripheral current consumption[1]**

| Peripheral | | Typical consumption, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | | | Unit |
|---|---|---|---|---|---|---|
| | | Range 1, $V_{CORE}$= 1.8 V VOS[1:0] = 01 | Range 2, $V_{CORE}$= 1.5 V VOS[1:0] = 10 | Range 3, $V_{CORE}$= 1.2 V VOS[1:0] = 11 | Low-power sleep and run | |
| APB1 | TIM2 | 12.0 | 10.0 | 8.0 | 10.0 | μA/MHz ($f_{HCLK}$) |
| | TIM3 | 10.5 | 8.8 | 7.0 | 8.8 | |
| | TIM4 | 10.4 | 8.8 | 7.0 | 8.8 | |
| | TIM5 | 13.8 | 11.5 | 9.1 | 11.5 | |
| | TIM6 | 3.9 | 3.0 | 2.5 | 3.0 | |
| | TIM7 | 3.8 | 3.3 | 2.6 | 3.3 | |
| | LCD | 4.2 | 3.6 | 2.8 | 3.6 | |
| | WWDG | 2.9 | 2.5 | 2.1 | 2.5 | |
| | SPI2 | 5.4 | 4.4 | 3.5 | 4.4 | |
| | SPI3 | 5.5 | 4.6 | 3.7 | 4.6 | |
| | USART2 | 7.6 | 6.2 | 4.9 | 6.2 | |
| | USART3 | 7.6 | 6.2 | 5.0 | 6.2 | |
| | USART4 | 7.3 | 6.1 | 4.8 | 6.1 | |
| | USART5 | 7.6 | 6.3 | 5.0 | 6.3 | |
| | I2C1 | 7.3 | 6.1 | 4.8 | 6.1 | |
| | I2C2 | 7.2 | 5.9 | 4.7 | 5.9 | |
| | USB | 13.0 | 11.2 | 8.9 | 11.2 | |
| | PWR | 2.6 | 2.3 | 1.9 | 2.3 | |
| | DAC | 5.9 | 5.0 | 4.0 | 5.0 | |
| | COMP | 3.9 | 3.3 | 2.6 | 3.3 | |

3. Data based on a differential I$_{DD}$ measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).

4. Data based on a differential I$_{DD}$ measurement between DAC in reset configuration and continuous DAC conversion of V$_{DD}$/2. DAC is in buffered mode, output is left floating.

5. Including supply current of internal reference voltage.

6  In Low-power sleep and run mode, the Flash memory must always be in power-down mode.

## 6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Stop mode
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under the conditions summarized in *Table 13*.

**Table 25. Low-power mode wakeup timings**

| Symbol | Parameter | Conditions | Typ | Max[1] | Unit |
|---|---|---|---|---|---|
| t$_{WUSLEEP}$ | Wakeup from Sleep mode | f$_{HCLK}$ = 32 MHz | 0.4 | - | µs |
| t$_{WUSLEEP\_LP}$ | Wakeup from Low-power sleep mode, f$_{HCLK}$ = 262 kHz | f$_{HCLK}$ = 262 kHz Flash enabled | 46 | - | |
| | | f$_{HCLK}$ = 262 kHz Flash switched OFF | 46 | - | |
| t$_{WUSTOP}$ | Wakeup from Stop mode, regulator in Run mode ULP bit = 1 and FWU bit = 1 | f$_{HCLK}$ = f$_{MSI}$ = 4.2 MHz | 8.2 | - | |
| | Wakeup from Stop mode, regulator in low-power mode ULP bit = 1 and FWU bit = 1 | f$_{HCLK}$ = f$_{MSI}$ = 4.2 MHz Voltage range 1 and 2 | 7.7 | 8.9 | |
| | | f$_{HCLK}$ = f$_{MSI}$ = 4.2 MHz Voltage range 3 | 8.2 | 13.1 | |
| | | f$_{HCLK}$ = f$_{MSI}$ = 2.1 MHz | 10.2 | 13.4 | |
| | | f$_{HCLK}$ = f$_{MSI}$ = 1.05 MHz | 16 | 20 | |
| | | f$_{HCLK}$ = f$_{MSI}$ = 524 kHz | 31 | 37 | |
| | | f$_{HCLK}$ = f$_{MSI}$ = 262 kHz | 57 | 66 | |
| | | f$_{HCLK}$ = f$_{MSI}$ = 131 kHz | 112 | 123 | |
| | | f$_{HCLK}$ = MSI = 65 kHz | 221 | 236 | |
| t$_{WUSTDBY}$ | Wakeup from Standby mode ULP bit = 1 and FWU bit = 1 | f$_{HCLK}$ = MSI = 2.1 MHz | 58 | 104 | |
| | Wakeup from Standby mode FWU bit = 0 | f$_{HCLK}$ = MSI = 2.1 MHz | 2.6 | 3.25 | ms |

1. Guaranteed by characterization, unless otherwise specified

### 6.3.6 External clock source characteristics

**High-speed external user clock generated from an external source**

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 14*.

**Table 26. High-speed external user clock characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE\_ext}$ | User external clock source frequency | CSS is on or PLL is used | 1 | 8 | 32 | MHz |
| | | CSS is off, PLL not used | 0 | 8 | 32 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time | - | 12 | - | - | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time | | - | - | 20 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance | | - | 2.6 | - | pF |

1. Guaranteed by design.

**Figure 14. High-speed external clock source AC timing diagram**
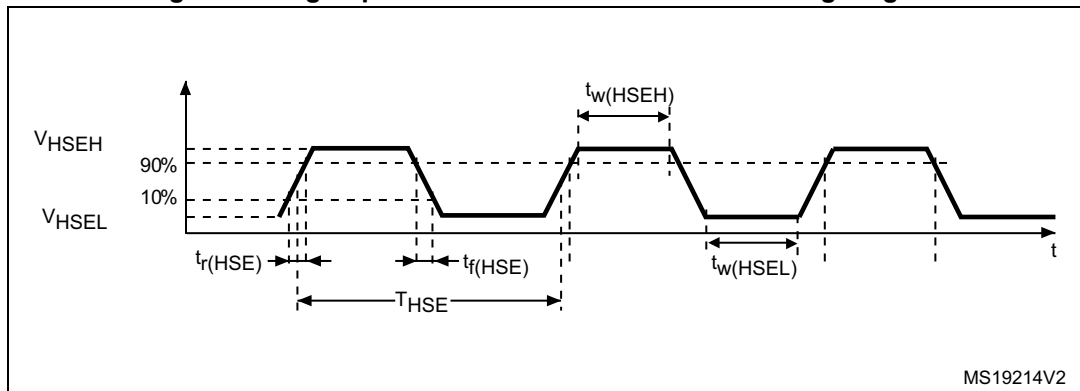
## 6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 37*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 37. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|--------|-----------|------------|--------------|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP144, $T_A$ = +25 °C, $f_{HCLK}$ = 32 MHz conforms to IEC 61000-4-2 | 4B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP144, $T_A$ = +25 °C, $f_{HCLK}$ = 32 MHz conforms to IEC 61000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:
- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

### SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the conditions summarized in *Table 13*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 49. SPI characteristics[1]**

| Symbol | Parameter | Conditions | Min | Max[2] | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 16 | MHz |
| | | Slave mode | - | 16 | |
| | | Slave transmitter | - | 12[3] | |
| $t_{r(SCK)}$[2] $t_{f(SCK)}$[2] | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 6 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | $4t_{HCLK}$ | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | $2t_{HCLK}$ | - | |
| $t_{w(SCKH)}$[2] $t_{w(SCKL)}$[2] | SCK high and low time | Master mode | $t_{SCK}/2{-}5$ | $t_{SCK}/2{+}3$ | |
| $t_{su(MI)}$[2] | Data input setup time | Master mode | 5 | - | |
| $t_{su(SI)}$[2] | | Slave mode | 6 | - | |
| $t_{h(MI)}$[2] | Data input hold time | Master mode | 5 | - | |
| $t_{h(SI)}$[2] | | Slave mode | 5 | - | |
| $t_{a(SO)}$[4] | Data output access time | Slave mode | 0 | $3t_{HCLK}$ | |
| $t_{v(SO)}$[2] | Data output valid time | Slave mode | - | 33 | |
| $t_{v(MO)}$[2] | Data output valid time | Master mode | - | 6.5 | |
| $t_{h(SO)}$[2] | Data output hold time | Slave mode | 17 | - | |
| $t_{h(MO)}$[2] | | Master mode | 0.5 | - | |

1. The characteristics above are given for voltage range 1.

2. Guaranteed by characterization results.

3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.

4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

### 6.3.22    LCD controller

The device embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the $V_{DD}$ voltage. An external capacitor $C_{ext}$ must be connected to the $V_{LCD}$ pin to decouple this converter.

**Table 64. LCD controller characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| $V_{LCD}$ | LCD external voltage | - | - | 3.6 | V |
| $V_{LCD0}$ | LCD internal reference voltage 0 | - | 2.6 | - | |
| $V_{LCD1}$ | LCD internal reference voltage 1 | - | 2.73 | - | |
| $V_{LCD2}$ | LCD internal reference voltage 2 | - | 2.86 | - | |
| $V_{LCD3}$ | LCD internal reference voltage 3 | - | 2.98 | - | |
| $V_{LCD4}$ | LCD internal reference voltage 4 | - | 3.12 | - | |
| $V_{LCD5}$ | LCD internal reference voltage 5 | - | 3.26 | - | |
| $V_{LCD6}$ | LCD internal reference voltage 6 | - | 3.4 | - | |
| $V_{LCD7}$ | LCD internal reference voltage 7 | - | 3.55 | - | |
| $C_{ext}$ | $V_{LCD}$ external capacitance | 0.1 | - | 2 | µF |
| $I_{LCD}$[1] | Supply current at $V_{DD}$ = 2.2 V | - | 3.3 | - | µA |
| | Supply current at $V_{DD}$ = 3.0 V | - | 3.1 | - | |
| $R_{Htot}$[2] | Low drive resistive network overall value | 5.28 | 6.6 | 7.92 | MΩ |
| $R_L$[2] | High drive resistive network total value | 192 | 240 | 288 | kΩ |
| $V_{44}$ | Segment/Common highest level voltage | - | - | $V_{LCD}$ | V |
| $V_{34}$ | Segment/Common 3/4 level voltage | - | 3/4 $V_{LCD}$ | - | V |
| $V_{23}$ | Segment/Common 2/3 level voltage | - | 2/3 $V_{LCD}$ | - | |
| $V_{12}$ | Segment/Common 1/2 level voltage | - | 1/2 $V_{LCD}$ | - | |
| $V_{13}$ | Segment/Common 1/3 level voltage | - | 1/3 $V_{LCD}$ | - | |
| $V_{14}$ | Segment/Common 1/4 level voltage | - | 1/4 $V_{LCD}$ | - | |
| $V_0$ | Segment/Common lowest level voltage | 0 | - | - | |
| $\Delta Vxx$[3] | Segment/Common level voltage error $T_A$ = -40 to 105 °C | - | - | ± 50 | mV |

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.

2. Guaranteed by design.

3. Guaranteed by characterization results.

## 7.2 LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information

**Figure 34. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline**
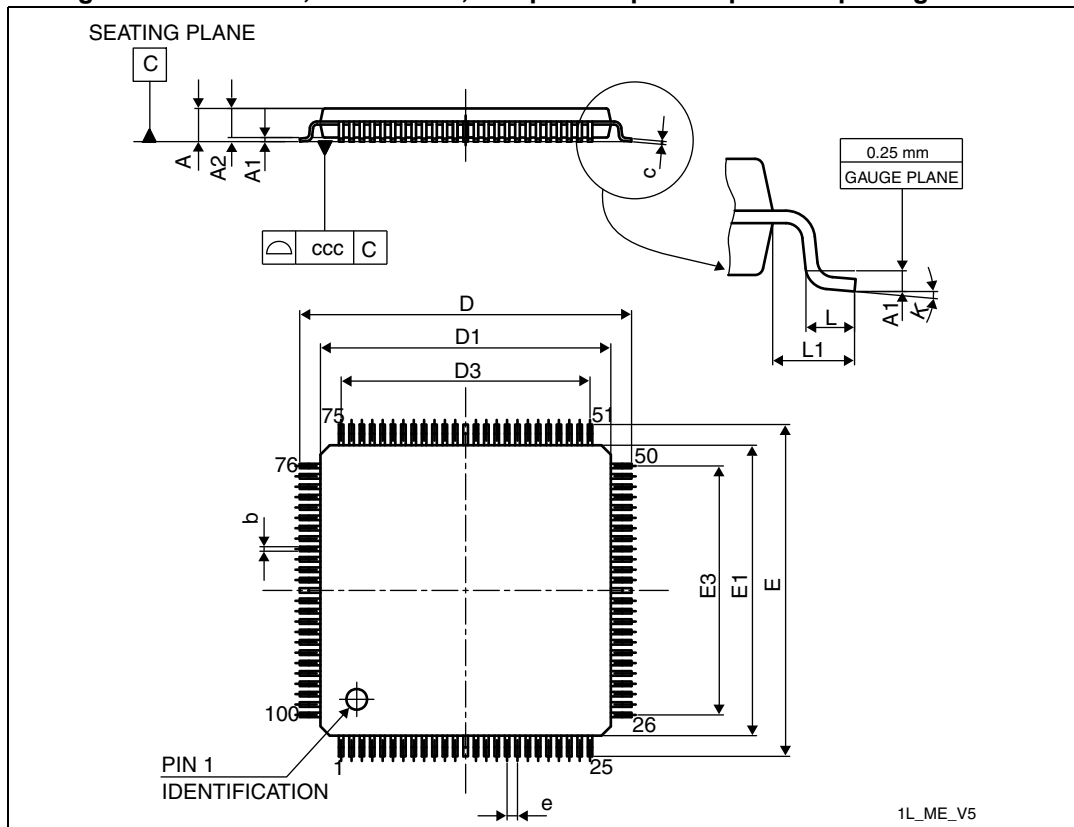


1. Drawing is not to scale.

**Table 66. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|--------|------|------|------|------|------|------|
| | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.000 | - | - | 0.4724 | - |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |

**Table 70. WLCSP104, 0.4 mm pitch recommended PCB design rules**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 |
| Dpad | 260 µm max. (circular) |
| | 220 µm recommended |
| Dsm | 300 µm min. (for 260 µm diameter pad) |
| PCB pad design | Non-solder mask defined via underbump allowed. |

### Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

**Figure 45. WLCSP104, 0.4 mm pitch wafer level chip scale package top view example**
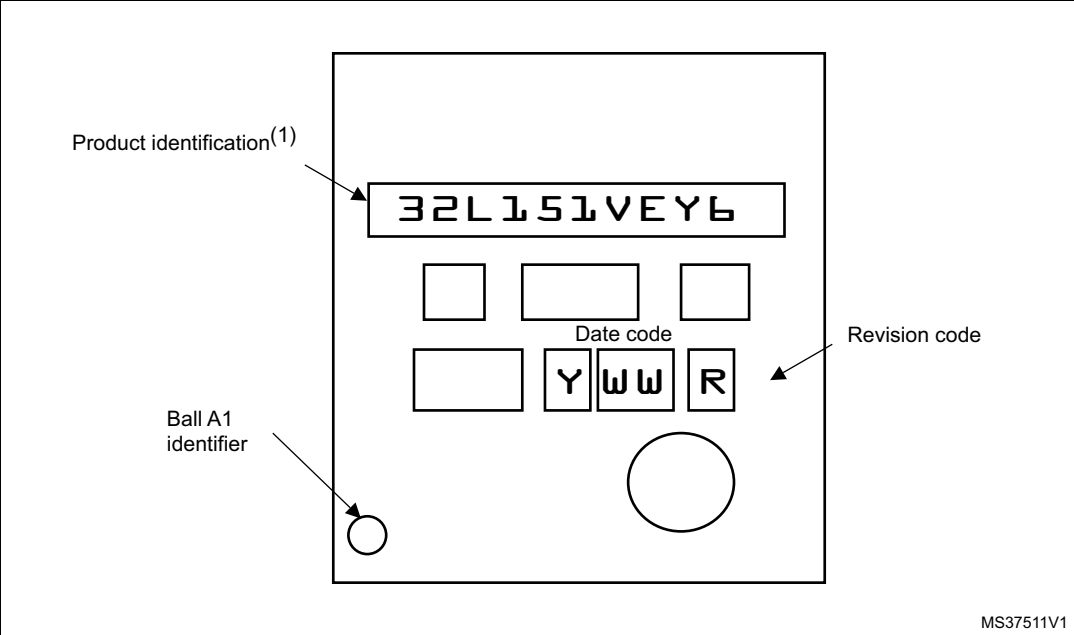


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Table 73. Document revision history (continued)**

| Date | Revision | Changes |
|------|----------|---------|
| 10-Feb-2015 | 6 | Updated *Section : In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.* with new package device marking.<br>Updated *Figure 8: Memory map*. |
| 27-Apr-2015 | 7 | Updated *Section 7: Package information* structure: Paragraph titles and paragraph heading level.<br>Updated *Section 7.1: LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package information* removing gate mark in *Figure 33* and adding text for device orientation versus pin1 identifier.<br>Updated *Section 7.2: LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information* removing gate mark in *Figure 36* and adding note for device orientation versus pin 1 identifier.<br>Updated *Section 7: Package information* for all other package device marking adding text in for device orientation versus pin 1 or ball A1 identifier.<br>Added *Figure 44: WLCSP104, 0.4 mm pitch wafer level chip scale package recommended footprint* and *Table 70: WLCSP104, 0.4 mm pitch recommended PCB design rules*.<br>Updated *Table 8: STM32L151xE and STM32L152xE pin definitions* ADC inputs.<br>Updated *Table 16: Embedded internal reference voltage* temperature coefficient at 100ppm/°C.<br>and table footnote 3: "guaranteed by design" changed by "guaranteed by characterization results".<br>Updated *Table 63: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C. |
| 09-Feb-2016 | 8 | Updated cover page putting eight SPIs in the peripheral communication interface list.<br>Updated *Table 2: Ultra-low-power STM32L151xE and STM32L152xE device features and peripheral counts* SPI and I2S lines.<br>Updated *Table 39: ESD absolute maximum ratings* CDM class II by class C3 and C4 depending of the package.<br>Updated all the notes, removing 'not tested in production'.<br>Updated *Table 10: Voltage characteristics* adding note about $V_{REF-}$ pin.<br>Updated *Table 5: Functionalities depending on the working mode (from Run/active down to standby)* LSI and LSE functionalities putting "Y" in Standby mode. |