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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152vet6tr

2 Description

The ultra-low-power STM32L151xE and STM32L152xE devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 512 Kbytes and RAM up to 80 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32L151xE and STM32L152xE devices offer two operational amplifiers, one 12-bit ADC, two DACs, two ultra-low-power comparators, one general-purpose 32-bit timer, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151xE and STM32L152xE devices contain standard and advanced communication interfaces: up to two I2Cs, three SPIs, two I2S, three USARTs, two UARTs and an USB. The STM32L151xE and STM32L152xE devices offer up to 34 capacitive sensing channels to simply add a touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151xE devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with the contrast independent of the supply voltage.

The ultra-low-power STM32L151xE and STM32L152xE devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105 °C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.

stored by ST in the system memory area, accessible in read-only mode. See *Table 60: Temperature sensor calibration values*.

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, VREF+, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode. See *Table 15: Embedded internal reference voltage calibration values*.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels, independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151xE and STM32L152xE devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Operational amplifier

The STM32L151xE and STM32L152xE devices embed two operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

The operational amplifiers feature:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)

Pins					Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP104					Alternate functions	Additional functions
34	L2	23	14	K9	PA0-WKUP1	I/O	FT	PA0	TIM2_CH1_ETR/ TIM5_CH1/ USART2_CTS	WKUP1/RTC_TAMP2/ADC_IN0/ COMP1_INP
35	M2	24	15	L9	PA1	I/O	FT	PA1	TIM2_CH2/TIM5_CH2/ USART2_RTS/ LCD_SEG0	ADC_IN1/ COMP1_INP/ OPAMP1_VINP
36	-	25	16	J8	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1	ADC_IN2/ COMP1_INP/ OPAMP1_VINM
-	K3	-	-	-	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1	ADC_IN2/ COMP1_INP
-	M3	-	-		OPAMP1_VINM	I	TC	OPAMP1_ VINM	-	-
37	L3	26	17	H7	PA3	I/O	TC	PA3	TIM2_CH4/TIM5_CH4/ TIM9_CH2/ USART2_RX/LCD_SEG2	ADC_IN3/ COMP1_INP/ OPAMP1_VOUT
38	-	27	18	K8	V_{SS_4}	S	-	V_{SS_4}	-	-
39	-	28	19	L8, M9	V_{DD_4}	S	-	V_{DD_4}	-	-
40	J4	29	20	J7	PA4	I/O	TC	PA4	SPI1_NSS/SPI3_NSS/ I2S3_WS/ USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
41	K4	30	21	M8	PA5	I/O	TC	PA5	TIM2_CH1_ETR/ SPI1_SCK	ADC_IN5/ DAC_OUT2/ COMP1_INP
42	L4	31	22	H6	PA6	I/O	FT	PA6	TIM3_CH1/TIM10_CH1/SPI1_MISO/ LCD_SEG3	ADC_IN6/ COMP1_INP/ OPAMP2_VINP
43	-	32	23	K7	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4	ADC_IN7/ COMP1_INP/ OPAMP2_VINM
-	J5	-	-	-	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4	ADC_IN7/ COMP1_INP

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	-	-	-	-	-	COM3	-	-	EVENT OUT
PB10	-	TIM2_CH3	-	-	I2C2_SCL	-	-	USART3_TX	-	-	SEG10	-	-	EVENT OUT
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	SEG11	-	-	EVENT OUT
PB12	-	-	-	TIM10_CH1	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	-	SEG12	-	-	EVENT OUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-	-	SEG13	-	-	EVENT OUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-	-	SEG14	-	-	EVENT OUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI I2S2_SD	-	-	-	-	SEG15	-	-	EVENT OUT
PC0	-	-	-	-	-	-	-	-	-	-	SEG18	-	TIMx_IC1	EVENT OUT
PC1	-	-	-	-	-	-	-	-	-	-	SEG19	-	TIMx_IC2	EVENT OUT
PC2	-	-	-	-	-	-	-	-	-	-	SEG20	-	TIMx_IC3	EVENT OUT
PC3	-	-	-	-	-	-	-	-	-	-	SEG21	-	TIMx_IC4	EVENT OUT
PC4	-	-	-	-	-	-	-	-	-	-	SEG22	-	TIMx_IC1	EVENT OUT
PC5	-	-	-	-	-	-	-	-	-	-	SEG23	-	TIMx_IC2	EVENT OUT
PC6	-	-	TIM3_CH1	-	-	I2S2_MCK	-	-	-	-	SEG24	-	TIMx_IC3	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PD4	-	-	-	-	-	SPI2_MOSI I2S2_SD	-	USART2_RTS	-	-	-	-	TIMx_IC1	EVENT OUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	TIMx_IC2	EVENT OUT
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	TIMx_IC3	EVENT OUT
PD7	-	-	-	TIM9_CH2	-	-	-	USART2_CK	-	-	-	-	TIMx_IC4	EVENT OUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	SEG28	-	TIMx_IC1	EVENT OUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	SEG29	-	TIMx_IC2	EVENT OUT
PD10	-	-	-	-	-	-	-	USART3_CK	-	-	SEG30	-	TIMx_IC3	EVENT OUT
PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	SEG31	-	TIMx_IC4	EVENT OUT
PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	SEG32	-	TIMx_IC1	EVENT OUT
PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	SEG33	-	TIMx_IC2	EVENT OUT
PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	SEG34	-	TIMx_IC3	EVENT OUT
PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	SEG35	-	TIMx_IC4	EVENT OUT
PE0	-	-	TIM4_ETR	TIM10_CH1	-	-	-	-	-	-	SEG36	-	TIMx_IC1	EVENT OUT
PE1	-	-	-	TIM11_CH1	-	-	-	-	-	-	SEG37	-	TIMx_IC2	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-	-	-	SEG 38	-	TIMx_IC3	EVENT OUT
PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-	-	-	SEG 39	-	TIMx_IC4	EVENT OUT
PE4	TRACED1	-	TIM3_CH2	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENT OUT
PE5	TRACED2	-	-	TIM9_CH1	-	-	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PE6-WKUP3	TRACED3	-	-	TIM9_CH2	-	-	-	-	-	-	-	-	TIMx_IC3	EVENT OUT
PE7	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENT OUT
PE8	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENT OUT
PE9	-	TIM2_CH1_ETR	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PE10	-	TIM2_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENT OUT
PE11	-	TIM2_CH3	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENT OUT
PE12	-	TIM2_CH4	-	-	-	SPI1_NSS	-	-	-	-	-	-	TIMx_IC1	EVENT OUT
PE13	-	-	-	-	-	SPI1_SCK	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PE14	-	-	-	-	-	SPI1_MISO	-	-	-	-	-	-	TIMx_IC3	EVENT OUT
PE15	-	-	-	-	-	SPI1_MOSI	-	-	-	-	-	-	TIMx_IC4	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PG12	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PG13	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PG14	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PG15	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PH0OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH1OSC_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH2	-	-	-	-	-	-	-	-	-	-	-	-	-	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 10: Voltage characteristics*, *Table 11: Current characteristics*, and *Table 12: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all different ground pins(3)	-	50	
V_{REF+} –V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 11* for maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 11. Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(\Sigma)}$	Total current into sum of all V_{DD_x} power lines (source)(1)	100	mA
$I_{VSS(\Sigma)}$(2)	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	100	
$I_{VDD(PIN)}$	Maximum current into each V_{DD_x} power pin (source)(1)	70	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x ground pin (sink)(1)	-70	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	60	
	Total output current sourced by sum of all IOs and control pins(2)	-60	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4), RST and B pins	-5/+0	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.17*.

Table 18. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	200	470	µA
				2 MHz	360	780	
				4 MHz	685	1200	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.80	1.5	mA
				8 MHz	1.6	3	
				16 MHz	3.1	5	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	1.9	3.5	
				16 MHz	3.7	5.55	
				32 MHz	7.55	10.9	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	3.15	4.8	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	7.75	11.7	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	40	130	µA
		MSI clock, 524 kHz		524 kHz	115	215	
		MSI clock, 4.2 MHz		4.2 MHz	715	1100	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 19. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	51	220	µA
				2 MHz	81	300	
				4 MHz	140	380	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	175	500	
				8 MHz	330	700	
				16 MHz	625	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	395	800	
				16 MHz	760	1250	
				32 MHz	1700	2700	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	670	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1750	2700	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	19	92	
		MSI clock, 524 kHz		524 kHz	33	110	
		MSI clock, 4.2 MHz		4.2 MHz	150	273	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	63	250	
				2 MHz	93	300	
				4 MHz	155	380	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	190	500	
				8 MHz	340	700	
				16 MHz	640	1120	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	410	800	
				16 MHz	770	1300	
				32 MHz	1750	2700	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	690	1160	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1750	2800	
	Supply current in Sleep mode, Flash ON	MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	31	105	
		MSI clock, 524 kHz		524 kHz	45	125	
		MSI clock, 4.2 MHz		4.2 MHz	160	290	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

Table 42. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC and FT I/O	-	-	0.3 V_{DD}(1)(2)	V
		BOOT0	-	-	0.14 V_{DD}(2)	
V_{IH}	Input high level voltage	TC I/O	0.45 V_{DD}+0.38(2)	-	-	
		FT I/O	0.39 V_{DD}+0.59(2)	-	-	
		BOOT0	0.15 V_{DD}+0.56(2)	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	TC and FT I/O	-	10% V_{DD}(3)	-	
		BOOT0	-	0.01	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB	-	-	±250	
		$V_{SS} \le V_{IN} \le V_{DD}$ TC and FT I/Os	-	-	±50	
		FT I/O $V_{DD} \le V_{IN} \le 5V$	-	-	±10	µA
R_{PU}	Weak pull-up equivalent resistor(5)(1)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by test in production
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 50. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 51. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}(2)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(2)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(2)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(3)	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}(3)	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_L is the load connected on the USB drivers.

Figure 24. USB timings: definition of data signal rise and fall time

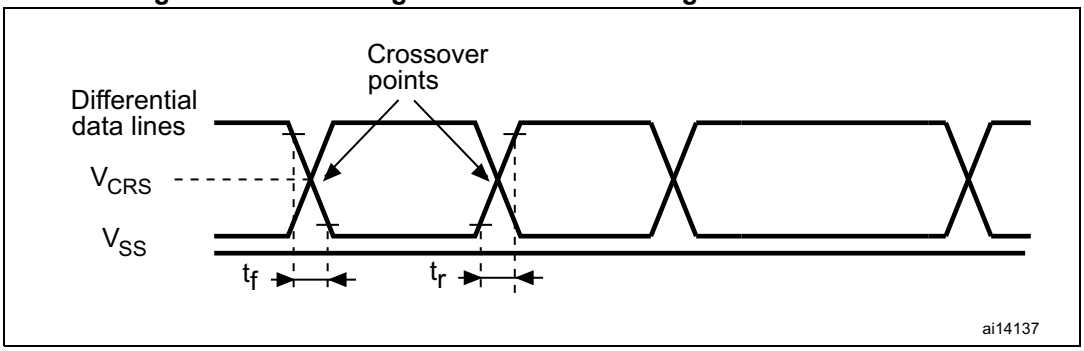


Table 52. USB: full speed electrical characteristics

Driver characteristics(1)					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall Time(2)	C_L = 50 pF	4	20	ns

Figure 27. ADC accuracy characteristics

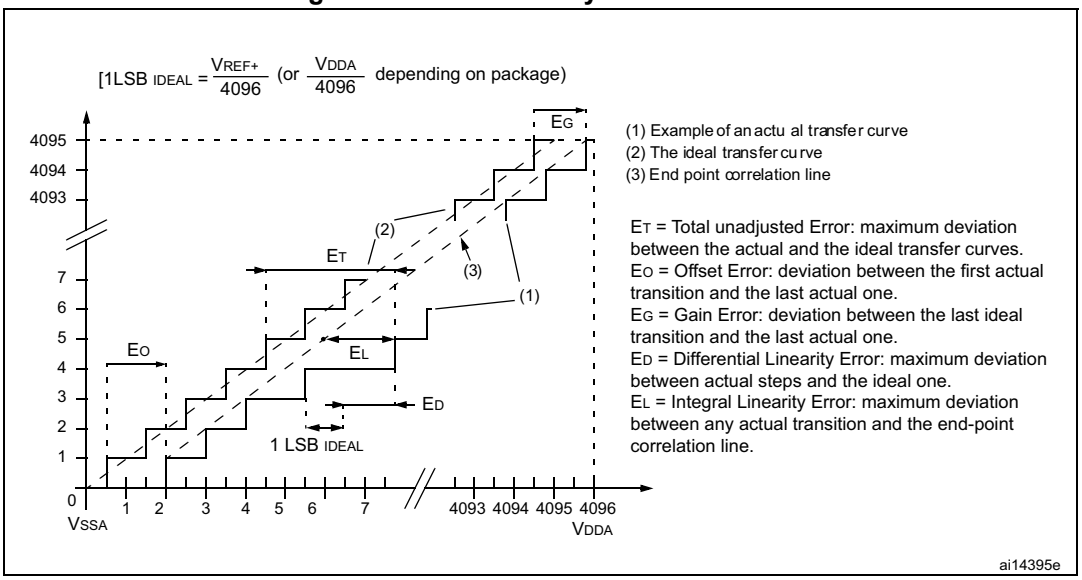
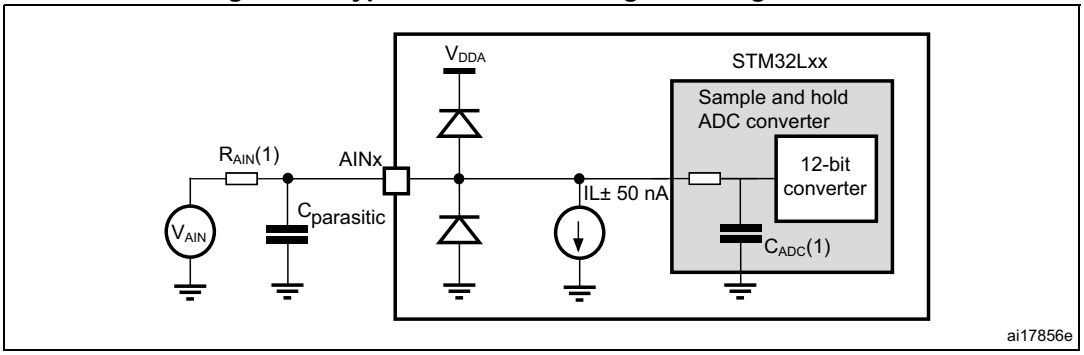


Figure 28. Typical connection diagram using the ADC



1. Refer to *Table 57: Maximum source impedance RAIN max* for the value of R_{AIN} and *Table 55: ADC characteristics* for the value of C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.20 Temperature sensor characteristics

Table 60. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00FA - 0x1FF8 00FB
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00FE - 0x1FF8 00FF

Table 61. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{110}	Voltage at 110°C ±5°C(2)	612	626.8	641.5	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	4	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V110 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.

6.3.21 Comparator

Table 62. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}$/dt	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

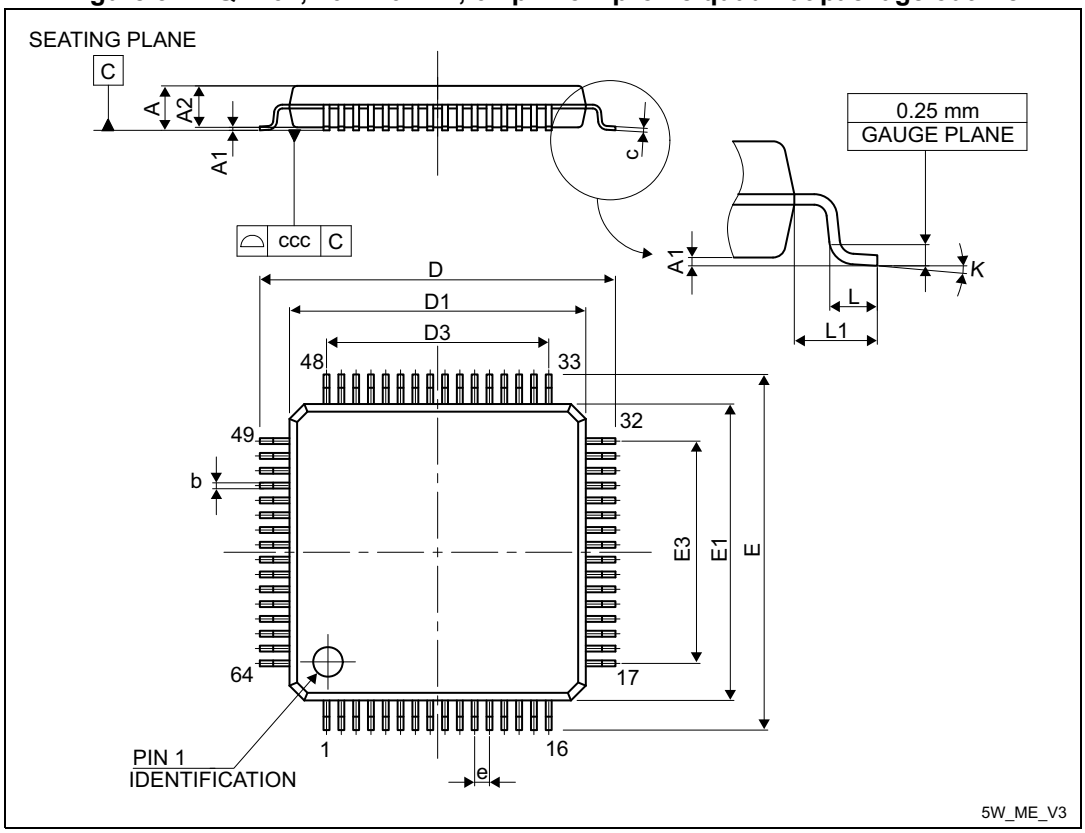
Table 65. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.3 LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package information

Figure 37. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline



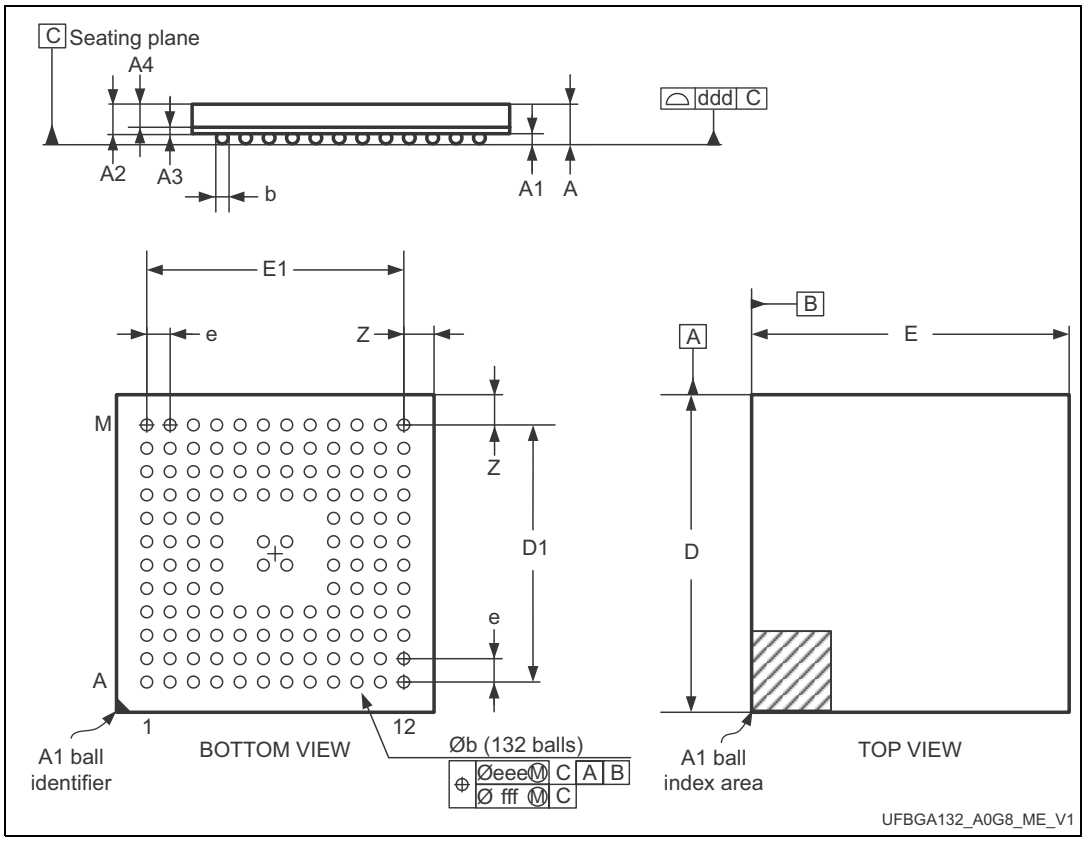
1. Drawing is not to scale.

Table 67. LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

7.4 UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package information

Figure 40. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 68. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

7.6 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 71. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP144 - 20 x 20 mm / 0.5 mm pitch	40	°C/W
	Thermal resistance junction-ambient UFBGA132 - 7 x 7 mm	60	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	43	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient WLCSP104 - 0.400 mm pitch	46	