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## What is "Embedded - Microcontrollers"?

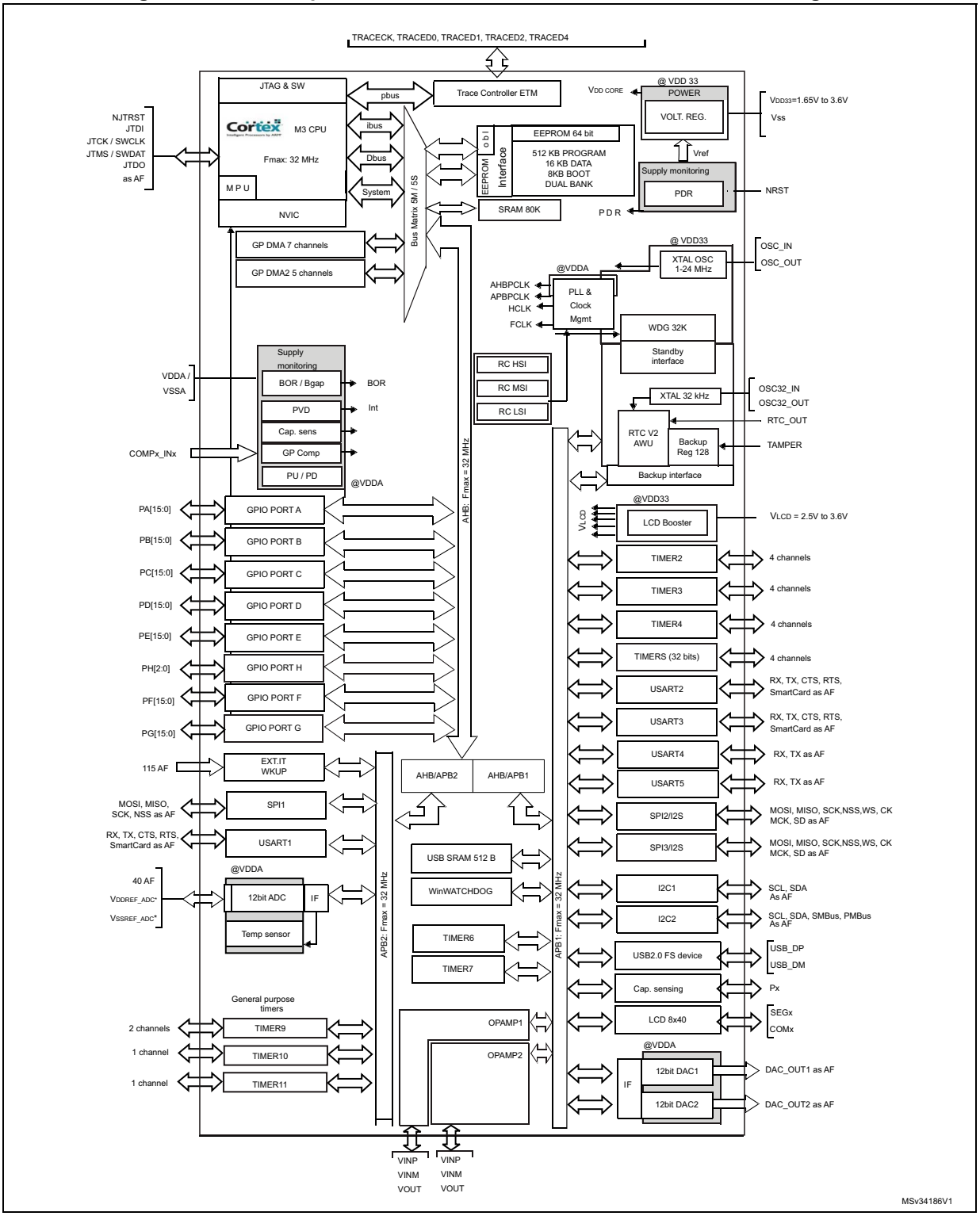
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 16K x 8 |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 25x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 104-UFBGA, WLCSP |
| Supplier Device Package | 104-WLCSP (5.09x4.1) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152vey6tr |

# 3 Functional overview

**Figure 1. Ultra-low-power STM32L151xE and STM32L152xE block diagram**



The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151xE and STM32L152xE devices are compatible with all ARM tools and software.

#### Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151xE and STM32L152xE devices embed a nested vectored interrupt controller able to handle up to 56 maskable interrupt channels (not including the 16 interrupt lines of ARM® Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

## 3.3 Reset and supply management

### 3.3.1 Power supply schemes

- $V_{DD}$ = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to $V_{DDA}$ is 1.8 V when the ADC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.

### 3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the $V_{DD}$ threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the $V_{DD}$ min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the

## 3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**: three different clock sources can be used to drive the master clock SYSCLK:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

## 3.13 Ultra-low-power comparators and reference voltage

The STM32L151xE and STM32L152xE devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage ($V_{REFINT}$) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

## 3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage $V_{REFINT}$.

## 3.15 Touch sensing

The STM32L151xE and STM32L152xE devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 34 capacitive sensing channels distributed over 11 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.14: System configuration controller and routing interface*).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

## 3.16 Timers and watchdogs

The ultra-low-power STM32L151xE and STM32L152xE devices include seven general-purpose timers, two basic timers, and two watchdog timers.

*Table 6* compares the features of the general-purpose and basic timers.

**Table 6. Timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM2, TIM3, TIM4 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM5 | 32-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM9 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | No | 2 | No |
| TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No |
| TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

### 3.16.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L151xE and STM32L152xE devices (see *Table 6* for differences).

#### TIM2, TIM3, TIM4, TIM5

TIM2, TIM3, TIM4 are based on 16-bit auto-reload up/down counter. TIM5 is based on a 32-bit auto-reload up/down counter. They include a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures/output compares/PWMs on the largest packages.

TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

#### TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

## 3.19 Development support

### 3.19.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

### 3.19.2 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151xE and STM32L152xE device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)

| Pins | | | | | Pin name | Pin Type(1) | I / O structure | Main function(2) (after reset) | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP104 | | | | | Alternate functions | Additional functions |
| 63 | L8 | 41 | - | J5 | PE10 | I/O | TC | PE10 | TIM2_CH2 | ADC_IN25/ COMP1_INP |
| 64 | M9 | 42 | - | L5 | PE11 | I/O | FT | PE11 | TIM2_CH3 | - |
| 65 | L9 | 43 | - | M3 | PE12 | I/O | FT | PE12 | TIM2_CH4/SPI1_NSS | - |
| 66 | M10 | 44 | - | K5 | PE13 | I/O | FT | PE13 | SPI1_SCK | - |
| 67 | M11 | 45 | - | L4 | PE14 | I/O | FT | PE14 | SPI1_MISO | - |
| 68 | M12 | 46 | - | K4 | PE15 | I/O | FT | PE15 | SPI1_MOSI | - |
| 69 | L10 | 47 | 29 | M2 | PB10 | I/O | FT | PB10 | TIM2_CH3/I2C2_SCL/ USART3_TX/ LCD_SEG10 | - |
| 70 | L11 | 48 | 30 | L3 | PB11 | I/O | FT | PB11 | TIM2_CH4/I2C2_SDA/ USART3_RX/ LCD_SEG11 | - |
| 71 | F12 | 49 | 31 | L2, M1 | $V_{SS\_1}$ | S | - | $V_{SS\_1}$ | - | - |
| 72 | G12 | 50 | 32 | K3 | $V_{DD\_1}$ | S | - | $V_{DD\_1}$ | - | - |
| 73 | L12 | 51 | 33 | J4 | PB12 | I/O | FT | PB12 | TIM10_CH1/I2C2_SMBA/ SPI2_NSS/I2S2_WS/ USART3_CK/ LCD_SEG12 | ADC_IN18/ COMP1_INP |
| 74 | K12 | 52 | 34 | J3 | PB13 | I/O | FT | PB13 | TIM9_CH1/SPI2_SCK/ I2S2_CK/ USART3_CTS/ LCD_SEG13 | ADC_IN19/ COMP1_INP |
| 75 | K11 | 53 | 35 | L1 | PB14 | I/O | FT | PB14 | TIM9_CH2/SPI2_MISO/ USART3_RTS/ LCD_SEG14 | ADC_IN20/ COMP1_INP |
| 76 | K10 | 54 | 36 | K2 | PB15 | I/O | FT | PB15 | TIM11_CH1/SPI2_MOSI/ I2S2_SD/ LCD_SEG15 | ADC_IN21/ COMP1_INP/ RTC_REFIN |
| 77 | K9 | 55 | - | H4 | PD8 | I/O | FT | PD8 | USART3_TX/ LCD_SEG28 | - |
| 78 | K8 | 56 | - | J2 | PD9 | I/O | FT | PD9 | USART3_RX/ LCD_SEG29 | - |

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)

| Pins | | | | | Pin name | Pin Type(1) | I / O structure | Main function(2) (after reset) | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP104 | | | | | Alternate functions | Additional functions |
| 102 | C12 | 69 | 43 | F2 | PA10 | I/O | FT | PA10 | USART1_RX / LCD_COM2 | - |
| 103 | B12 | 70 | 44 | E1 | PA11 | I/O | FT | PA11 | USART1_CTS/ SPI1_MISO | USB_DM |
| 104 | A12 | 71 | 45 | E2 | PA12 | I/O | FT | PA12 | USART1_RTS/ SPI1_MOSI | USB_DP |
| 105 | A11 | 72 | 46 | E3 | PA13 | I/O | FT | JTMS-SWDIO | JTMS-SWDIO | - |
| 106 | C11 | 73 | - | D1 | PH2 | I/O | FT | PH2 | - | - |
| 107 | F11 | 74 | 47 | D2, A1 | $V_{SS\_2}$ | S | - | $V_{SS\_2}$ | - | - |
| 108 | G11 | 75 | 48 | C1 | $V_{DD\_2}$ | S | - | $V_{DD\_2}$ | - | - |
| 109 | A10 | 76 | 49 | D3 | PA14 | I/O | FT | JTCK-SWCLK | JTCK-SWCLK | - |
| 110 | A9 | 77 | 50 | B1 | PA15 | I/O | FT | JTDI | TIM2_CH1_ETR/ SPI1_NSS/SPI3_NSS/ I2S3_WS/LCD_SEG17/ JTDI | - |
| 111 | B11 | 78 | 51 | E4 | PC10 | I/O | FT | PC10 | SPI3_SCK/I2S3_CK/ USART3_TX/ UART4_TX/ LCD_SEG28/ LCD_SEG40/LCD_COM4 | - |
| 112 | C10 | 79 | 52 | C2 | PC11 | I/O | FT | PC11 | SPI3_MISO/USART3_RX/ UART4_RX/ LCD_SEG29/ LCD_SEG41/LCD_COM5 | - |
| 113 | B10 | 80 | 53 | B2 | PC12 | I/O | FT | PC12 | SPI3_MOSI/I2S3_SD/ USART3_CK/ UART5_TX/LCD_SEG30/ LCD_SEG42/ LCD_COM6 | - |
| 114 | C9 | 81 | - | A2 | PD0 | I/O | FT | PD0 | TIM9_CH1/SPI2_NSS/ I2S2_WS | - |
| 115 | B9 | 82 | - | D4 | PD1 | I/O | FT | PD1 | SPI2_SCK/I2S2_CK | - |

**Table 17. Current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from Flash) | Supply current in Run mode, code executed from Flash | $f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 1 MHz | 225 | 500 | µA |
| | | | | 2 MHz | 420 | 750 | |
| | | | | 4 MHz | 780 | 1200 | |
| | | | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 4 MHz | 0.98 | 1.6 | mA |
| | | | | 8 MHz | 1.85 | 2.9 | |
| | | | | 16 MHz | 3.6 | 5.2 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 8 MHz | 2.2 | 3.5 | |
| | | | | 16 MHz | 4.4 | 6.5 | |
| | | | | 32 MHz | 8.6 | 12 | |
| | | HSI clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 16 MHz | 3.6 | 5.2 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 32 MHz | 8.7 | 12.3 | |
| | | MSI clock, 65 kHz | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 65 kHz | 42 | 145 | µA |
| | | MSI clock, 524 kHz | | 524 kHz | 135 | 250 | |
| | | MSI clock, 4.2 MHz | | 4.2 MHz | 820 | 1200 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 18. Current consumption in Run mode, code with data processing running from RAM**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from RAM) | Supply current in Run mode, code executed from RAM, Flash switched off | $f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 1 MHz | 200 | 470 | µA |
| | | | | 2 MHz | 360 | 780 | |
| | | | | 4 MHz | 685 | 1200 | |
| | | | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 4 MHz | 0.80 | 1.5 | mA |
| | | | | 8 MHz | 1.6 | 3 | |
| | | | | 16 MHz | 3.1 | 5 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 8 MHz | 1.9 | 3.5 | |
| | | | | 16 MHz | 3.7 | 5.55 | |
| | | | | 32 MHz | 7.55 | 10.9 | |
| | | HSI clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V VOS[1:0] = 10 | 16 MHz | 3.15 | 4.8 | |
| | | | Range 1, $V_{CORE}$=1.8 V VOS[1:0] = 01 | 32 MHz | 7.75 | 11.7 | |
| | | MSI clock, 65 kHz | Range 3, $V_{CORE}$=1.2 V VOS[1:0] = 11 | 65 kHz | 40 | 130 | µA |
| | | MSI clock, 524 kHz | | 524 kHz | 115 | 215 | |
| | | MSI clock, 4.2 MHz | | 4.2 MHz | 715 | 1100 | |

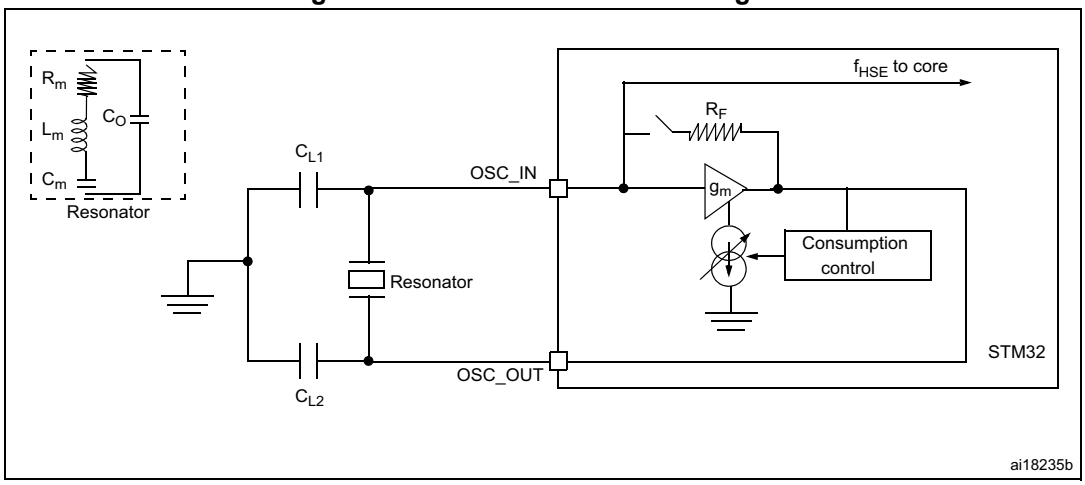
1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 20. Current consumption in Low-power run mode**

| Symbol | Parameter | Conditions | | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD\ (LP\ Run)}$ | Supply current in Low-power run mode | All peripherals OFF, code executed from RAM, Flash switched OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 11 | 16 | µA |
| | | | | $T_A$ = 85 °C | 36.2 | 40 | |
| | | | | $T_A$ = 105 °C | 65.4 | 102 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ =-40 °C to 25 °C | 16.5 | 23 | |
| | | | | $T_A$ = 85 °C | 41.9 | 48 | |
| | | | | $T_A$ = 105 °C | 72.1 | 108 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 30 | 45 | |
| | | | | $T_A$ = 55 °C | 36.1 | 48 | |
| | | | | $T_A$ = 85 °C | 55.7 | 66 | |
| | | | | $T_A$ = 105 °C | 86.6 | 125 | |
| | | All peripherals OFF, code executed from Flash, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 26 | 40.5 | |
| | | | | $T_A$ = 85 °C | 53.2 | 67 | |
| | | | | $T_A$ = 105 °C | 92.1 | 120 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ = -40 °C to 25 °C | 33 | 49 | |
| | | | | $T_A$ = 85 °C | 60.2 | 75 | |
| | | | | $T_A$ = 105 °C | 95.6 | 130 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 48.5 | 71 | |
| | | | | $T_A$ = 55 °C | 54.7 | 75 | |
| | | | | $T_A$ = 85 °C | 76.1 | 95 | |
| | | | | $T_A$ = 105 °C | 112 | 140 | |
| $I_{DD}$ max (LP Run) | Max allowed current in Low-power run mode | $V_{DD}$ from 1.65 V to 3.6 V | - | - | - | 200 | |

1. Guaranteed by characterization results, unless otherwise specified.

**Figure 16. HSE oscillator circuit diagram**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

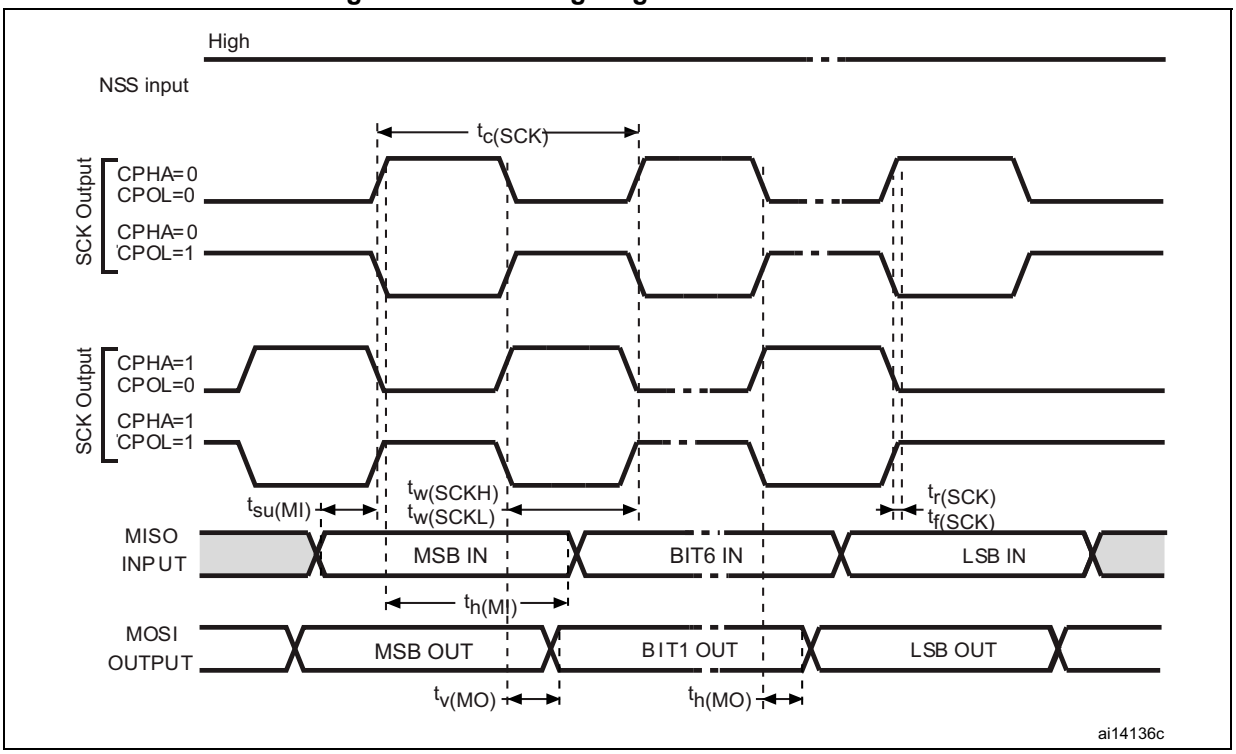
The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 29. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE}$ | Low speed external oscillator frequency | - | - | 32.768 | - | kHz |
| $R_F$ | Feedback resistor | - | - | 1.2 | - | MΩ |
| $C^{(2)}$ | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$ = 30 kΩ | - | 8 | - | pF |
| $I_{LSE}$ | LSE driving current | $V_{DD}$ = 3.3 V, $V_{IN}$ = $V_{SS}$ | - | - | 1.1 | µA |
| $I_{DD\ (LSE)}$ | LSE oscillator current consumption | $V_{DD}$ = 1.8 V | - | 450 | - | nA |
| | | $V_{DD}$ = 3.0 V | - | 600 | - | |
| | | $V_{DD}$ = 3.6V | - | 750 | - | |
| $g_m$ | Oscillator transconductance | - | 3 | - | - | µA/V |
| $t_{SU(LSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 1 | - | s |

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small $R_S$ value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.

**Figure 23. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

## USB characteristics

The USB interface is USB-IF certified (full speed).

**Table 50. USB startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB transceiver startup time | 1 | µs |

1. Guaranteed by design.

**Table 51. USB DC electrical characteristics**

| Symbol | Parameter | Conditions | Min.(1) | Max.(1) | Unit |
|---|---|---|---|---|---|
| **Input levels** | | | | | |
| $V_{DD}$ | USB operating voltage | - | 3.0 | 3.6 | V |
| $V_{DI}$(2) | Differential input sensitivity | I(USB_DP, USB_DM) | 0.2 | - | V |
| $V_{CM}$(2) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$(2) | Single ended receiver threshold | - | 1.3 | 2.0 | |
| **Output levels** | | | | | |
| $V_{OL}$(3) | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(4) | - | 0.3 | V |
| $V_{OH}$(3) | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(4) | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. $R_L$ is the load connected on the USB drivers.

**Figure 24. USB timings: definition of data signal rise and fall time**

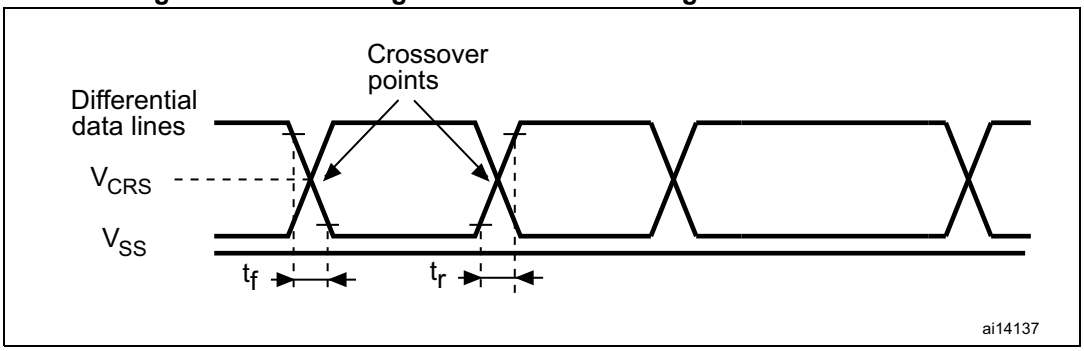



**Table 52. USB: full speed electrical characteristics**

| Driver characteristics(1) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall Time(2) | $C_L$ = 50 pF | 4 | 20 | ns |

**Table 55. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_S$ (5) | Sampling time | Direct channels 2.4 V ≤$V_{DDA}$ ≤3.6 V | 0.25 | - | - | µs |
| | | Multiplexed channels 2.4 V ≤$V_{DDA}$ ≤3.6 V | 0.56 | - | - | |
| | | Direct channels 1.8 V ≤$V_{DDA}$ ≤2.4 V | 0.56 | - | - | |
| | | Multiplexed channels 1.8 V ≤$V_{DDA}$ ≤2.4 V | 1 | - | - | |
| | | - | 4 | - | 384 | $1/f_{ADC}$ |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 16 MHz | 1 | - | 24.75 | µs |
| | | - | 4 to 384 (sampling phase) +12 (successive approximation) | | | $1/f_{ADC}$ |
| $C_{ADC}$ | Internal sample and hold capacitor | Direct channels | - | 16 | - | pF |
| | | Multiplexed channels | - | | - | |
| $f_{TRIG}$ | External trigger frequency Regular sequencer | 12-bit conversions | - | - | Tconv+1 | $1/f_{ADC}$ |
| | | 6/8/10-bit conversions | - | - | Tconv | $1/f_{ADC}$ |
| $f_{TRIG}$ | External trigger frequency Injected sequencer | 12-bit conversions | - | - | Tconv+2 | $1/f_{ADC}$ |
| | | 6/8/10-bit conversions | - | - | Tconv+1 | $1/f_{ADC}$ |
| $R_{AIN}$ (6) | Signal source impedance | | - | - | 50 | kΩ |
| $t_{lat}$ | Injection trigger conversion latency | $f_{ADC}$ = 16 MHz | 219 | - | 281 | ns |
| | | - | 3.5 | - | 4.5 | $1/f_{ADC}$ |
| $t_{latr}$ | Regular trigger conversion latency | $f_{ADC}$ = 16 MHz | 156 | - | 219 | ns |
| | | - | 2.5 | - | 3.5 | $1/f_{ADC}$ |
| $t_{STAB}$ | Power-up time | - | - | - | 3.5 | µs |

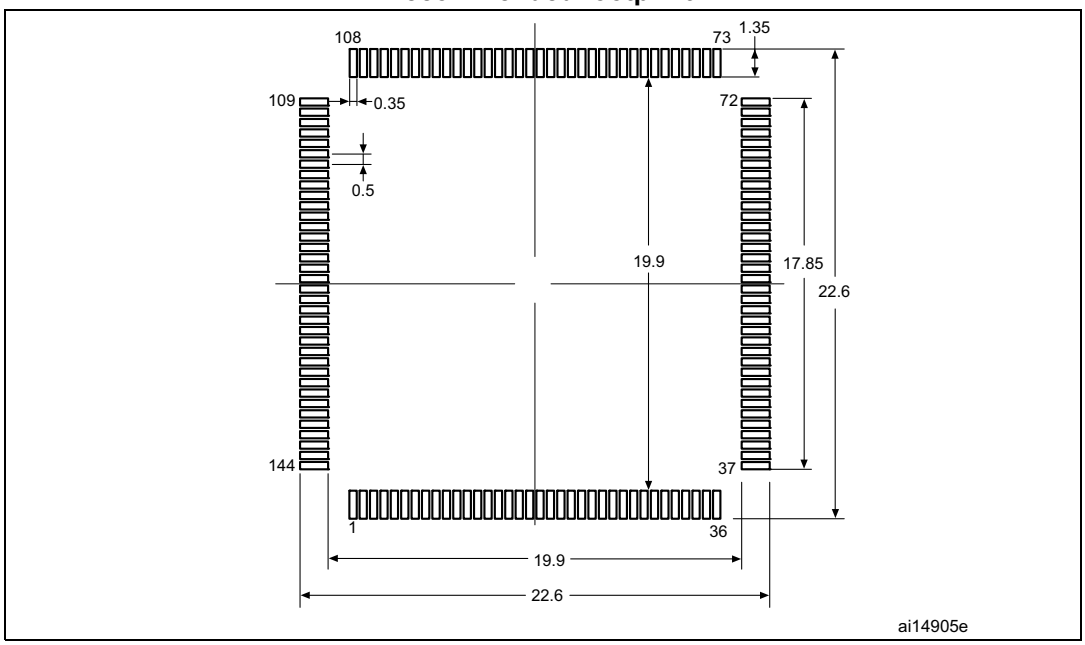
1. The Vref+ input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through VREF is composed of two parameters:

   - one constant (max 300 µA)

   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses

   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. $V_{SSA}$ or $V_{REF-}$ must be tied to ground.
5. Minimum sampling time is reached for an external input impedance limited to a value as defined in *Table 57: Maximum source impedance RAIN max*.
6. External impedance has another high value limitation when using short sampling time as defined in *Table 57: Maximum source impedance RAIN max*.

**Figure 32. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint**

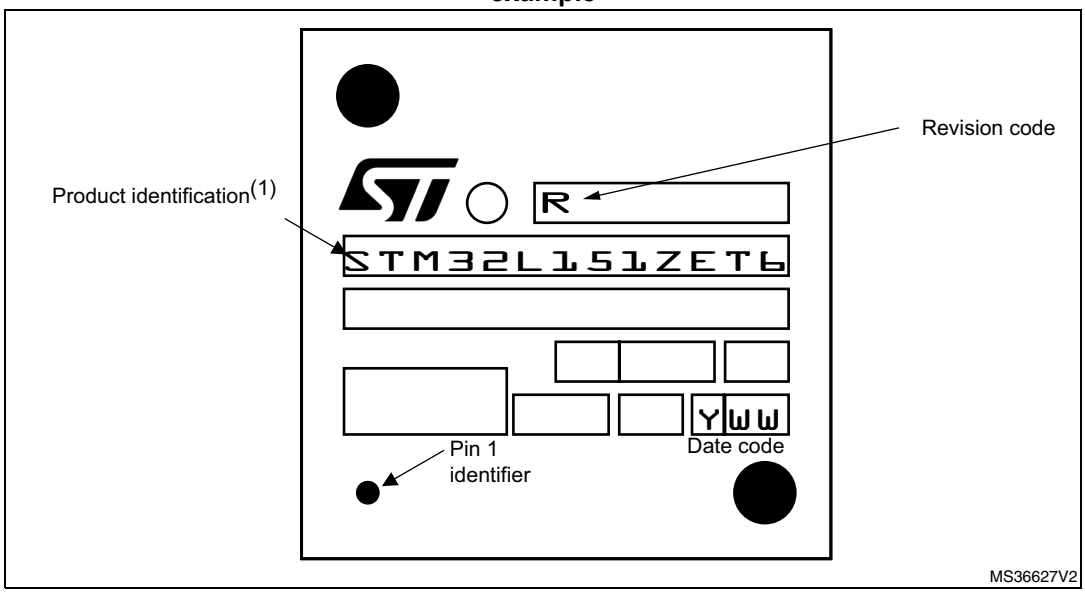



1. Dimensions are in millimeters.

## Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 33. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package top view example**

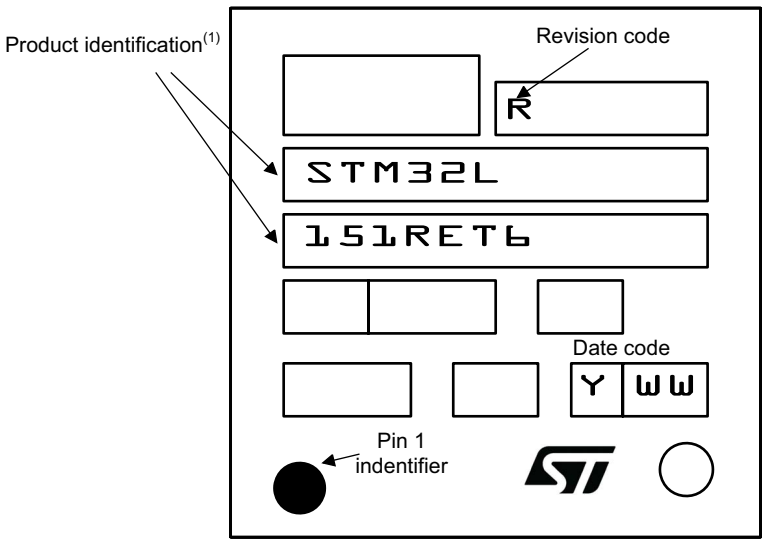



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

### Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

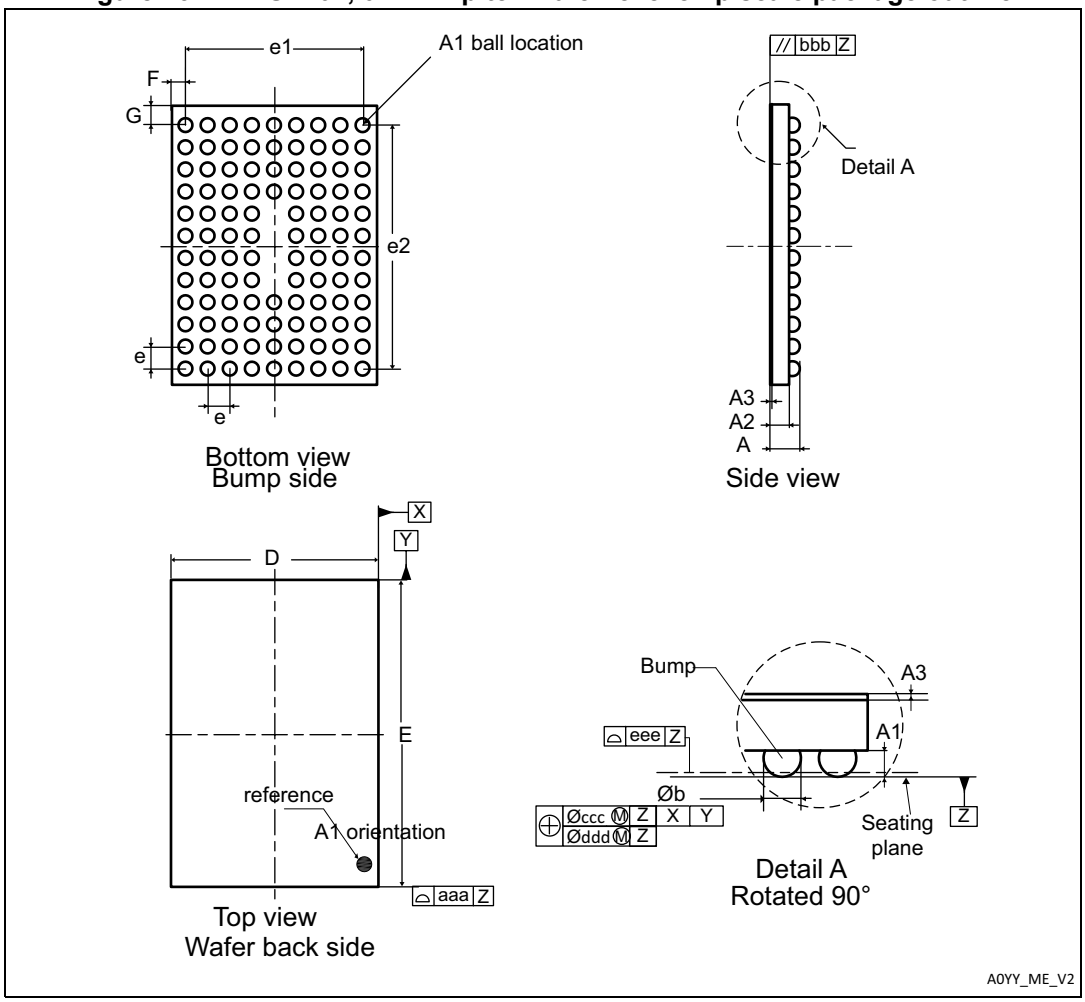
**Figure 39. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

## 7.5 WLCSP104, 0.4 mm pitch wafer level chip scale package information

**Figure 43. WLCSP104, 0.4 mm pitch wafer level chip scale package outline**




1. Drawing is not to scale.

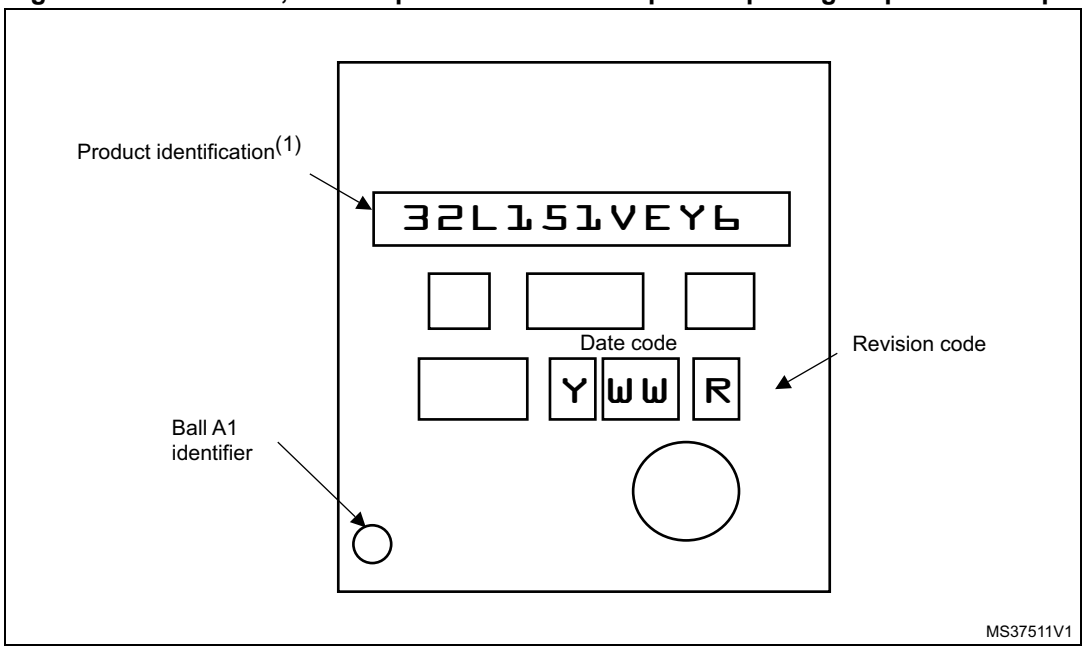
**Table 70. WLCSP104, 0.4 mm pitch recommended PCB design rules**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 |
| Dpad | 260 µm max. (circular) |
| | 220 µm recommended |
| Dsm | 300 µm min. (for 260 µm diameter pad) |
| PCB pad design | Non-solder mask defined via underbump allowed. |

## Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

**Figure 45. WLCSP104, 0.4 mm pitch wafer level chip scale package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

# 8 Part numbering

**Table 72. STM32L151xE and STM32L152xE Ordering information scheme**

Example: STM32 L 151 R E T 6 D TR

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

L = Low-power

**Device subfamily**

151: Devices without LCD

152: Devices with LCD

**Pin count**

R = 64 pins

V = 100/104 pins

Z = 144 pins

Q = 132 pins

**Flash memory size**

E= 512 Kbytes of Flash memory

**Package**

H = BGA

T = LQFP

Y = WLCSP104

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

**Options**

No character = $V_{DD}$ range: 1.8 to 3.6 V and BOR enabled

D = $V_{DD}$ range: 1.65 to 3.6 V and BOR disabled

**Packing**

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.