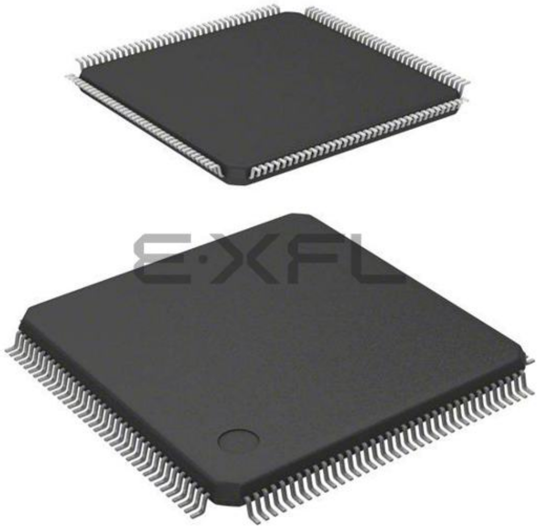

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	115
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152zet6d

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151xE and STM32L152xE ultra-low-power ARM® Cortex®-M3 based microcontroller product line. STM32L151xE and STM32L152xE devices are microcontrollers with a Flash memory density of 512 Kbytes.

The ultra-low-power STM32L151xE and STM32L152xE family includes devices in 5 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151xE and STM32L152xE microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, video intercom
- Utility metering

This STM32L151xE and STM32L152xE datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The application note “Getting started with STM32L1xxxx hardware development” (AN3216) gives a hardware implementation overview. Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M3 core please refer to the ARM® Cortex®-M3 technical reference manual, available from the www.arm.com website. *Figure 1* shows the general block diagram of the device family.

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From proprietary 8-bit to up to Cortex-M3, including the Cortex-M0+, the STM32Lx series are the best choice to answer the user needs, in terms of ultra-low-power features. The STM32 ultra-low-power series are the best fit, for instance, for gas/water meter, keyboard/mouse or fitness and healthcare, wearable applications. Several built-in features like LCD drivers, dual-bank memory, Low-power run mode, op-amp, AES 128-bit, DAC, USB crystal-less and many others will clearly allow to build very cost-optimized applications by reducing BOM.

Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lxxxxx and STM32Lxxxxx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, the old applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx, STM32L15xxx and STM32L162xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy.

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx and STM32L162xx family uses a common architecture:

- Same power supply range from 1.65 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 15 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 2 to 512 Kbytes

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.
- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.
- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}= V_{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151xE and STM32L152xE devices with up to 40 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs with up to 28 external channels in a group.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC’s runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Temperature sensor

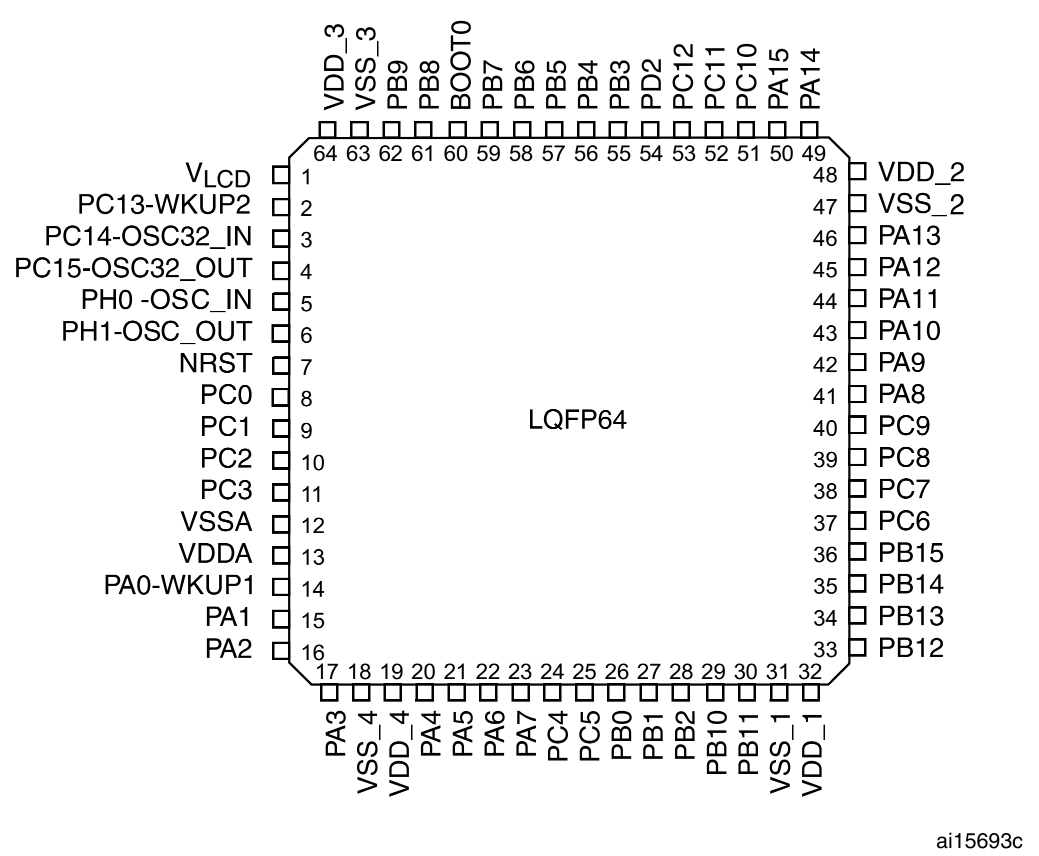
The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are

Figure 6. STM32L15xRE LQFP64 pinout



1. This figure shows the package top view.

Table 8. STM32L151xE and STM32L152xE pin definitions (continued)

Pins					Pin name	Pin Type[(1)]	I / O structure	Main function[(2)] (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP104					Alternate functions	Additional functions
16	F2	10	-	E8	V_{SS_5}	S		V_{SS_5}	-	-
17	G2	11	-	E9	V_{DD_5}	S		V_{DD_5}	-	-
18	G3	-	-	-	PF6	I/O	FT	PF6	TIM5_CH1/TIM5_ETR	ADC_IN27
19	G4	-	-	-	PF7	I/O	FT	PF7	TIM5_CH2	ADC_IN28/ COMP1_INP
20	H4	-	-	-	PF8	I/O	FT	PF8	TIM5_CH3	ADC_IN29/ COMP1_INP
21	J6	-	-	-	PF9	I/O	FT	PF9	TIM5_CH4	ADC_IN30/ COMP1_INP
22	-	-	-	-	PF10	I/O	FT	PF10	-	ADC_IN31/ COMP1_INP
23	F1	12	5	F8	PH0-OSC_IN[(5)]	I/O	TC	PH0	-	OSC_IN
24	G1	13	6	F9	PH1-OSC_OUT[(5)]	I/O	TC	PH1	-	OSC_OUT
25	H2	14	7	F7	NRST	I/O	RST	NRST	-	-
26	H1	15	8	F6	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ COMP1_INP
27	J2	16	9	H9	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP
28	-	17	10	G9	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
-	J3	-	-	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
-	K1	-	-	-	NC	I		NC	-	-
29	K2	18	11	G8	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP
30	J1	19	12	J9	V_{SSA}	S	-	V_{SSA}	-	-
31	-	20	-	H8	V_{REF-}	S	-	V_{REF-}	-	-
32	L1	21	-	G7	V_{REF+}	S	-	V_{REF+}	-	-
33	M1	22	13	G6	V_{DDA}	S	-	V_{DDA}	-	-

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number													
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	..	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PC7	-	-	TIM3_CH2	-	-	-	I2S3_MCK	-	-	-	SEG25	-	TIMx_IC4	EVENT OUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG26	-	TIMx_IC1	EVENT OUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG27	-	TIMx_IC2	EVENT OUT
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	USART3_TX	UART4_TX	-	COM4/ SEG28/ SEG40	-	TIMx_IC3	EVENT OUT
PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX	UART4_RX	-	COM5/ SEG29 /SEG41	-	TIMx_IC4	EVENT OUT
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	COM6/ SEG30/ SEG42	-	TIMx_IC1	EVENT OUT
PC13-WKUP2	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PC14 OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENT OUT
PC15 OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENT OUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS I2S2_WS	-	-	-	-	-	-	TIMx_IC1	EVENT OUT
PD1	-	-	-	-	-	SPI2 SCK I2S2_CK	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	COM7/ SEG31/ SEG43	-	TIMx_IC3	EVENT OUT
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	-	TIMx_IC4	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number													
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	..	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PF14	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF15	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG0	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG2	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG3	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG4	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG5	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG7	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG8	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG9	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG10	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG11	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 18. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max[1]	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = $f_{HCLK}/2$ above 16 MHz (PLL ON)[2]	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	200	470	µA
				2 MHz	360	780	
				4 MHz	685	1200	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.80	1.5	mA
				8 MHz	1.6	3	
				16 MHz	3.1	5	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	1.9	3.5	
				16 MHz	3.7	5.55	
				32 MHz	7.55	10.9	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	3.15	4.8	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	7.75	11.7	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	40	130	µA
		MSI clock, 524 kHz		524 kHz	115	215	
		MSI clock, 4.2 MHz		4.2 MHz	715	1100	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 23. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ	Max[(1)]	Unit
I_{DD} (Standby with RTC)	Supply current in Standby mode with RTC enabled	RTC clocked by LSI (no independent watchdog)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.865	-	µA
			T_A = -40 °C to 25 °C	1.11	1.9	
			T_A = 55 °C	1.72	2.2	
			T_A= 85 °C	2.12	4	
			T_A = 105 °C	2.54	8.3[(2)]	
		RTC clocked by LSE external quartz (no independent watchdog)[(3)]	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.97	-	
			T_A = -40 °C to 25 °C	1.28	-	
			T_A = 55 °C	2.01	-	
			T_A= 85 °C	2.5	-	
			T_A = 105 °C	2.98	-	
I_{DD} (Standby)	Supply current in Standby mode (RTC disabled)	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	1	1.7	
		Independent watchdog and LSI OFF	T_A = -40 °C to 25 °C	0.29	1	
			T_A = 55 °C	0.96	1.3	
			T_A = 85 °C	1.38	3	
			T_A = 105 °C	1.98	7[(2)]	
I_{DD} (WU from Standby)	Supply current during wakeup time from Standby mode	-	T_A = -40 °C to 25 °C	1	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 24. Peripheral current consumption(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	TIM2	12.0	10.0	8.0	10.0	µA/MHz (f_{HCLK})
	TIM3	10.5	8.8	7.0	8.8	
	TIM4	10.4	8.8	7.0	8.8	
	TIM5	13.8	11.5	9.1	11.5	
	TIM6	3.9	3.0	2.5	3.0	
	TIM7	3.8	3.3	2.6	3.3	
	LCD	4.2	3.6	2.8	3.6	
	WWDG	2.9	2.5	2.1	2.5	
	SPI2	5.4	4.4	3.5	4.4	
	SPI3	5.5	4.6	3.7	4.6	
	USART2	7.6	6.2	4.9	6.2	
	USART3	7.6	6.2	5.0	6.2	
	USART4	7.3	6.1	4.8	6.1	
	USART5	7.6	6.3	5.0	6.3	
	I2C1	7.3	6.1	4.8	6.1	
	I2C2	7.2	5.9	4.7	5.9	
	USB	13.0	11.2	8.9	11.2	
	PWR	2.6	2.3	1.9	2.3	
	DAC	5.9	5.0	4.0	5.0	
	COMP	3.9	3.3	2.6	3.3	

6.3.7 Internal clock source characteristics

The parameters given in *Table 30* are derived from tests performed under the conditions summarized in *Table 13*.

High-speed internal (HSI) RC oscillator

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	±0.4	0.7	%
		Trimming code is a multiple of 16	-	-	±1.5	%
$ACC_{HSI}^{(2)}$	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	$-1^{(3)}$	-	$1^{(3)}$	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI)}^{(2)}$	HSI oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI)}^{(2)}$	HSI oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Low-speed internal (LSI) RC oscillator

Table 31. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{LSI}^{(2)}$	LSI oscillator frequency drift $0°C \leq T_A \leq 105°C$	-10	-	4	%
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 32. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤ T_A ≤ 105 °C	-	±3	-	%
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤ V_{DD} ≤ 3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 37*. They are based on the EMS levels and classes defined in application note AN1709.

Table 37. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	4B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

Table 55. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S(5)	Sampling time	Direct channels $2.4\ V \le V_{DDA} \le 3.6\ V$	0.25	-	-	µs
		Multiplexed channels $2.4\ V \le V_{DDA} \le 3.6\ V$	0.56	-	-	
		Direct channels $1.8\ V \le V_{DDA} \le 2.4\ V$	0.56	-	-	
		Multiplexed channels $1.8\ V \le V_{DDA} \le 2.4\ V$	1	-	-	
		-	4	-	384	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	1	-	24.75	µs
		-	4 to 384 (sampling phase) +12 (successive approximation)			$1/f_{ADC}$
C_{ADC}	Internal sample and hold capacitor	Direct channels	-	16	-	pF
		Multiplexed channels	-		-	
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN}(6)	Signal source impedance		-	-	50	kΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

1. The Vref+ input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through VREF is composed of two parameters:

   - one constant (max 300 µA)

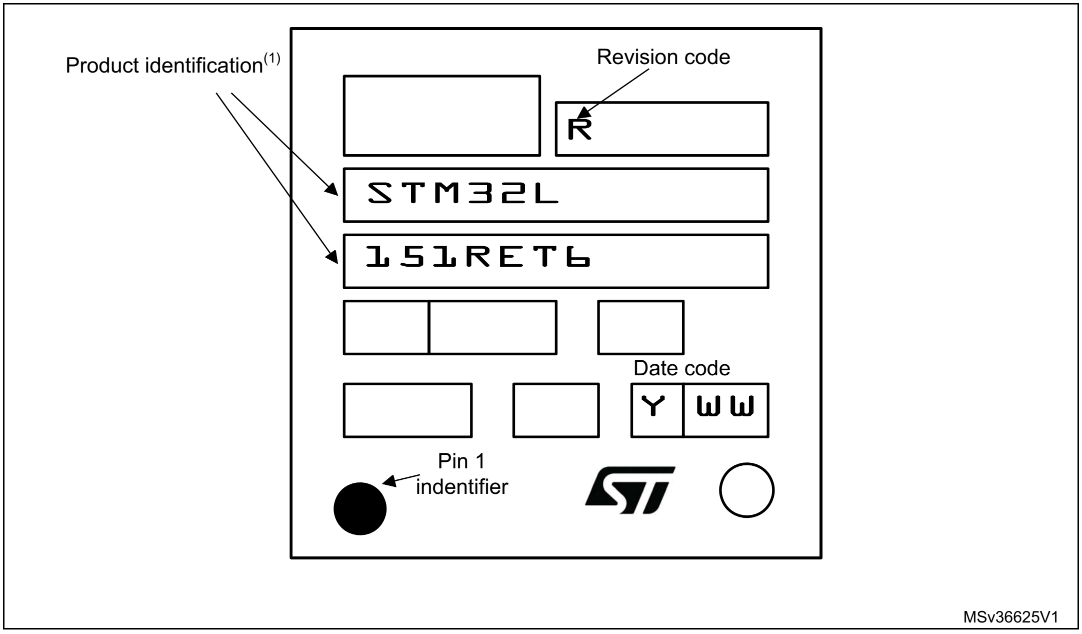
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses

   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. V_{SSA} or V_{REF-} must be tied to ground.
5. Minimum sampling time is reached for an external input impedance limited to a value as defined in *Table 57: Maximum source impedance RAIN max*.
6. External impedance has another high value limitation when using short sampling time as defined in *Table 57: Maximum source impedance RAIN max*.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

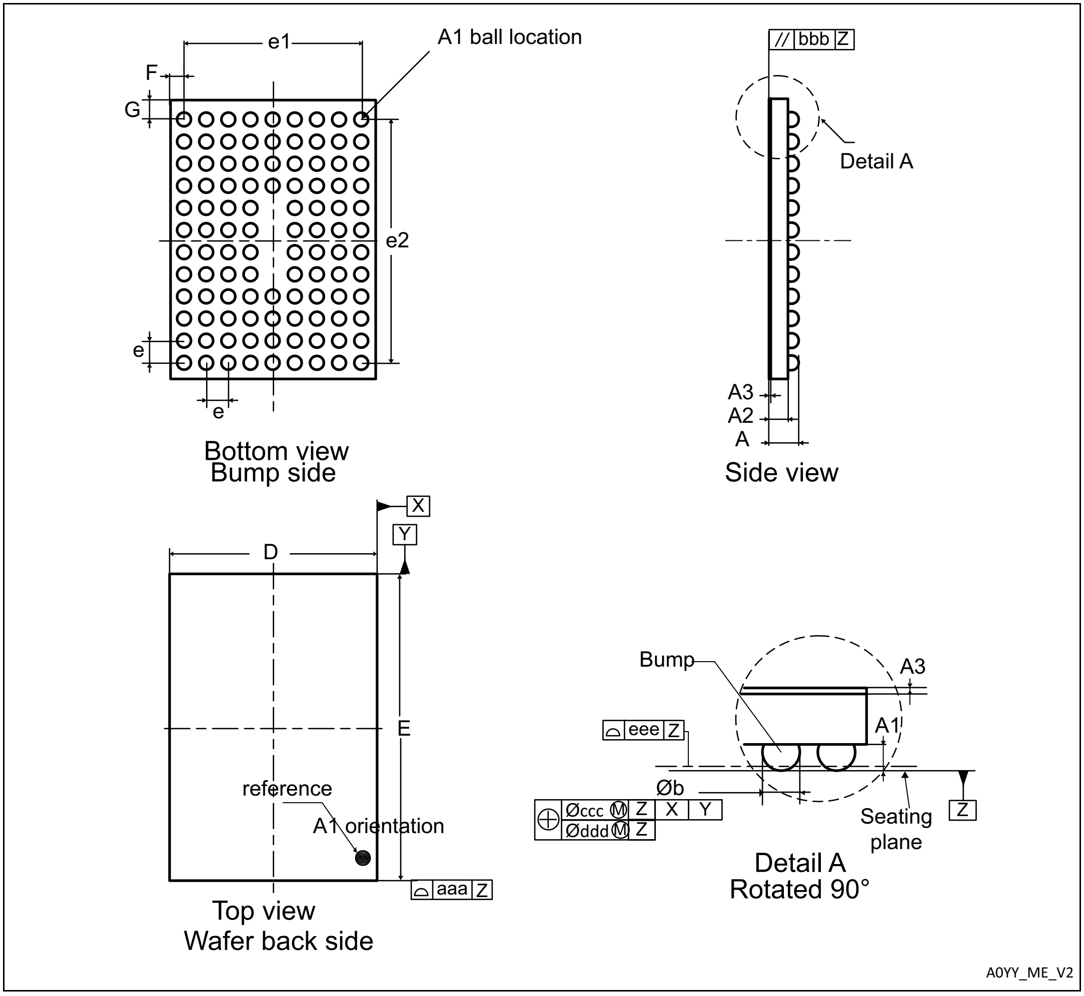
Figure 39. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

7.5 WLCSP104, 0.4 mm pitch wafer level chip scale package information

Figure 43. WLCSP104, 0.4 mm pitch wafer level chip scale package outline



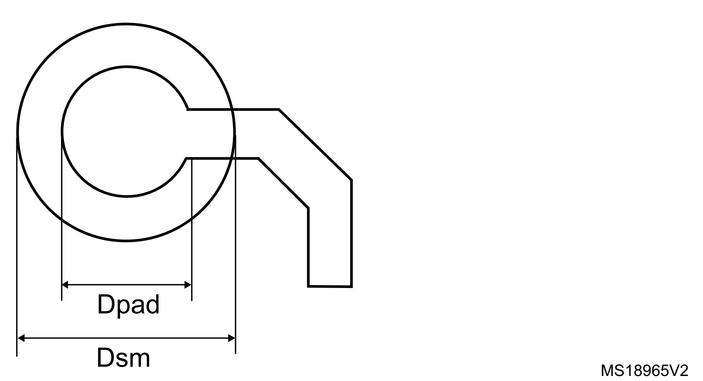
1. Drawing is not to scale.

Table 69. WLCSP104, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.023
A1	-	0.175	-	-	0.0069	-
A2	-	0.38	-	-	0.015	-
A3[2]	-	0.025	-	-	0.001	-
ø b[3]	0.22	0.25	0.28	0.0087	0.0098	0.011
D	4.06	4.095	4.13	0.1598	0.1612	0.1626
E	5.059	5.094	5.129	0.1992	0.2006	0.2019
e	-	0.4	-	-	0.0157	-
e1	-	3.2	-	-	0.126	-
e2	-	4.4	-	-	0.1732	-
F	-	0.447	-	-	0.0176	-
G	-	0.347	-	-	0.0137	-
aaa	-	-	0.1	-	-	0.0039
bbb	-	-	0.1	-	-	0.0039
ccc	-	-	0.1	-	-	0.0039
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 44. WLCSP104, 0.4 mm pitch wafer level chip scale package recommended footprint



8 Part numbering

Table 72. STM32L151xE and STM32L152xE Ordering information scheme

Example: STM32 L 151 R E T 6 D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low-power

Device subfamily

151: Devices without LCD
152: Devices with LCD

Pin count

R = 64 pins
V = 100/104 pins
Z = 144 pins
Q = 132 pins

Flash memory size

E= 512 Kbytes of Flash memory

Package

H = BGA
T = LQFP
Y = WLCSP104

Temperature range

6 = Industrial temperature range, –40 to 85 °C
7 = Industrial temperature range, –40 to 105 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled
D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel
No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the nearest ST sales office.