Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

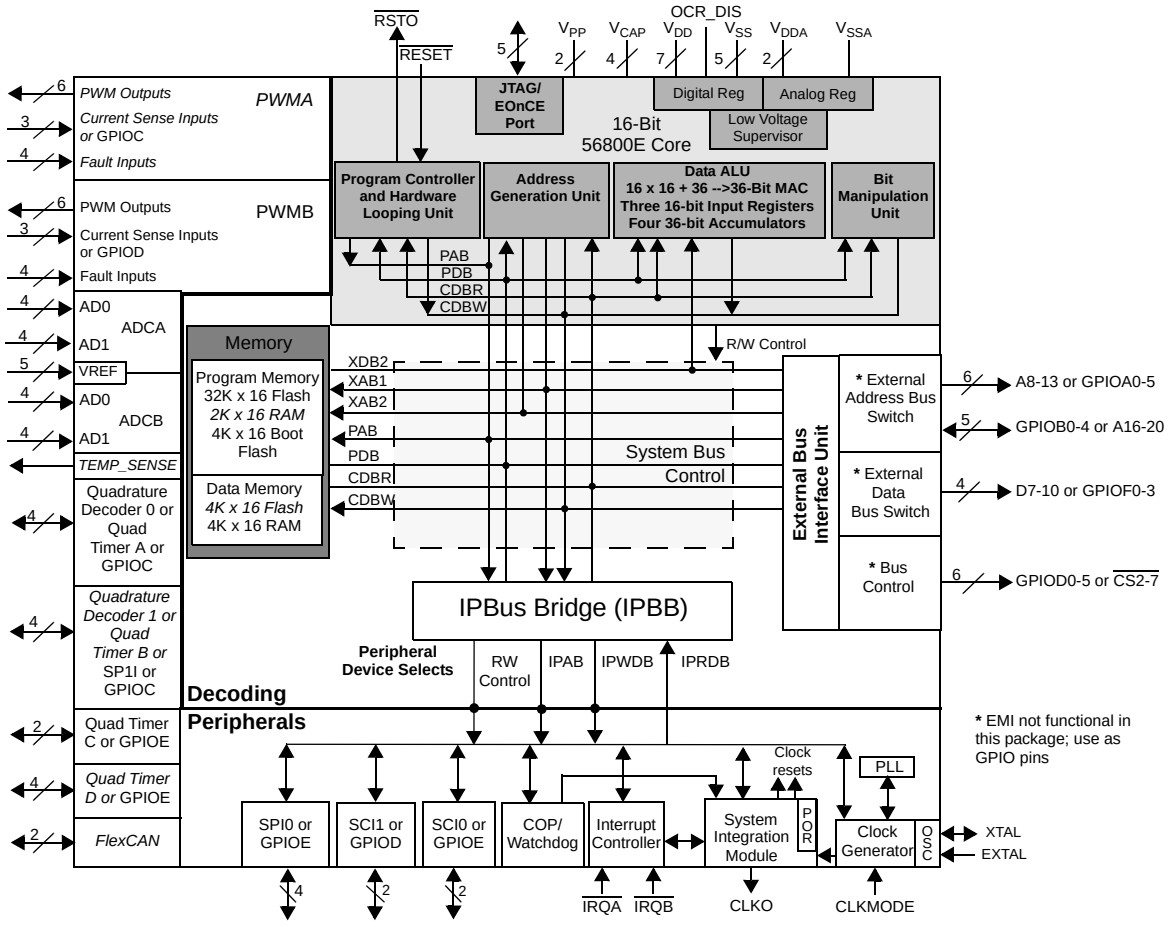
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	49
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8335mfge

56F8335/56F8135 General Description

Note: *Features in italics are NOT available in the 56F8135 device.*

- Up to 60 MIPS at 60MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- 64KB Program Flash
- *4KB Program RAM*
- *8KB Data Flash*
- 8KB Data RAM
- 8KB Boot Flash
- Up to two 6-channel PWM modules
- Four 4-channel, 12-bit ADCs
- *Temperature Sensor*
- *Up to two* Quadrature Decoders
- *FlexCAN module*
- Optional On-Chip Regulator
- Two Serial Communication Interfaces (SCIs)
- Up to two Serial Peripheral Interface (SPIs)
- Up to four general-purpose Quad Timers
- Computer Operating Properly (COP)/Watchdog
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Up to 49 GPIO lines
- 128-pin LQFP Package



56F8335/56F8135 Block Diagram - 128 LQFP

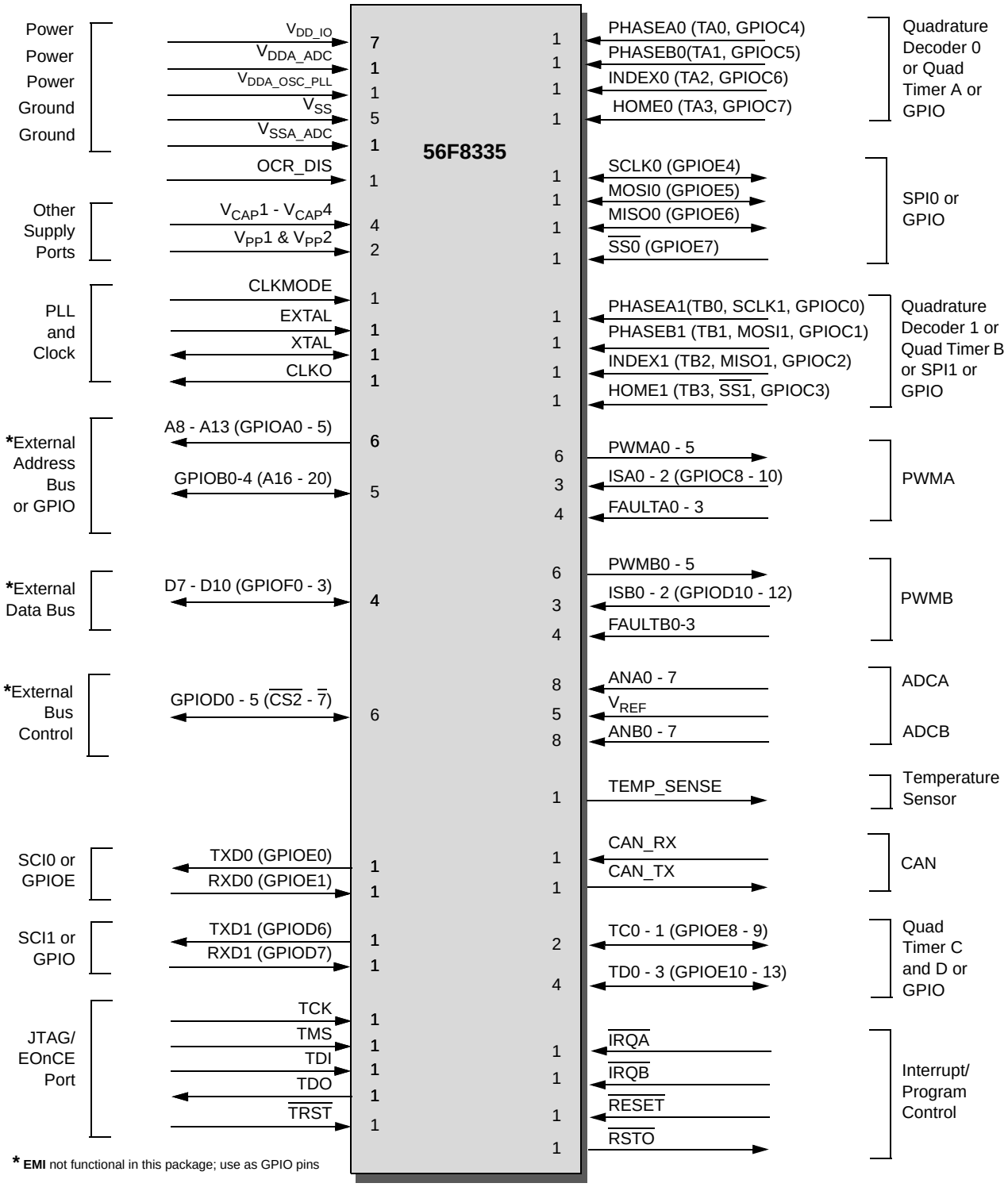


Figure 2-1 56F8335 Signals Identified by Functional Group[1] (128-Pin LQFP)

1. Alternate pin functionality is shown in parenthesis; pin direction/type shown is the default functionality.

Table 2-2 Signal and Package Information for the 128-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
CLKO	6	Output	In reset, output is disabled	**Clock Output** — This pin outputs a buffered clock signal. Using the SIM CLKO Select Register (SIM_CLKOSR), this pin can be programmed as any of the following: disabled, CLK_MSTR (system clock), IPBus clock, oscillator output, prescaler clock and postscaler clock. Other signals are also available for test purposes. See **Part 6.5.7** for details.
A8 **(GPIOA0)**	15	Output Schmitt Input/ Output	In reset, output is disabled, pull-up is enabled	**Address Bus** — A8 - A13 specify six of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A8 - A13 and EMI control signals are tri-stated when the external bus is inactive. **Port A GPIO** — These six GPIO pins can be individually programmed as input or output pins. After reset, these pins default to address bus functionality and must be programmed as GPIO. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOA_PUR register. Example: GPIOA0, clear bit 0 in the GPIOA_PUR register. **Note:** Primary function is not available in this package configuration; GPIO function must be used instead.
A9 (GPIOA1)	16			
A10 (GPIOA2)	17			
A11 (GPIOA3)	18			
A12 (GPIOA4)	19			
A13 (GPIOA5)	20			
GPIOB0 **(A16)**	27	Schmitt Input/ Output Output	Input, pull-up enabled	**Port B GPIO** — These four GPIO pins can be individually programmed as an input or output pin. **Address Bus** — A16 - A19 specify four of the address lines for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), A16 - A19 and EMI control signals are tri-stated when the external bus is inactive. After reset, the default state is GPIO. To deactivate the internal pull-up resistor, clear bit 0 in the GPIOB_PUR register. Example: GPIOB1, clear bit 1 in the GPIOB_PUR register.
GPIOB1 **(A17)**	28			
GPIOB2 **(A18)**	29			
GPIOB3 **(A19)**	30			

Table 2-2 Signal and Package Information for the 128-Pin LQFP (Continued)

Signal Name	Pin No.	Type	State During Reset	Signal Description
ANB0	96	Input	Analog Input	**ANB0 - 3** — Analog inputs to ADC B, channel 0
ANB1	97			
ANB2	98			
ANB3	99			
ANB4	100	Input	Analog Input	**ANB4 - 7** — Analog inputs to ADC B, channel 1
ANB5	101			
ANB6	102			
ANB7	103			
TEMP_ SENSE	88	Output	Analog Output	**Temperature Sense Diode** — This signal connects to an on-chip diode that can be connected to one of the ADC inputs and is used to monitor the temperature of the die. Must be bypassed with a 0.01 μF capacitor.
CAN_RX	121	Schmitt Input	Input, pull-up enabled	**FlexCAN Receive Data** — This is the CAN input. This pin has an internal pull-up resistor. To deactivate the internal pull-up resistor, set the CAN bit in the SIM_PUDR register.
CAN_TX	120	Open Drain Output	Open Drain Output	**FlexCAN Transmit Data** — CAN output with internal pull-up enable at reset.* * **Note**: If a pin is configured as open drain output mode, internal pull-up will automatically be disabled when it outputs low. Internal pull-up will be enabled unless it has been manually disabled by clearing the corresponding bit in the PUREN register of the GPIO module, when it outputs high. If a pin is configured as push-pull output mode, internal pull-up will automatically be disabled, whether it outputs low or high.
TC0 **(GPIOE8)**	111	Schmitt Input/ Output Schmitt Input/ Output	Input, pull-up enabled	**TC0 - 1** — Timer C, Channels 0 and 1 **Port E GPIO** — These GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Timer functionality. To deactivate the internal pull-up resistor, clear the appropriate bit of the GPIOE_PUR register. See **Part 6.5.6** for details.
TC1 (GPIOE9)	113			

1. Setting this bit can cause unpredictable results and is not recommended, since the EMI is not functional in this package.

Table 4-4 shows the memory map options of the 56F8335/56F8135. The two right columns cannot be used, since the EMI pins are not provided in the package; therefore, only the Mode 0 column is relevant.

Note: *Program RAM is NOT available on the 56F8135 device.*

Table 4-4 Program Memory Map at Reset

<table>
<tr><th rowspan="3">Begin/End Address</th><th>Mode 0 (MA = 0)</th><th colspan="2">Mode 1[1] (MA = 1)</th></tr>
<tr><th>Internal Boot</th><th colspan="2">External Boot</th></tr>
<tr><th>Internal Boot
16-Bit External Address Bus</th><th>EMI_MODE = 0[2, 3]
16-Bit External Address Bus</th><th>EMI_MODE = 1[4]
20-Bit External Address Bus</th></tr>
<tr><td>P:$1F FFFF
P:$10 0000</td><td rowspan="2">External Program Memory[5]</td><td rowspan="2">External Program Memory[5]</td><td>External Program Memory[5]</td></tr>
<tr><td>P:$0F FFFF
P:$03 0000</td><td rowspan="9">External Program RAM[5]
COP Reset Address = 02 0002
Boot Location = 02 0000</td></tr>
<tr><td>P:$02 FFFF
P:$02 F800</td><td>On-Chip Program RAM
4KB</td><td>On-Chip Program RAM
4KB</td></tr>
<tr><td>P:$02 F7FF
P:$02 1000</td><td colspan="2">Reserved
116KB</td></tr>
<tr><td>P:$02 0FFF
P:$02 0000</td><td>Boot Flash
8KB
COP Reset Address = 02 0002
Boot Location = 02 0000</td><td>Boot Flash
8KB
(Not Used for Boot in this Mode)</td></tr>
<tr><td>P:$01 FFFF
P:$01 8000</td><td rowspan="2">External Program RAM[5]</td><td>Reserved
64KB</td></tr>
<tr><td>P:$01 7FFF
P:$01 0000</td><td>Internal Program Flash
64KB</td></tr>
<tr><td>P:$00 FFFF
P:$00 8000</td><td>Reserved
64KB</td><td rowspan="2">External Program RAM[5]
COP Reset Address = 00 0002
Boot Location = 00 0000</td></tr>
<tr><td>P:$00 7FFF
P:$00 0000</td><td>Internal Program Flash
64KB</td></tr>
</table>

1. Cannot be used since MA = EXTBOOT = 0 and the EMI is not available; information in shaded areas not applicable to 56F8335/56F8135.
2. This mode provides maximum compatibility with 56F80x parts while operating externally.
3. “EMI_MODE = 0”, EMI_MODE pin is tied to ground at boot up.
4. “EMI_MODE = 1”, EMI_MODE pin is tied to V_{DD} at boot up.
5. Not accessible in this part, since the EMI is not fully pinned out in this package; information in shaded areas not applicable to 56F8335/56F8135.

4.3 Interrupt Vector Table

Table 4-5 provides the reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. The priority of an interrupt can be assigned to different levels, as indicated, allowing some control over

Table 4-9 Data Memory Peripheral Base Address Map Summary (Continued)

Peripheral	Prefix	Base Address	Table Number
GPIO Port C	GPIOC	X:$00 F310	4-31
GPIO Port D	GPIOD	X:$00 F320	4-32
GPIO Port E	GPIOE	X:$00 F330	4-33
GPIO Port F	GPIOF	X:$00 F340	4-34
SIM	SIM	X:$00 F350	4-35
Power Supervisor	LVI	X:$00 F360	4-36
FM	FM	X:$00 F400	4-37
FlexCAN	FC	X:$00 F800	4-38

Table 4-12 Quad Timer B Registers Address Map (Continued)
(TMRB_BASE = $00 F080)
Quad Timer B is NOT available in the 56F8135 device

Register Acronym	Address Offset	Register Description
TMRB1_CTRL	$16	Control Register
TMRB1_SCR	$17	Status and Control Register
TMRB1_CMPLD1	$18	Comparator Load Register 1
TMRB1_CMPLD2	$19	Comparator Load Register 2
TMRB1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRB2_CMP1	$20	Compare Register 1
TMRB2_CMP2	$21	Compare Register 2
TMRB2_CAP	$22	Capture Register
TMRB2_LOAD	$23	Load Register
TMRB2_HOLD	$24	Hold Register
TMRB2_CNTR	$25	Counter Register
TMRB2_CTRL	$26	Control Register
TMRB2_SCR	$27	Status and Control Register
TMRB2_CMPLD1	$28	Comparator Load Register 1
TMRB2_CMPLD2	$29	Comparator Load Register 2
TMRB2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRB3_CMP1	$30	Compare Register 1
TMRB3_CMP2	$31	Compare Register 2
TMRB3_CAP	$32	Capture Register
TMRB3_LOAD	$33	Load Register
TMRB3_HOLD	$34	Hold Register
TMRB3_CNTR	$35	Counter Register
TMRB3_CTRL	$36	Control Register
TMRB3_SCR	$37	Status and Control Register
TMRB3_CMPLD1	$38	Comparator Load Register 1
TMRB3_CMPLD2	$39	Comparator Load Register 2
TMRB3_COMSCR	$3A	Comparator Status and Control Register

Table 4-14 Quad Timer D Registers Address Map (Continued)
(TMRD_BASE = $00 F100)
Quad Timer D is NOT available in the 56F8135 device

Register Acronym	Address Offset	Register Description
TMRD1_CAP	$12	Capture Register
TMRD1_LOAD	$13	Load Register
TMRD1_HOLD	$14	Hold Register
TMRD1_CNTR	$15	Counter Register
TMRD1_CTRL	$16	Control Register
TMRD1_SCR	$17	Status and Control Register
TMRD1_CMPLD1	$18	Comparator Load Register 1
TMRD1_CMPLD2	$19	Comparator Load Register 2
TMRD1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRD2_CMP1	$20	Compare Register 1
TMRD2_CMP2	$21	Compare Register 2
TMRD2_CAP	$22	Capture Register
TMRD2_LOAD	$23	Load Register
TMRD2_HOLD	$24	Hold Register
TMRD2_CNTR	$25	Counter Register
TMRD2_CTRL	$26	Control Register
TMRD2_SCR	$27	Status and Control Register
TMRD2_CMPLD1	$28	Comparator Load Register 1
TMRD2_CMPLD2	$29	Comparator Load Register 2
TMRD2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRD3_CMP1	$30	Compare Register 1
TMRD3_CMP2	$31	Compare Register 2
TMRD3_CAP	$32	Capture Register
TMRD3_LOAD	$33	Load Register
TMRD3_HOLD	$34	Hold Register
TMRD3_CNTR	$35	Counter Register
TMRD3_CTRL	$36	Control Register
TMRD3_SCR	$37	Status and Control Register
TMRD3_CMPLD1	$38	Comparator Load Register 1
TMRD3_CMPLD2	$39	Comparator Load Register 2
TMRD3_COMSCR	$3A	Comparator Status and Control Register

Table 4-38 FlexCAN Registers Address Map (Continued) (FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8135 device

Register Acronym	Address Offset	Register Description
FCMB13_DATA	$AB	Message Buffer 13 Data Register
FCMB13_DATA	$AC	Message Buffer 13 Data Register
FCMB13_DATA	$AD	Message Buffer 13 Data Register
FCMB13_DATA	$AE	Message Buffer 13 Data Register
		Reserved
FCMB14_CONTROL	$B0	Message Buffer 14 Control / Status Register
FCMB14_ID_HIGH	$B1	Message Buffer 14 ID High Register
FCMB14_ID_LOW	$B2	Message Buffer 14 ID Low Register
FCMB14_DATA	$B3	Message Buffer 14 Data Register
FCMB14_DATA	$B4	Message Buffer 14 Data Register
FCMB14_DATA	$B5	Message Buffer 14 Data Register
FCMB14_DATA	$B6	Message Buffer 14 Data Register
		Reserved
FCMB15_CONTROL	$B8	Message Buffer 15 Control / Status Register
FCMB15_ID_HIGH	$B9	Message Buffer 15 ID High Register
FCMB15_ID_LOW	$BA	Message Buffer 15 ID Low Register
FCMB15_DATA	$BB	Message Buffer 15 Data Register
FCMB15_DATA	$BC	Message Buffer 15 Data Register
FCMB15_DATA	$BD	Message Buffer 15 Data Register
FCMB15_DATA	$BE	Message Buffer 15 Data Register
		Reserved

5.6.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2.2 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.3 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.4 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

Two examples of FM_CLKDIV calculations follow.

EXAMPLE 1: If the system clock is the 8MHz crystal frequency because the PLL has not been set up, the input clock will be below 12.8MHz, so PRDIV8 = FM_CLKDIV[6] = 0. Using the following equation yields a DIV value of 19 for a clock of 200kHz, and a DIV value of 20 for a clock of 190kHz. This translates into an FM_CLKDIV[6:0] value of $13 or $14, respectively.

$$150[\text{kHz}] < \frac{\left(\frac{\text{SYS\_CLK}}{(2)}\right)}{(\text{DIV} + 1)} < 200[\text{kHz}]$$

EXAMPLE 2: In this example, the system clock has been set up with a value of 32MHz, making the FM input clock 16MHz. Because that is greater than 12.8MHz, PRDIV8 = FM_CLKDIV[6] = 1. Using the following equation yields a DIV value of 9 for a clock of 200kHz, and a DIV value of 10 for a clock of 181kHz. This translates to an FM_CLKDIV[6:0] value of $49 or $4A, respectively.

$$150[\text{kHz}] < \frac{\left(\frac{\text{SYS\_CLK}}{(2)}\right)}{(\text{DIV} + 1)} < 200[\text{kHz}]$$

Once the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, the user must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence has completed. For details, see the JTAG Section in the **56F8300 Peripheral User Manual**.

Note: When the lockout recovery sequence has completed, the user must reset both the JTAG TAP controller (by asserting $\overline{\text{TRST}}$) and the device (by asserting external chip reset) to return to normal unsecured operation.

7.2.4 Product Analysis

The recommended method of unsecuring a programmed device for product analysis of field failures is via the backdoor key access. The customer would need to supply Technical Support with the backdoor key and the protocol to access the backdoor routine in the Flash. Additionally, the KEYEN bit that allows backdoor key access must be set.

An alternative method for performing analysis on a secured hybrid controller would be to mass-erase and reprogram the Flash with the original code, but to modify the security bytes.

To insure that a customer does not inadvertently lock himself out of the device during programming, it is recommended that he program the backdoor access key first, his application code second, and the security bytes within the FM configuration field last.

Table 8-3 GPIO External Signals Map

Pins in shaded rows are not available in 56F8335 / 56F8135

Pins in italics are NOT available in the 56F8135 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin #
GPIOA	0	Peripheral	A8[1]	15
	1	Peripheral	A9[1]	16
	2	Peripheral	A10[1]	17
	3	Peripheral	A11[1]	18
	4	Peripheral	A12[1]	19
	5	Peripheral	A13[1]	20
	6	N/A		
	7	N/A		
	8	N/A		
	9	N/A		
	10	N/A		
	11	N/A		
	12	N/A		
	13	N/A		
GPIOB	0	GPIO	A16[1]	27
	1	GPIO	A17[1]	28
	2	GPIO	A18[1]	29
	3	GPIO	A19[1]	30
	4	GPIO	A20 / Prescaler_clock	31
	5	N/A		
	6	N/A		
	7	N/A		

Table 8-3 GPIO External Signals Map (Continued)

Pins in shaded rows are not available in 56F8335 / 56F8135

Pins in italics are NOT available in the 56F8135 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package Pin #
GPIOE	0	Peripheral	TXD0	7
	1	Peripheral	RXD0	8
	2	N/A		
	3	N/A		
	4	Peripheral	SCLK0	124
	5	Peripheral	MOSI0	126
	6	Peripheral	MISO0	125
	7	Peripheral	$\overline{SS0}$	123
	8	Peripheral	TC0	111
	9	Peripheral	TC1	113
	10	Peripheral	*TD0*	107
	11	Peripheral	*TD1*	108
	12	Peripheral	*TD2*	109
	13	Peripheral	*TD3*	110

Part 10 Specifications

10.1 General Characteristics

The 56F8335/56F8135 are fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Note: All specifications meet both Automotive and Industrial requirements unless individual specifications are listed.

Note: *The 56F8135 device is guaranteed to 40MHz and specified to meet Industrial requirements only.*

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Note: *The 56F8135 device is specified to meet Industrial requirements only; CAN is NOT available on the 56F8135 device.*

Table 10-1 Absolute Maximum Ratings

(V_{SS} = V_{SSA_ADC} = 0)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply voltage	V_{DD_IO}		- 0.3	4.0	V
ADC Supply Voltage	V_{DDA_ADC}, V_{REFH}	V_{REFH} must be less than or equal to V_{DDA_ADC}	- 0.3	4.0	V
Oscillator / PLL Supply Voltage	$V_{DDA\_OSC\_PLL}$		- 0.3	4.0	V
Internal Logic Core Supply Voltage	V_{DD_CORE}	OCR_DIS is High	- 0.3	3.0	V
Input Voltage (digital)	V_{IN}	Pin Groups 1, 2, 5, 6, 9, 10	-0.3	6.0	V

Table 10-10. PLL Parameters

Characteristics	Symbol	Min	Typical	Max	Unit
PLL Start-up time	T_{PS}	0.3	0.5	10	ms
Resonator Start-up time	T_{RS}	0.1	0.18	1	ms
Min-Max Period Variation	T_{PV}	120	—	200	ps
Peak-to-Peak Jitter	T_{PJ}	—	—	175	ps
Bias Current	I_{BIAS}	—	1.5	2	mA
Quiescent Current, power-down mode	I_{PD}	—	100	150	μA

10.2.1 Temperature Sense

Note: *Temperature Sensor is NOT available in the 56F8135 device.*

Table 10-11 Temperature Sense Parametrics

Characteristics	Symbol	Min	Typical	Max	Unit
Slope (Gain)[1]	m	—	7.762	—	mV/°C
Room Trim Temp. [1, 2]	T_{RT}	24	26	28	°C
Hot Trim Temp. (Industrial)[1,2]	T_{HT}	122	125	128	°C
Hot Trim Temp. (Automotive)[1,2]	T_{HT}	147	150	153	°C
Output Voltage @ V_{DDA_ADC} = 3.3V, T_J =0°C[1]	V_{TS0}	—	1.370	—	V
Supply Voltage	V_{DDA_ADC}	3.0	3.3	3.6	V
Supply Current - OFF	I_{DD-OFF}	—	—	10	μA
Supply Current - ON	I_{DD-ON}	—	—	250	μA
Accuracy[3,1] from -40°C to 150°C Using V_{TS} = mT + V_{TS0}	T_{ACC}	-6.7	0	6.7	°C
Resolution[4, 5,1]	R_{ES}	—	0.104	—	°C / bit

1. Includes the ADC conversion of the analog Temperature Sense voltage.
2. The ADC is not calibrated for the conversion of the Temperature Sensor trim value stored in the Flash Memory at FMOPT0 and FMOPT1.
3. See Application Note, AN1980, for methods to increase accuracy.
4. Assuming a 12-bit range from 0V to 3.3V.
5. Typical resolution calculated using equation,

Table 10-17 SPI Timing[1] (Continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	10-9, 10-10, 10-11
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	10-9, 10-10, 10-11, 10-12
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	10-9, 10-10, 10-11, 10-12

1. Parameters listed are guaranteed by design.

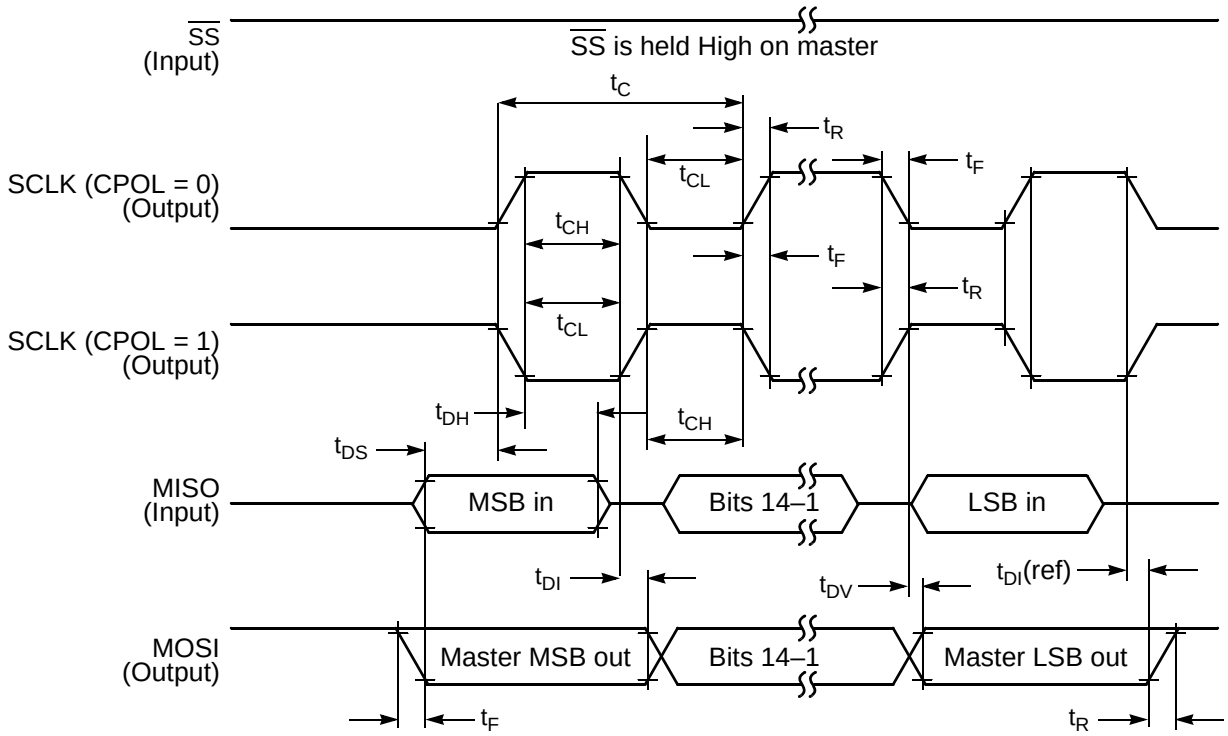


Figure 10-9 SPI Master Timing (CPHA = 0)

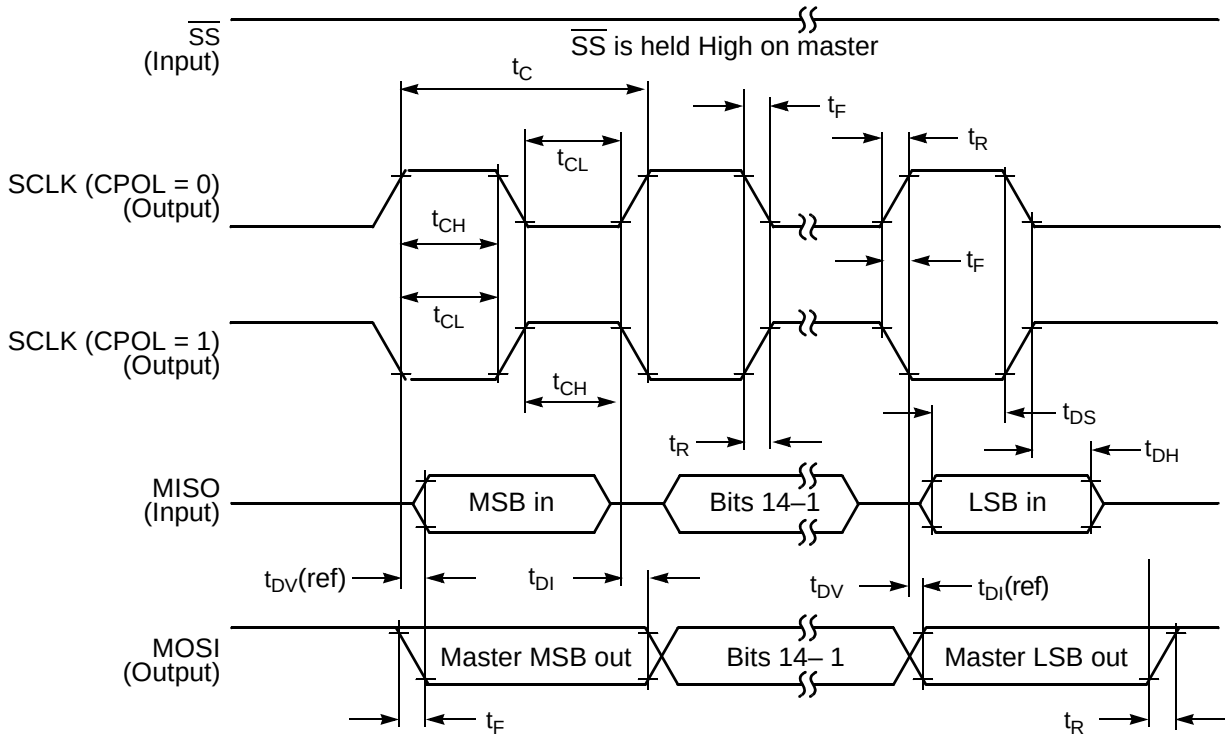


Figure 10-10 SPI Master Timing (CPHA = 1)

10.15 Analog-to-Digital Converter (ADC) Parameters

Table 10-23 ADC Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltages	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[1]	INL	—	+/- 2.4	+/- 3.2	LSB[2]
Differential Non-Linearity	DNL	—	+/- 0.7	< +1	LSB[2]
Monotonicity	GUARANTEED				
ADC internal clock	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC channel power-up time	t_{ADPU}	5	6	16	t_{AIC} cycles[3]
ADC reference circuit power-up time[4]	t_{VREF}	—	—	25	ms
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Input capacitance	C_{ADI}	—	5	—	pF
Input injection current[5], per pin	I_{ADI}	—	—	3	mA
Input injection current, total	I_{ADIT}	—	—	20	mA
V_{REFH} current	I_{VREFH}	—	1.2	3	mA
ADC A current	I_{ADCA}	—	25	—	mA
ADC B current	I_{ADCB}	—	25	—	mA
Quiescent current	I_{ADCQ}	—	0	10	μA
Uncalibrated Gain Error (ideal = 1)	E_{GAIN}	—	+/- .004	+/- .01	—
Uncalibrated Offset Voltage	V_{OFFSET}	—	+/- 18	+/- 46	mV
Calibrated Absolute Error[6]	AE_{CAL}	—	See **Figure 10-21**	—	LSBs
Calibration Factor 1[7]	CF1	—	-0.003141	—	—
Calibration Factor 2[7]	CF2	—	-17.6	—	—
Crosstalk between channels	—	—	-60	—	dB
Common Mode Voltage	V_{common}	—	$(V_{REFH} - V_{REFLO}) / 2$	—	V
Signal-to-noise ratio	SNR	—	64.6	—	db

Please see **www.freescale.com** for the most current case outline.

Part 12 Design Considerations

12.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single-layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = Package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = Package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = Thermocouple temperature on top of package (^oC)

Ψ_{JT} = Thermal characterization parameter (^{o}C)/W
P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8335/56F8135:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead