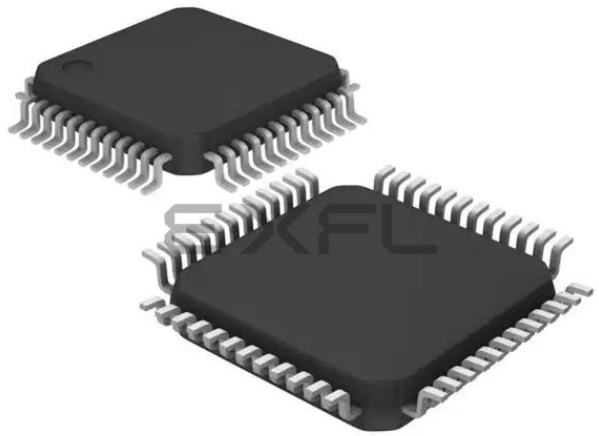

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	42
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc131lc2ae

4.3 Pin Configuration

4.3.1 NuMicro™ NUC131 Pin Diagram

*4.3.1.1 NuMicro™ NUC131SxxAE LQFP 64 pin (7 mm * 7mm)*

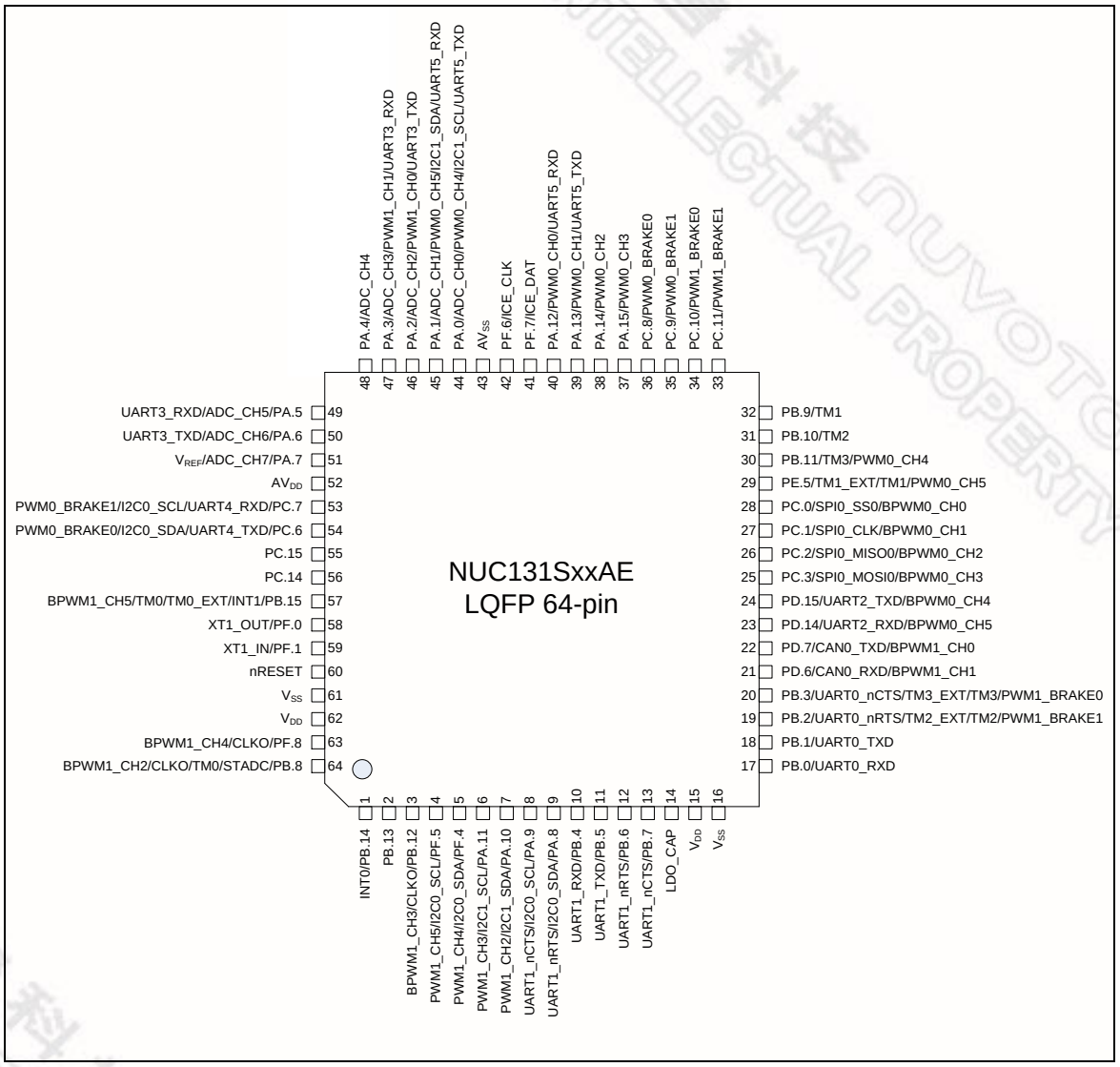


Figure 4-2 NuMicro™ NUC131SxxAE LQFP 64-pin Diagram

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		BPWM0_CH4	I/O	BPWM0 CH4 input/Capture input.
25	21	PC.3	I/O	General purpose digital I/O pin.
		SPI0_MOSI0	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		BPWM0_CH3	O	BPWM0 CH3 input/Capture input.
26	22	PC.2	I/O	General purpose digital I/O pin.
		SPI0_MISO0	I/O	SPI0 MISO (Master In, Slave Out) pin.
		BPWM0_CH2	I	BPWM0 CH2 input/Capture input.
27	23	PC.1	I/O	General purpose digital I/O pin.
		SPI0_CLK	I/O	SPI0 serial clock pin.
		BPWM0_CH1	I/O	BPWM0 CH1 input/Capture input.
28	24	PC.0	I/O	General purpose digital I/O pin.
		SPI0_SS0	I/O	SPI0 slave select pin.
		BPWM0_CH0	I/O	BPWM0 CH0 input/Capture input.
29		PE.5	I/O	General purpose digital I/O pin.
		PWM0_CH5	I/O	PWM0 CH5 output/Capture input.
		TM1_EXT	I	Timer1 external capture input pin.
		TM1	O	Timer1 toggle output pin.
30		PB.11	I/O	General purpose digital I/O pin.
		TM3	I/O	Timer3 event counter input / toggle output.
		PWM0_CH4	I/O	PWM0 CH4 output/Capture input.
31		PB.10	I/O	General purpose digital I/O pin.
		TM2	I/O	Timer2 event counter input / toggle output.
32		PB.9	I/O	General purpose digital I/O pin.
		TM1	I/O	Timer1 event counter input / toggle output.
33		PC.11	I/O	General purpose digital I/O pin.
		PWM1_BRAKE1	I	PWM1 brake input pin.
34		PC.10	I/O	General purpose digital I/O pin.
		PWM1_BRAKE0	I	PWM1 brake input pin.
35		PC.9	I/O	General purpose digital I/O pin.
		PWM0_BRAKE1	I	PWM0 brake input pin.
36		PC.8	I/O	General purpose digital I/O pin.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
60	46	nRESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
61		V_{SS}	**P**	Ground pin for digital circuit.
62		V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
63	47	PF.8	**I/O**	General purpose digital I/O pin.
		CLKO	**O**	Frequency divider clock output pin.
		BPWM1_CH4	**I/O**	BPWM1 CH4 output/Capture input.
64	48	PB.8	**I/O**	General purpose digital I/O pin.
		STADC	**I**	ADC external trigger input.
		TM0	**I/O**	Timer0 event counter input / toggle output.
		CLKO	**O**	Frequency divider clock output pin.
		BPWM1_CH2	**I/O**	BPWM1 CH2 output/Capture input.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

(WFE) instructions, or the return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Power-on Reset
- Low level on the nRESET pin
- Watchdog Time-out Reset
- Low Voltage Reset
- Brown-out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-on Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-on Reset is external crystal circuit and BS (ISPCON[1]) bit. System Reset does not reset external crystal circuit and BS (ISPCON[1]) bit, but Power-on Reset does.

6.2.4 System Memory Map

The NuMicro™ NUC131 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripheral. The NuMicro™ NUC131 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_0FFF	FLASH_BA	FLASH Memory Space (68 KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (8 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	BPWM0_BA	BPWM0 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4005_4000 – 0x4005_7FFF	UART3_BA	UART3 Control Registers
0x4005_8000 – 0x4005_BFFF	UART4_BA	UART4 Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4014_0000 – 0x4014_3FFF	PWM1_BA	PWM1 Control Registers
0x4014_4000 – 0x4014_7FFF	BPWM1_BA	BPWM1 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4015_8000 – 0x4015_BFFF	UART5_BA	UART5 Control Registers
0x4018_0000 – 0x4018_3FFF	CAN0_BA	CAN0 Bus Control Registers

6.2.6.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-4 Vector Table Format

6.2.6.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

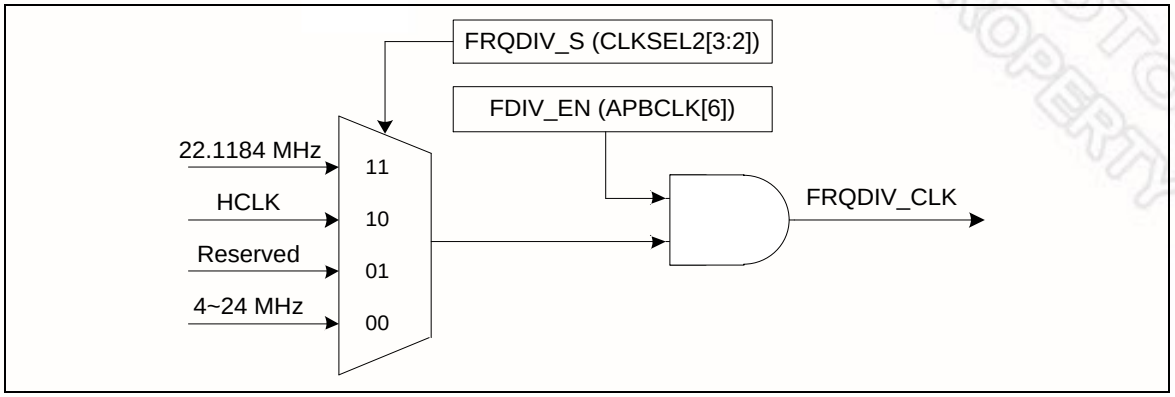


Figure 6-7 Clock Source of Frequency Divider

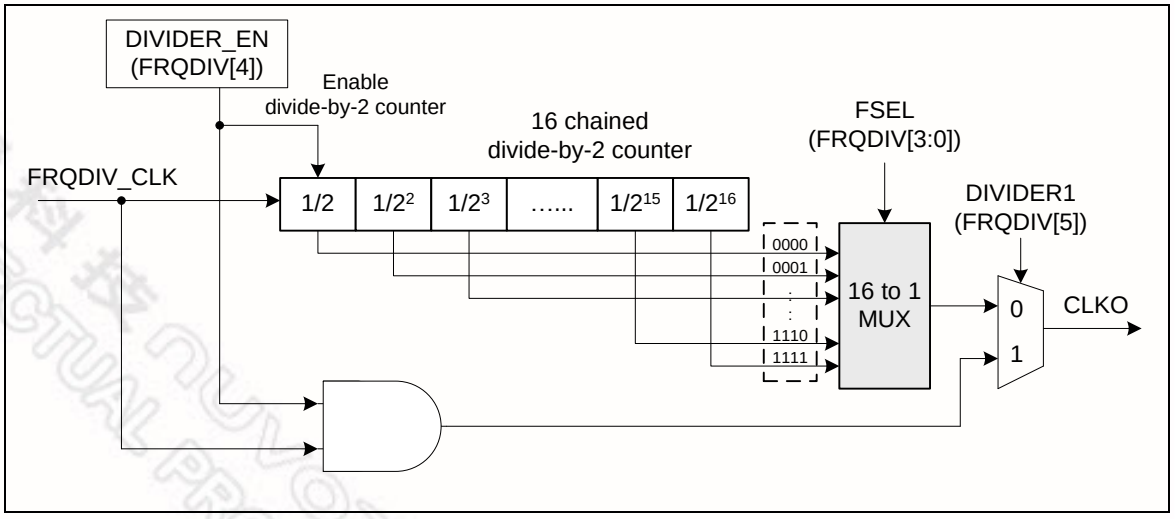


Figure 6-8 Frequency Divider Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro™ NUC131 series has 68/36K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro™ NUC131 series also provides additional Data Flash for user to store some application dependent data.

The NuMicro™ NUC131 supports another flexible feature: configurable Data Flash size. The Data Flash size is decided by Data Flash variable size enable (DFVSEN), Data Flash enable (DFEN) in Config0 and Data Flash base address (DFBADR) in Config1. When DFVSEN is set to 1, the Data Flash size is fixed at 4K and the address is started from 0x0001_f000, and the APROM size is become 64/32K. When DFVSEN is set to 0 and DFEN is set to 1, the Data Flash size is zero and the APROM size is 68/36K bytes. When DFVSEN is set to 0 and DFEN is set to 0, the APROM and Data Flash share 68/36K bytes continuous address and the start address of Data Flash is defined by (DFBADR) in Config1.

6.4.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 68/36 KB application program memory (APROM)
- 4KB In-System-Programming (ISP) loader program memory (LDROM)
- Configurable Data Flash size
- 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.6 Timer Controller (TIMER)

6.6.1 Overview

The timer controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external counter pin (TM0~TM3)
- Supports external pin capture (TM0_EXT~TM3_EXT) for interval measurement
- Supports external pin capture (TM0_EXT~TM3_EXT) for reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

6.8 Basic PWM Generator and Capture Timer (BPWM)

6.8.1 Overview

The NUC131 provides two BPWM generators – BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for ADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.8.2 Features

6.8.2.1 BPWM function features

- Supports maximum clock frequency up to100 MHz
- Supports up to two BPWM modules, each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution BPWM counter, each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt on the following events:
  - BPWM counter match zero, period value or compared value
- Supports trigger ADC on the following events:
  - BPWM counter match zero, period value or compared value

6.8.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.15 Analog-to-Digital Converter (ADC)

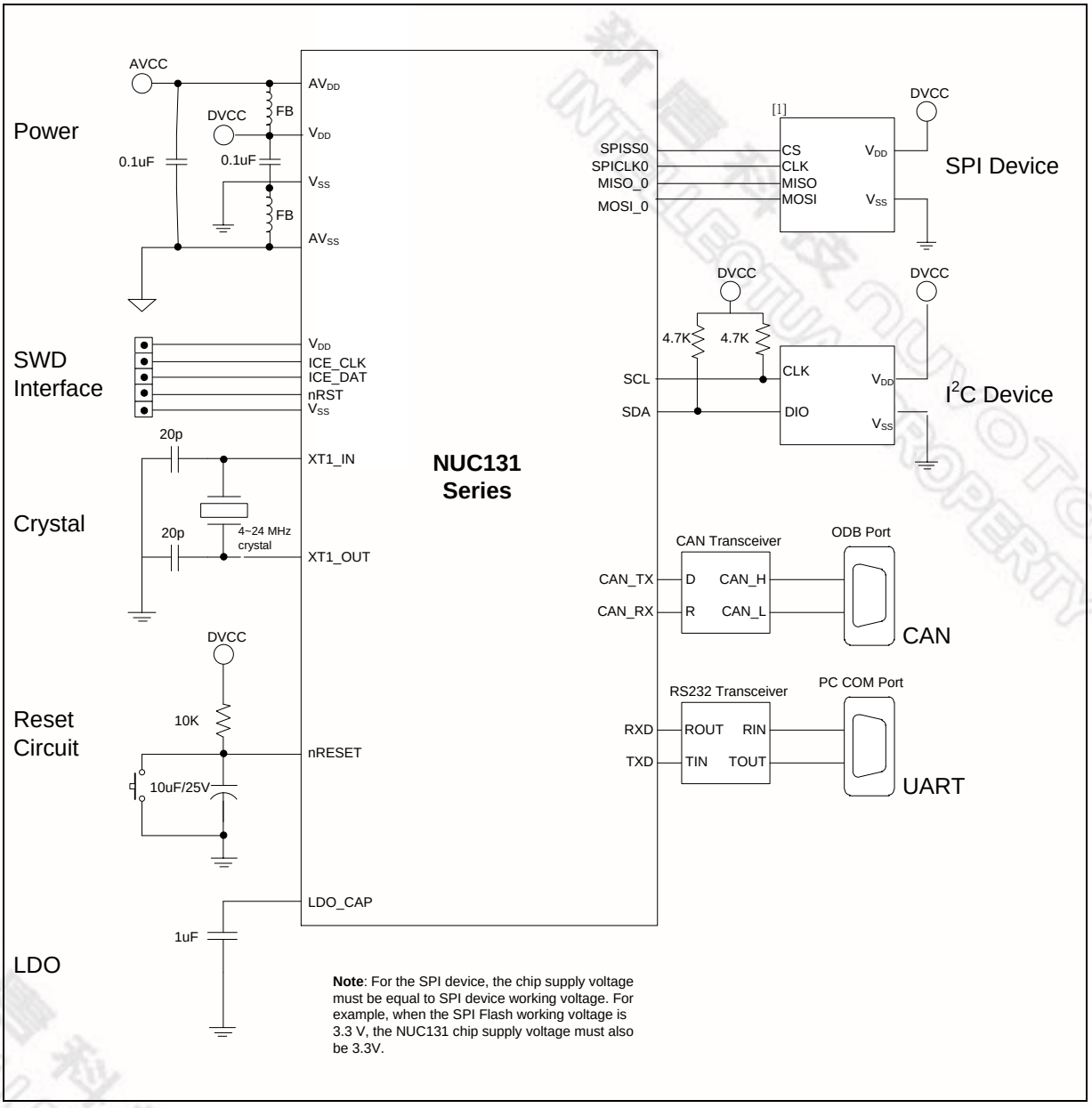
6.15.1 Overview

The NuMicro™ NUC131 series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM, BPWM trigger and external STADC pin.

6.15.2 Features

- Analog input voltage range: 0~V_{REF}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Up to 1 MSPS conversion rate (chip working at 5V)
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by:
  - Writing 1 to ADST bit (ADCR[11])through software
  - PWM and BPWM trigger
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Supports two set digital comparators. The conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: external analog voltage, and internal Band-gap voltage

7 APPLICATION CIRCUIT



Note: For the SPI device, the chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the NUC131 chip supply voltage must also be 3.3V.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

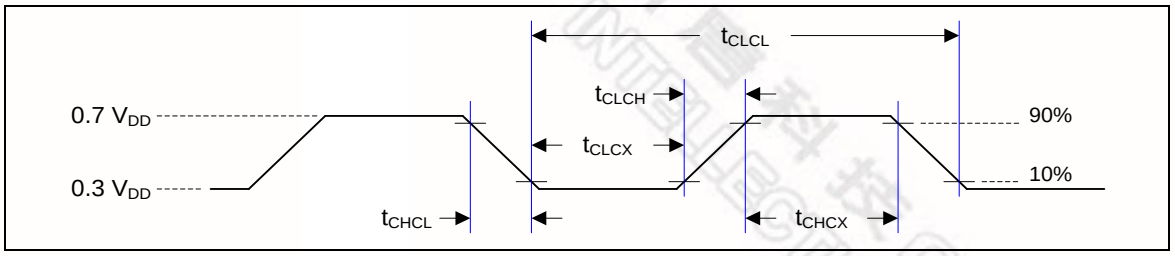
SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{PWD3}		17		µA	3.3V	X	32.768	V	V
	I_{PWD4}		17		µA	3.3V	X	32.768	V	V
	I_{PWD5}		10		µA	5.5V	X	X	X	X
	I_{PWD6}		9		µA	3.3V	X	X	X	X
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-67	-75	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}				
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-1	-	+1	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD} Open-drain or input only mode.				
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]		-610	-650	µA	V_{DD} = 5.5V, V_{IN}=2.0V				
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V				
		-0.3	-	0.6		V_{DD} = 2.5V				
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V				
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V				
Input Low Voltage XT1_IN[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V				
		0	-	0.4		V_{DD} = 3.0V				
Input High Voltage XT1_IN[*2]	V_{IH3}	3.5	-	V_{DD} +0.3	V	V_{DD} = 5.5V				
		2.4	-	V_{DD} +0.3		V_{DD} = 3.0V				
Negative going threshold (Schmitt input), nRESET	V_{ILS}	-0.3	-	0.2V_{DD}	V					
Positive going threshold (Schmitt input), nRESET	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V					
Internal nRESET pin pull up resistor	R_{RST}	40		150	kΩ					
Negative going threshold (Schmitt input),	V_{ILS}	-0.3	-	0.3 VDD	V					
Positive going threshold (Schmitt input),	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V					

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

8.3.2 External 4~24 MHz High Speed Crystal

SYMBOL	PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
V_{HXT}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
T_A	Temperature	-	-40	-	105	℃
I_{HXT}	Operating Current	12 MHz at V_{DD} = 5V	-	2	-	mA
		12 MHz at V_{DD} = 3V		0.8		mA
f_{HXT}	Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

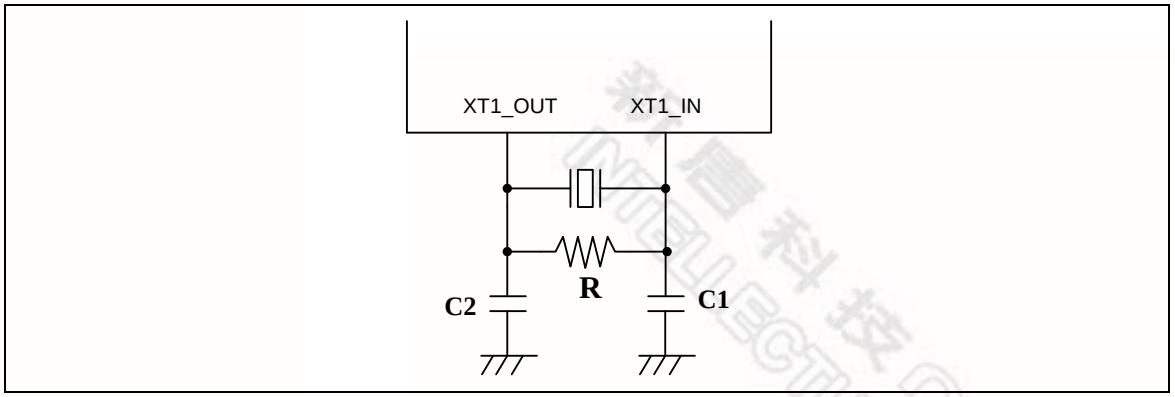


Figure 8-1 Typical Crystal Application Circuit

8.3.3 Internal 22.1184 MHz High Speed Oscillator

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HRC}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
f_{HRC}	Center Frequency	-	-	22.1184	-	MHz
	Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-1	-	+1	%
		-40℃~+105℃; V_{DD}=2.5 V~5.5 V	-2	-	+2	%
I_{HRC}	Operation Current	V_{DD} =5 V	-	744	-	uA

8.4.3 Low Voltage Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Quiescent Current	AV_{DD}=5.5 V	-	1	5	μA
I_{LVR}	Operation Temperature	-	-40	25	105	℃
V_{LVR}	Threshold Voltage	TA = 25 ℃	2.00	2.0	2.4	V
		TA = -40 ℃	1.95	1.98	2.02	V
		TA = 105 ℃	2.04	2.13	2.25	V

8.4.4 Brown-out Detector Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Temperature	-	-40	25	105	℃
I_{BOD}	Quiescent Current	AVDD=5.5 V	-	-	140	μA
V_{BOD}	Brown-out Voltage (Falling edge)	BOD_VL[1:0]=11	4.45	4.53	4.56	V
		BOD_VL [1:0]=10	3.74	3.8	3.84	V
		BOD_VL [1:0]=01	2.73	2.77	2.8	V
		BOD_VL [1:0]=00	2.22	2.25	2.28	V
V_{BOD}	Brown-out Voltage (Rising edge)	BOD_VL[1:0]=11	4.34	4.39	4.41	V
		BOD_VL [1:0]=10	3.65	3.69	3.71	V
		BOD_VL [1:0]=01	2.66	2.69	2.7	V
		BOD_VL [1:0]=00	2.16	2.19	2.2	V

8.4.5 Power-on Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
T_A	Operation Temperature	-	-40	25	105	℃
V_{POR}	Reset Voltage	V+	1.6	2	2.4	V
V_{POR}	VDD Start Voltage to Ensure Power-on Reset	-	-	-	100	mV
RR_{VDD}	VDD Raising Rate to Ensure Power-on Reset	-	0.025	-	-	V/ms
t_{POR}	Minimum Time for VDD Stays at VPOR to Ensure Power-on Reset	-	0.5	-	-	ms

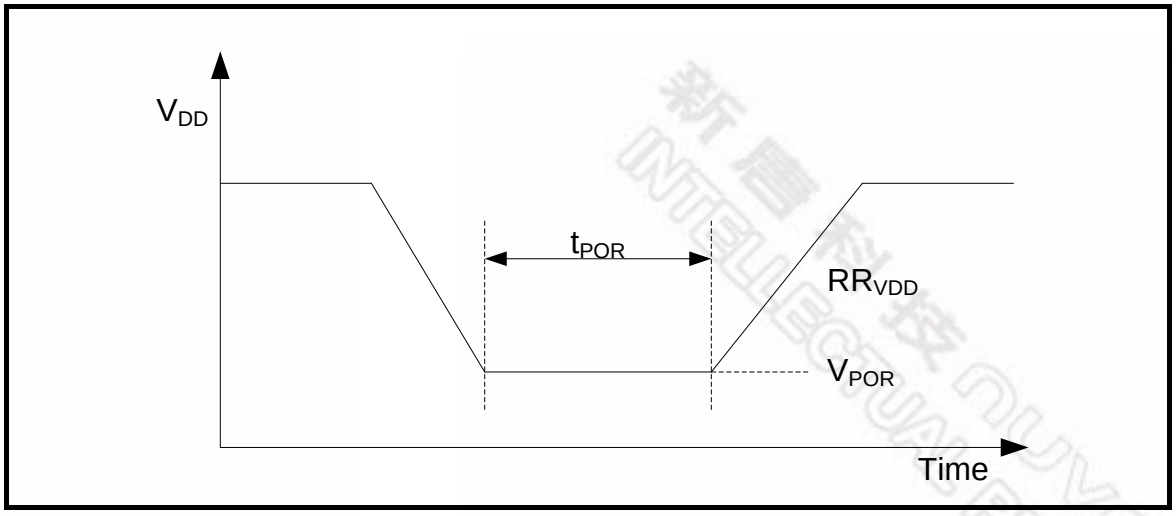


Figure 8-3 Power-up Ramp Condition

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{FLA}[1]	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		20000	-	-	cycles[2]
T_{RET}	Data Retention	At 85℃	100	-	-	year
T_{ERASE}	Page Erase Time		20	-	-	ms
T_{MER}	Mass Erase Time		40	-	-	ms
T_{PROG}	Program Time		40	-	-	μs

Note:

1. V_{FLA} is source from chip LDO output voltage
2. Number of program/erase cycles.