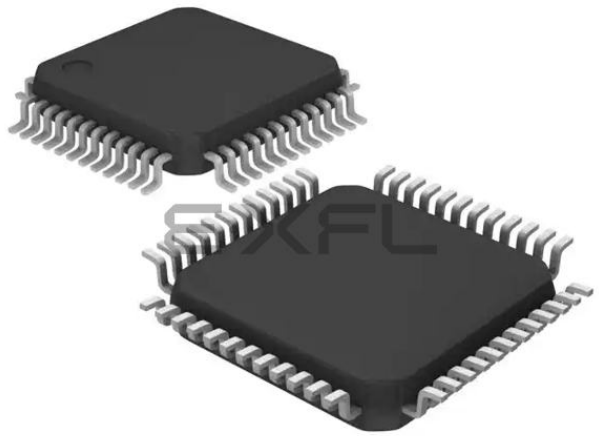

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	42
Program Memory Size	68KB (68K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc131ld2ae

channels
  - Supports independent mode for BPWM output/Capture input channel
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution BPWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each BPWM pin
  - Supports interrupt on the following events:
    - BPWM counter match zero, period value or compared value
  - Supports trigger ADC on the following events:
    - BPWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- PWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two PWM modules, each module provides three 16-bit timers and 6 output channels
  - Supports independent mode for PWM output/Capture input channel
  - Supports complementary mode for 3 complementary paired PWM output channel
    - Dead-time insertion with 12-bit resolution
    - Two compared values during one period
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution PWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each PWM pin
  - Supports brake function
    - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
    - Noise filter for brake source from pin
    - Edge detect brake source to control brake state until brake interrupt cleared
    - Level detect brake source to auto recover function after brake condition removed
  - Supports interrupt on the following events:
    - PWM counter match zero, period value or compared value
    - Brake condition happened
  - Supports trigger ADC on the following events:
    - PWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- UART
  - Up to six UART controllers
  - UART0 and UART1 ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0, UART1 and UART2 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Supports auto baud-rate generator
- SPI
  - One set of SPI controller
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently

3 ABBREVIATIONS

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
BPWM	Basic Pulse Width Modulation
CAN	Controller Area Network
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ MUC131 Series Selection Code

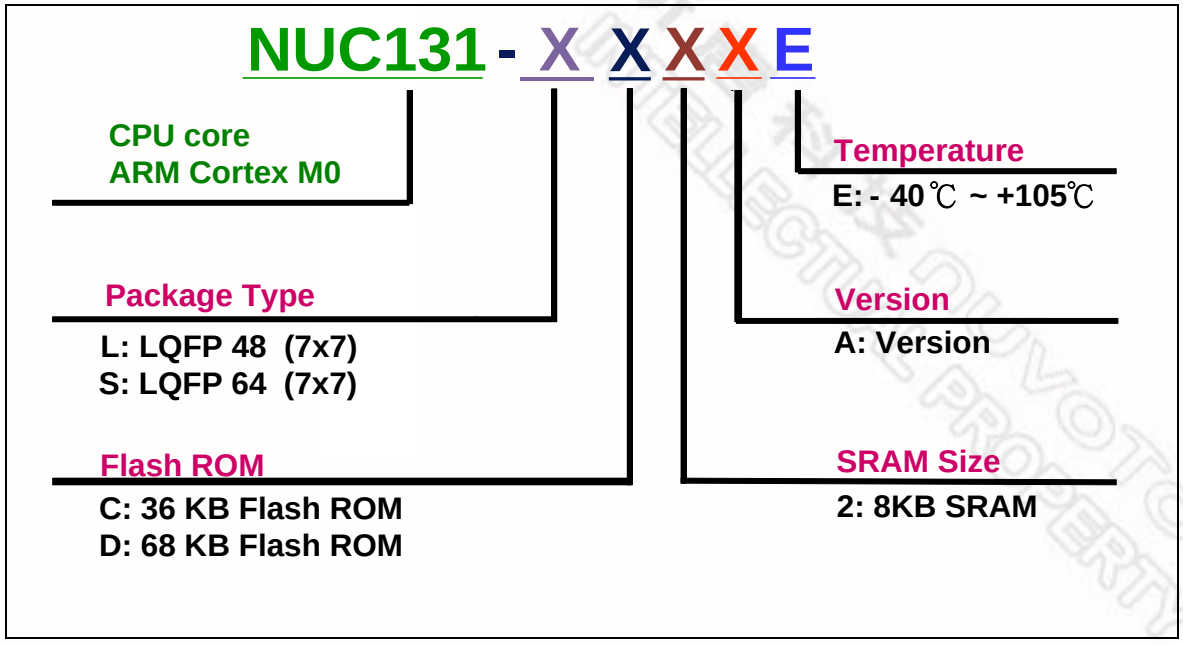


Figure 4-1 NuMicro™ NUC131 Series Selection Code

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		PWM0_BRAKE0	I	PWM0 brake input pin.
37	25	PA.15	I/O	General purpose digital I/O pin.
		PWM0_CH3	I/O	PWM0 CH3 output/Capture input.
38	26	PA.14	I/O	General purpose digital I/O pin.
		PWM0_CH2	I/O	PWM0 CH2 output/Capture input.
39	27	PA.13	I/O	General purpose digital I/O pin.
		PWM0_CH1	I/O	PWM0 CH1 output/Capture input.
		UART5_TXD	O	Data transmitter output pin for UART5.
40	28	PA.12	I/O	General purpose digital I/O pin.
		PWM0_CH0	I/O	PWM0 CH0 output/Capture input.
		UART5_RXD	I	Data receiver input pin for UART5.
41	29	PF.7	I/O	General purpose digital I/O pin.
		ICE_DAT	I/O	Serial wire debugger data pin.
42	30	PF.6	I/O	General purpose digital I/O pin.
		ICE_CLK	I	Serial wire debugger clock pin.
43	31	AV_{SS}	AP	Ground pin for analog circuit.
44	32	PA.0	I/O	General purpose digital I/O pin.
		ADC_CH0	AI	ADC_CH0 analog input.
		PWM0_CH4	I/O	PWM0 CH4 output/Capture input.
		I2C1_SCL	I/O	I^2C1 clock pin.
		UART5_TXD	O	Data transmitter output pin for UART5.
45	33	PA.1	I/O	General purpose digital I/O pin.
		ADC_CH1	AI	ADC_CH1 analog input.
		PWM0_CH5	I/O	PWM0 CH5 output/Capture input.
		I2C1_SDA	I/O	I^2C1 data input/output pin.
		UART5_RXD	I	Data receiver input pin for UART5.
46	34	PA.2	I/O	General purpose digital I/O pin.
		ADC_CH2	AI	ADC_CH2 analog input.
		PWM1_CH0	I/O	PWM1 CH0 output/Capture input.
		UART3_TXD	O	Data transmitter output pin for UART3.
47	35	PA.3	I/O	General purpose digital I/O pin.
		ADC_CH3	AI	ADC_CH3 analog input.

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

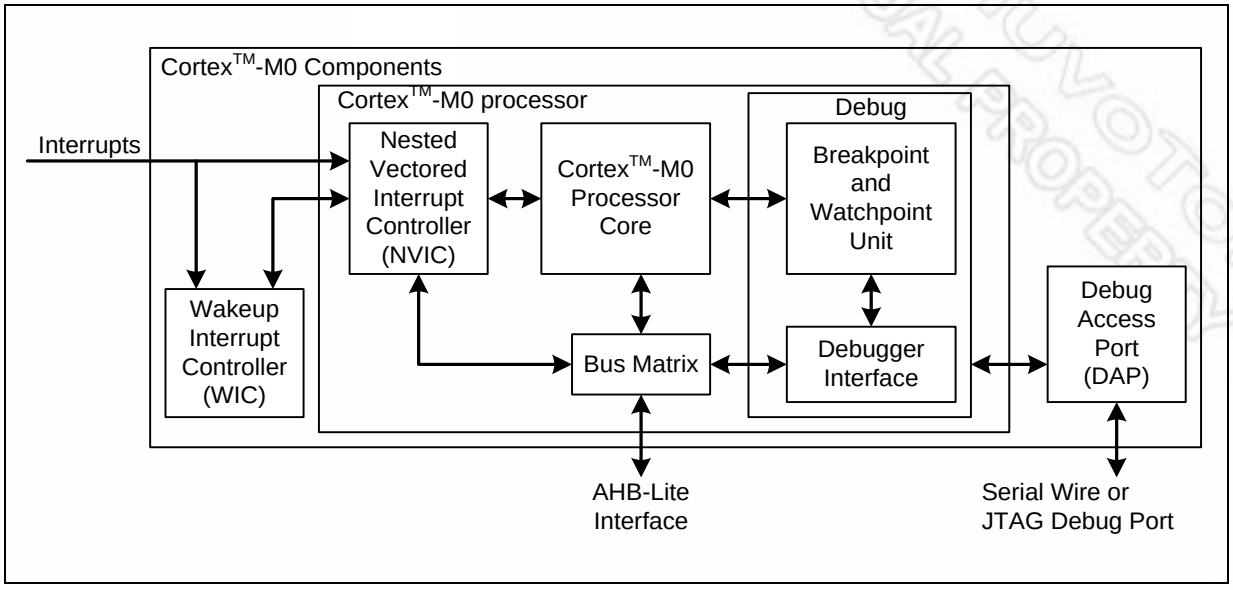


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event

(WFE) instructions, or the return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2.7 System Control

The Cortex™-M0 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex™-M0 interrupt priority and Cortex™-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro™ NUC131 series has up to 56 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 56 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B port has the maximum of 16 pins. The GPIOC port has the maximum of 12 pins. The GPIOD port has the maximum of 4 pins. The GPIOE port has the maximum of 1 pin. The GPIOF port has the maximum of 7 pins. Each of the 56 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} from 5.0 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function

6.7 PWM Generator and Capture Timer (PWM)

6.7.1 Overview

The NUC131 provides two PWM generators — PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses the comparator compared with counter to generate events. These events are used to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, which have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask, tri-state output enable and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.7.2 Features

6.7.2.1 PWM function features

- Supports maximum clock frequency up to100 MHz
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter, each module provides 3 PWM counters
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter match zero, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:

6.11 UART Interface Controller (UART)

6.11.1 Overview

The NuMicro™ NUC131 series provides up to six channels of Universal Asynchronous Receiver/Transmitters (UART). UART0/UART1/UART2 supports 16 bytes entry FIFO and UART3/UART4/UART5 support 1 byte buffer for data payload. Besides, only UART0 and UART1 support the flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function. UART0/UART1 provides RS-485 function mode. UART0/UART1/UART2 provides LIN master/slave function.

6.11.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16/16 bytes (UART0/UART1/UART2 support) entry FIFO and 1/1 bytes buffer for data payloads (UART3/UART4/UART5 support)
- Supports hardware auto-flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0/UART1 support).
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0/UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- LIN function mode (UART0/UART1/UART2 support)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode. (UART0/UART1 support)
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin.

6.12 I2C Serial Interface Controller (I2C)

6.12.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.12.2 Features

The I^2C bus uses two wires (I2Cn_SDA and I2Cn_SCL) to transfer information between devices connected to the bus. The main features of the I^2C bus include:

- Supports up to two I^2C serial interface controller
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in a 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function

6.15 Analog-to-Digital Converter (ADC)

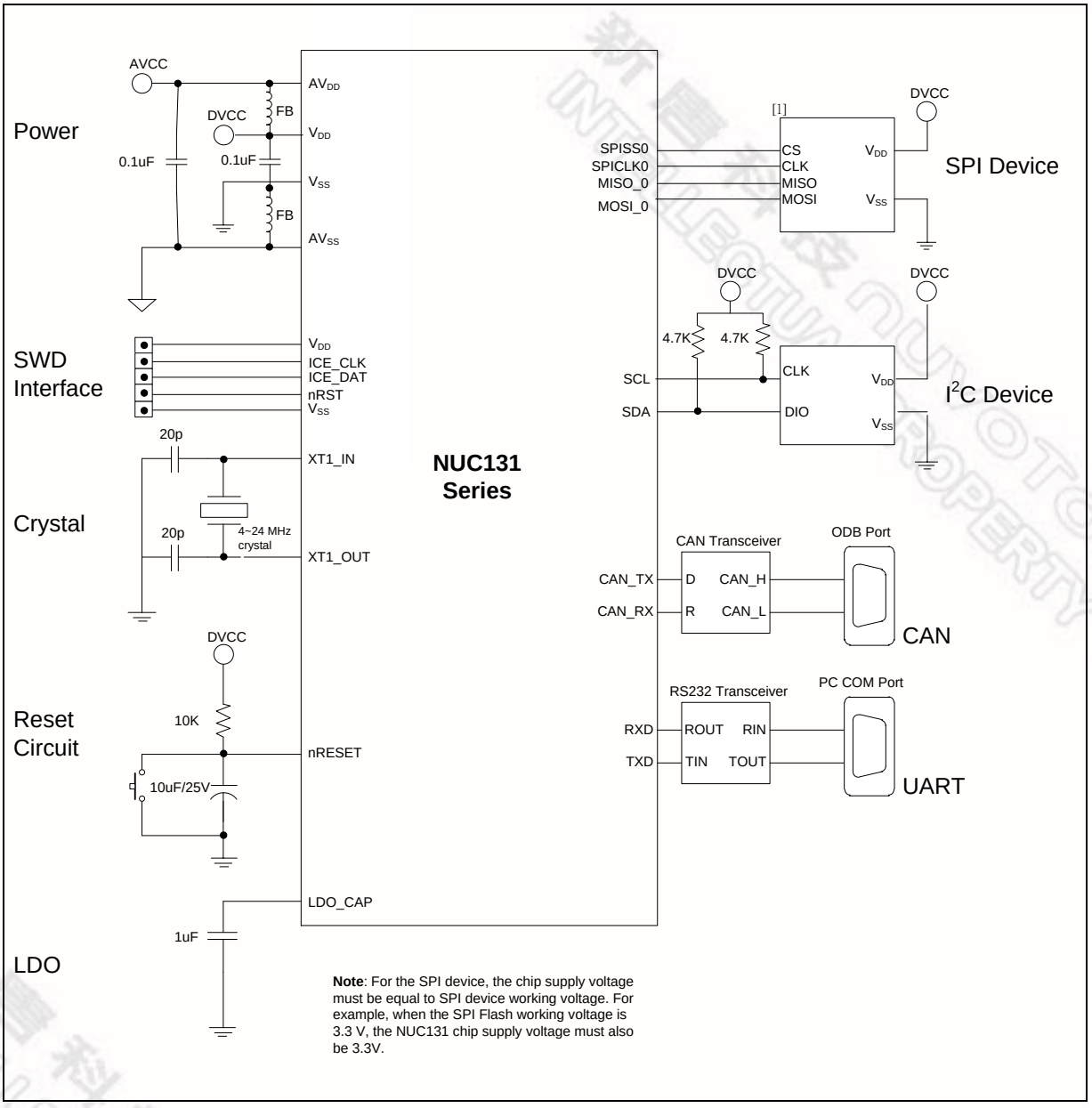
6.15.1 Overview

The NuMicro™ NUC131 series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. The A/D converter can be started by software, PWM, BPWM trigger and external STADC pin.

6.15.2 Features

- Analog input voltage range: 0~V_{REF}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Up to 1 MSPS conversion rate (chip working at 5V)
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by:
  - Writing 1 to ADST bit (ADCR[11])through software
  - PWM and BPWM trigger
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Supports two set digital comparators. The conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result matches the compare register setting
- Channel 7 supports 2 input sources: external analog voltage, and internal Band-gap voltage

7 APPLICATION CIRCUIT



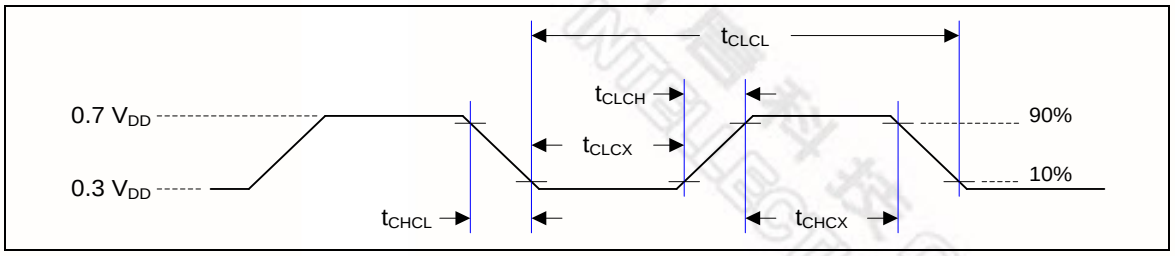
Note: For the SPI device, the chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the NUC131 chip supply voltage must also be 3.3V.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Normal Run Mode at 10 kHz while(1){} executed from flash VLDO =1.8 V						5.5V	X	10	X	V
	I_{DD22}		108		µA	5.5V	X	10	X	X
	I_{DD23}		98		µA	3.3V	X	10	X	V
	I_{DD24}		96		µA	3.3V	X	10	X	X
Operating Current Idle Mode at 50 MHz VLDO =1.8 V	I_{IDLE1}		21		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{IDLE2}		8		mA	5.5V	12 MHz	X	V	X
	I_{IDLE3}		20		mA	3.3V	12 MHz	X	V	V
	I_{IDLE4}		6.7		mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 22.1184 MHz VLDO =1.8 V	I_{IDLE5}	-	7.7	-	mA	5.5V	X	V	X	X
	I_{IDLE6}	-	2.1	-	mA	5.5V	X	V	X	X
	I_{IDLE7}	-	7.7	-	mA	3.3V	X	V	X	V
	I_{IDLE8}	-	2.1	-	mA	3.3V	X	V	X	X
Operating Current Idle Mode at 12 MHz V_{LDO} =1.8 V	I_{IDLE9}		7.3		mA	5.5V	12 MHz	X	X	V
	I_{IDLE10}		3.2		mA	5.5V	12 MHz	X	X	X
	I_{IDLE11}		5.8		mA	3.3V	12 MHz	X	X	V
	I_{IDLE12}		1.7		mA	3.3V	12 MHz	X	X	X
Operating Current Idle Mode at 4 MHz V_{LDO} =1.8 V	I_{IDLE13}		3.6		mA	5.5V	4 MHz	X	X	V
	I_{IDLE14}		2.2		mA	5.5V	4 MHz	X	X	X
	I_{IDLE15}		2.3		mA	3.3V	4 MHz	X	X	V
	I_{IDLE16}		0.96		mA	3.3V	4 MHz	X	X	X
Operating Current Idle Mode at 10 kHz	I_{IDLE21}		110		µA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{IDLE22}		107		µA	5.5V	X	10	X	X
	I_{IDLE23}		97		µA	3.3V	X	10	X	V
	I_{IDLE24}		95		µA	3.3V	X	10	X	X
Standby Current Power-down Mode (Deep Sleep Mode) V_{LDO} =1.6 V	I_{PWD1}		15		µA	V_{DD}	HXT/HIRC PLL	LXT (kHz)	RTC	RAM retension
						5.5V	X	X	X	V
	I_{PWD2}		15		µA	5.5V	X	X	X	V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{PWD3}		17		µA	3.3V	X	32.768	V	V
	I_{PWD4}		17		µA	3.3V	X	32.768	V	V
	I_{PWD5}		10		µA	5.5V	X	X	X	X
	I_{PWD6}		9		µA	3.3V	X	X	X	X
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-67	-75	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}				
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-1	-	+1	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD} Open-drain or input only mode.				
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]		-610	-650	µA	V_{DD} = 5.5V, V_{IN}=2.0V				
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V				
		-0.3	-	0.6		V_{DD} = 2.5V				
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V				
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V				
Input Low Voltage XT1_IN[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V				
		0	-	0.4		V_{DD} = 3.0V				
Input High Voltage XT1_IN[*2]	V_{IH3}	3.5	-	V_{DD} +0.3	V	V_{DD} = 5.5V				
		2.4	-	V_{DD} +0.3		V_{DD} = 3.0V				
Negative going threshold (Schmitt input), nRESET	V_{ILS}	-0.3	-	0.2V_{DD}	V					
Positive going threshold (Schmitt input), nRESET	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V					
Internal nRESET pin pull up resistor	R_{RST}	40		150	kΩ					
Negative going threshold (Schmitt input),	V_{ILS}	-0.3	-	0.3 VDD	V					
Positive going threshold (Schmitt input),	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V					

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

8.3.2 External 4~24 MHz High Speed Crystal

SYMBOL	PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
V_{HXT}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
T_A	Temperature	-	-40	-	105	℃
I_{HXT}	Operating Current	12 MHz at V_{DD} = 5V	-	2	-	mA
		12 MHz at V_{DD} = 3V		0.8		mA
f_{HXT}	Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

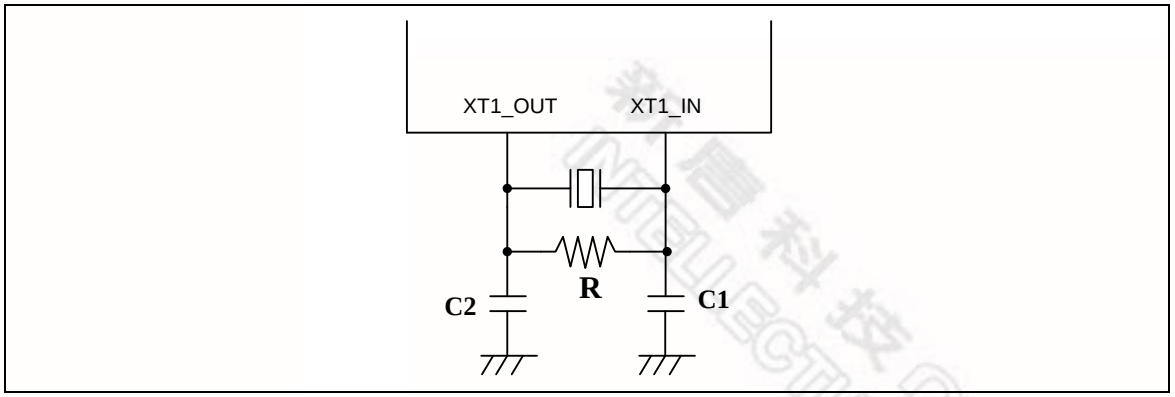


Figure 8-1 Typical Crystal Application Circuit

8.3.3 Internal 22.1184 MHz High Speed Oscillator

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HRC}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
f_{HRC}	Center Frequency	-	-	22.1184	-	MHz
	Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-1	-	+1	%
		-40℃~+105℃; V_{DD}=2.5 V~5.5 V	-2	-	+2	%
I_{HRC}	Operation Current	V_{DD} =5 V	-	744	-	uA

8.4.3 Low Voltage Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Quiescent Current	AV_{DD}=5.5 V	-	1	5	μA
I_{LVR}	Operation Temperature	-	-40	25	105	℃
V_{LVR}	Threshold Voltage	TA = 25 ℃	2.00	2.0	2.4	V
		TA = -40 ℃	1.95	1.98	2.02	V
		TA = 105 ℃	2.04	2.13	2.25	V

8.4.4 Brown-out Detector Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Temperature	-	-40	25	105	℃
I_{BOD}	Quiescent Current	AVDD=5.5 V	-	-	140	μA
V_{BOD}	Brown-out Voltage (Falling edge)	BOD_VL[1:0]=11	4.45	4.53	4.56	V
		BOD_VL [1:0]=10	3.74	3.8	3.84	V
		BOD_VL [1:0]=01	2.73	2.77	2.8	V
		BOD_VL [1:0]=00	2.22	2.25	2.28	V
V_{BOD}	Brown-out Voltage (Rising edge)	BOD_VL[1:0]=11	4.34	4.39	4.41	V
		BOD_VL [1:0]=10	3.65	3.69	3.71	V
		BOD_VL [1:0]=01	2.66	2.69	2.7	V
		BOD_VL [1:0]=00	2.16	2.19	2.2	V

8.4.5 Power-on Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
T_A	Operation Temperature	-	-40	25	105	℃
V_{POR}	Reset Voltage	V+	1.6	2	2.4	V
V_{POR}	VDD Start Voltage to Ensure Power-on Reset	-	-	-	100	mV
RR_{VDD}	VDD Raising Rate to Ensure Power-on Reset	-	0.025	-	-	V/ms
t_{POR}	Minimum Time for VDD Stays at VPOR to Ensure Power-on Reset	-	0.5	-	-	ms

8.7 SPI Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4	-	-	ns
t_V	Data output valid time	-	1	2	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	2	4	ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	3.5	-	-	ns
t_V	Data output valid time	-	16	22	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	18	24	ns

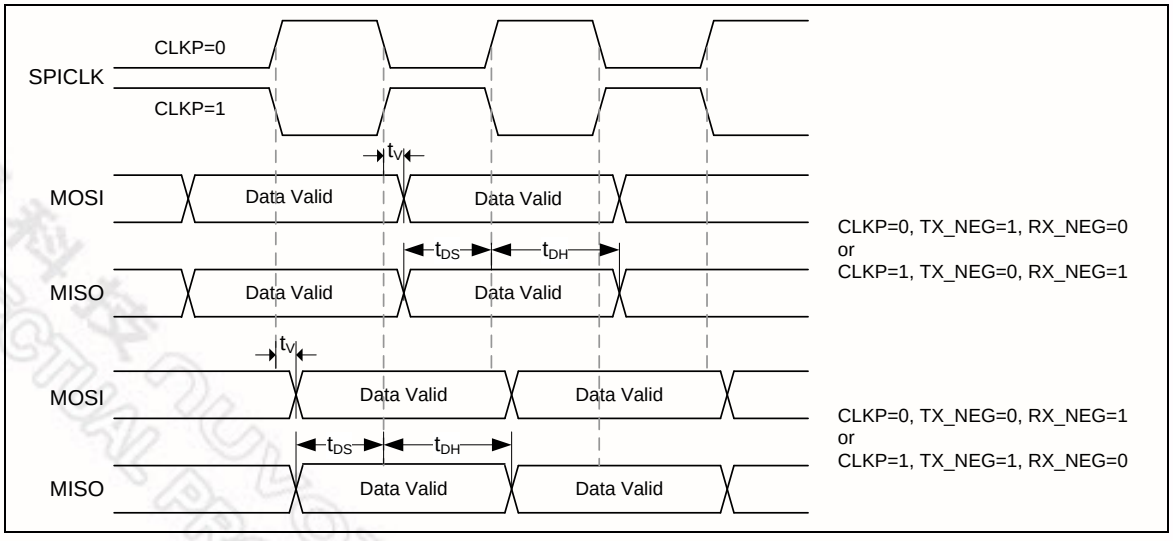


Figure 8-5 SPI Master Mode Timing Diagram