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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc131sc2ae

2 FEATURES

- ARM® Cortex™-M0 core
  - Runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 36K/68K bytes Flash for program code
  - Configurable Flash memory for data memory (Data Flash), 4 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 8KB embedded SRAM
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ±2 % at -40 ℃ ~ +105 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL output frequency up to 200 MHz, BPWM/PWM clock frequency up to 100 MHz, and System operation frequency up to 50 MHz
  - External 4~24 MHz high speed crystal input for precise timing operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- Watchdog Timer
  - Multiple clock sources
    - System clock (HCLK)
    - Internal 10 kHz oscillator (LIRC)
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- BPWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two BPWM modules, each module provides one 16-bit timer and 6 output

channels
  - Supports independent mode for BPWM output/Capture input channel
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution BPWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each BPWM pin
  - Supports interrupt on the following events:
    - BPWM counter match zero, period value or compared value
  - Supports trigger ADC on the following events:
    - BPWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- PWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two PWM modules, each module provides three 16-bit timers and 6 output channels
  - Supports independent mode for PWM output/Capture input channel
  - Supports complementary mode for 3 complementary paired PWM output channel
    - Dead-time insertion with 12-bit resolution
    - Two compared values during one period
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution PWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each PWM pin
  - Supports brake function
    - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
    - Noise filter for brake source from pin
    - Edge detect brake source to control brake state until brake interrupt cleared
    - Level detect brake source to auto recover function after brake condition removed
  - Supports interrupt on the following events:
    - PWM counter match zero, period value or compared value
    - Brake condition happened
  - Supports trigger ADC on the following events:
    - PWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- UART
  - Up to six UART controllers
  - UART0 and UART1 ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0, UART1 and UART2 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Supports auto baud-rate generator
- SPI
  - One set of SPI controller
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently

- Supports Byte Suspend mode in 32-bit transmission
- Supports three wire, no slave select signal, bi-direction interface

- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- CAN 2.0
  - One set of CAN device
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Support power-down wake-up function
- ADC
  - 12-bit SAR ADC with 800 kSPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming or external input
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40℃ ~ +105℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin / 48-pin (7mm x 7mm)

3 ABBREVIATIONS

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
BPWM	Basic Pulse Width Modulation
CAN	Controller Area Network
DAP	Debug Access Port
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4.2 NuMicro™ NUC131 Series Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity					PWM (16-Bit)	ADC (12-Bit)	ISP/ICP/IAP	Package
							UART	SPI	I^2C	LIN	CAN				
NUC131LC2AE	36	8	Configurable	4	42	4	6	1	2	3	1	24	8 ch	√	LQFP48
NUC131LD2AE	68	8	Configurable	4	42	4	6	1	2	3	1	24	8 ch	√	LQFP48
NUC131SC2AE	36	8	Configurable	4	56	4	6	1	2	3	1	24	8 ch	√	LQFP64
NUC131SD2AE	68	8	Configurable	4	56	4	6	1	2	3	1	24	8 ch	√	LQFP64

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		PWM0_BRAKE0	I	PWM0 brake input pin.
37	25	PA.15	I/O	General purpose digital I/O pin.
		PWM0_CH3	I/O	PWM0 CH3 output/Capture input.
38	26	PA.14	I/O	General purpose digital I/O pin.
		PWM0_CH2	I/O	PWM0 CH2 output/Capture input.
39	27	PA.13	I/O	General purpose digital I/O pin.
		PWM0_CH1	I/O	PWM0 CH1 output/Capture input.
		UART5_TXD	O	Data transmitter output pin for UART5.
40	28	PA.12	I/O	General purpose digital I/O pin.
		PWM0_CH0	I/O	PWM0 CH0 output/Capture input.
		UART5_RXD	I	Data receiver input pin for UART5.
41	29	PF.7	I/O	General purpose digital I/O pin.
		ICE_DAT	I/O	Serial wire debugger data pin.
42	30	PF.6	I/O	General purpose digital I/O pin.
		ICE_CLK	I	Serial wire debugger clock pin.
43	31	AV_{SS}	AP	Ground pin for analog circuit.
44	32	PA.0	I/O	General purpose digital I/O pin.
		ADC_CH0	AI	ADC_CH0 analog input.
		PWM0_CH4	I/O	PWM0 CH4 output/Capture input.
		I2C1_SCL	I/O	I^2C1 clock pin.
		UART5_TXD	O	Data transmitter output pin for UART5.
45	33	PA.1	I/O	General purpose digital I/O pin.
		ADC_CH1	AI	ADC_CH1 analog input.
		PWM0_CH5	I/O	PWM0 CH5 output/Capture input.
		I2C1_SDA	I/O	I^2C1 data input/output pin.
		UART5_RXD	I	Data receiver input pin for UART5.
46	34	PA.2	I/O	General purpose digital I/O pin.
		ADC_CH2	AI	ADC_CH2 analog input.
		PWM1_CH0	I/O	PWM1 CH0 output/Capture input.
		UART3_TXD	O	Data transmitter output pin for UART3.
47	35	PA.3	I/O	General purpose digital I/O pin.
		ADC_CH3	AI	ADC_CH3 analog input.

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
60	46	nRESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
61		V_{SS}	**P**	Ground pin for digital circuit.
62		V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
63	47	PF.8	**I/O**	General purpose digital I/O pin.
		CLKO	**O**	Frequency divider clock output pin.
		BPWM1_CH4	**I/O**	BPWM1 CH4 output/Capture input.
64	48	PB.8	**I/O**	General purpose digital I/O pin.
		STADC	**I**	ADC external trigger input.
		TM0	**I/O**	Timer0 event counter input / toggle output.
		CLKO	**O**	Frequency divider clock output pin.
		BPWM1_CH2	**I/O**	BPWM1 CH2 output/Capture input.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

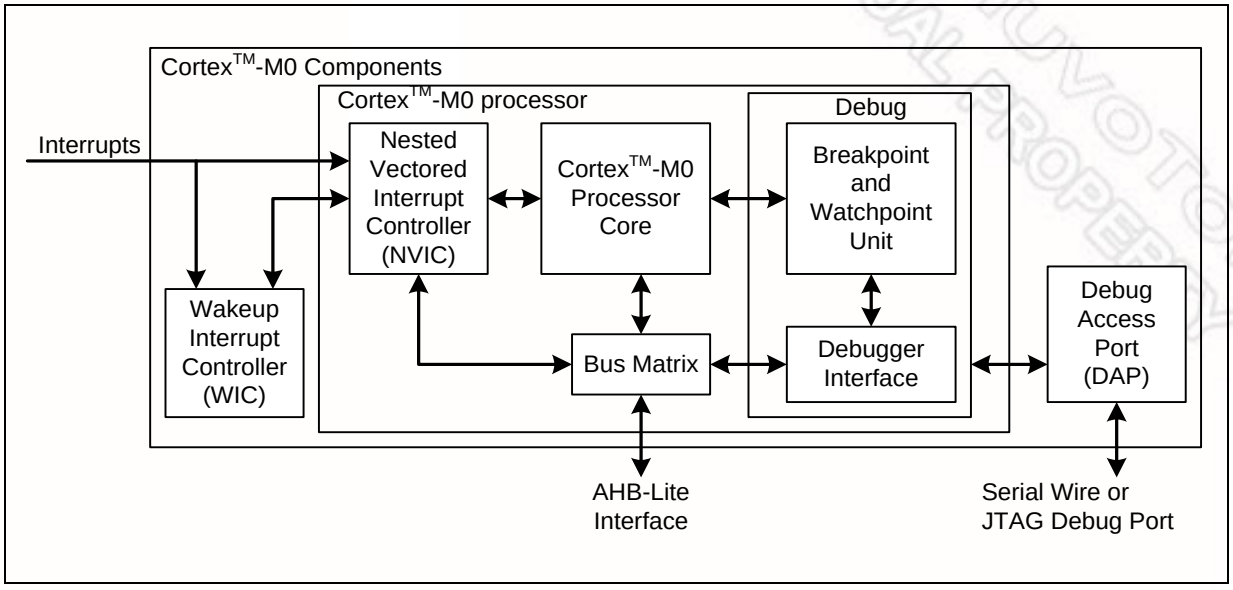


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Power-on Reset
- Low level on the nRESET pin
- Watchdog Time-out Reset
- Low Voltage Reset
- Brown-out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-on Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-on Reset is external crystal circuit and BS (ISPCON[1]) bit. System Reset does not reset external crystal circuit and BS (ISPCON[1]) bit, but Power-on Reset does.

6.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level with the digital power (V_{DD}). Figure 6-2 shows the NuMicro™ NUC131 power distribution.

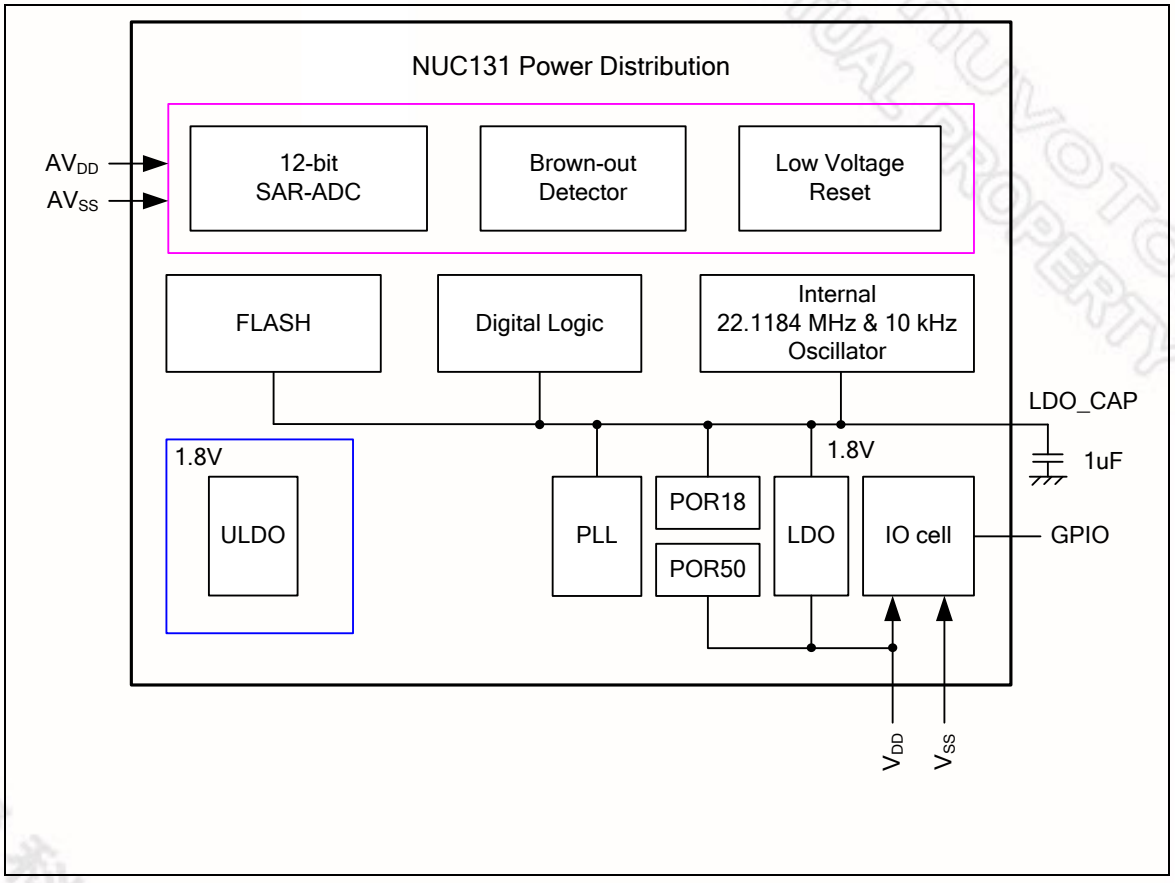


Figure 6-2 NuMicro™ NUC131 Power Distribution Diagram

6.2.5 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is unknown on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex™-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184 MHz internal high speed RC oscillator to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 5 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency(PLL FOUT),PLL source can be from external 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC))
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

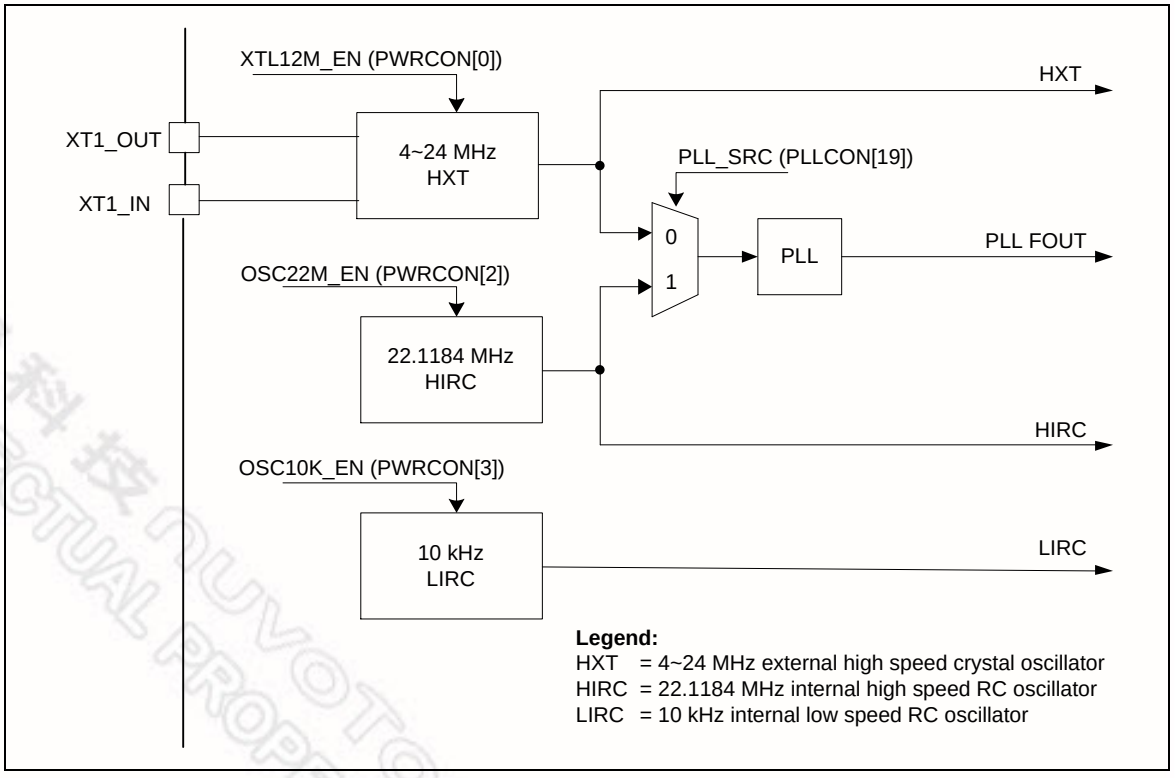


Figure 6-3 Clock Generator Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro™ NUC131 series has 68/36K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro™ NUC131 series also provides additional Data Flash for user to store some application dependent data.

The NuMicro™ NUC131 supports another flexible feature: configurable Data Flash size. The Data Flash size is decided by Data Flash variable size enable (DFVSEN), Data Flash enable (DFEN) in Config0 and Data Flash base address (DFBADR) in Config1. When DFVSEN is set to 1, the Data Flash size is fixed at 4K and the address is started from 0x0001_f000, and the APROM size is become 64/32K. When DFVSEN is set to 0 and DFEN is set to 1, the Data Flash size is zero and the APROM size is 68/36K bytes. When DFVSEN is set to 0 and DFEN is set to 0, the APROM and Data Flash share 68/36K bytes continuous address and the start address of Data Flash is defined by (DFBADR) in Config1.

6.4.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 68/36 KB application program memory (APROM)
- 4KB In-System-Programming (ISP) loader program memory (LDROM)
- Configurable Data Flash size
- 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.11 UART Interface Controller (UART)

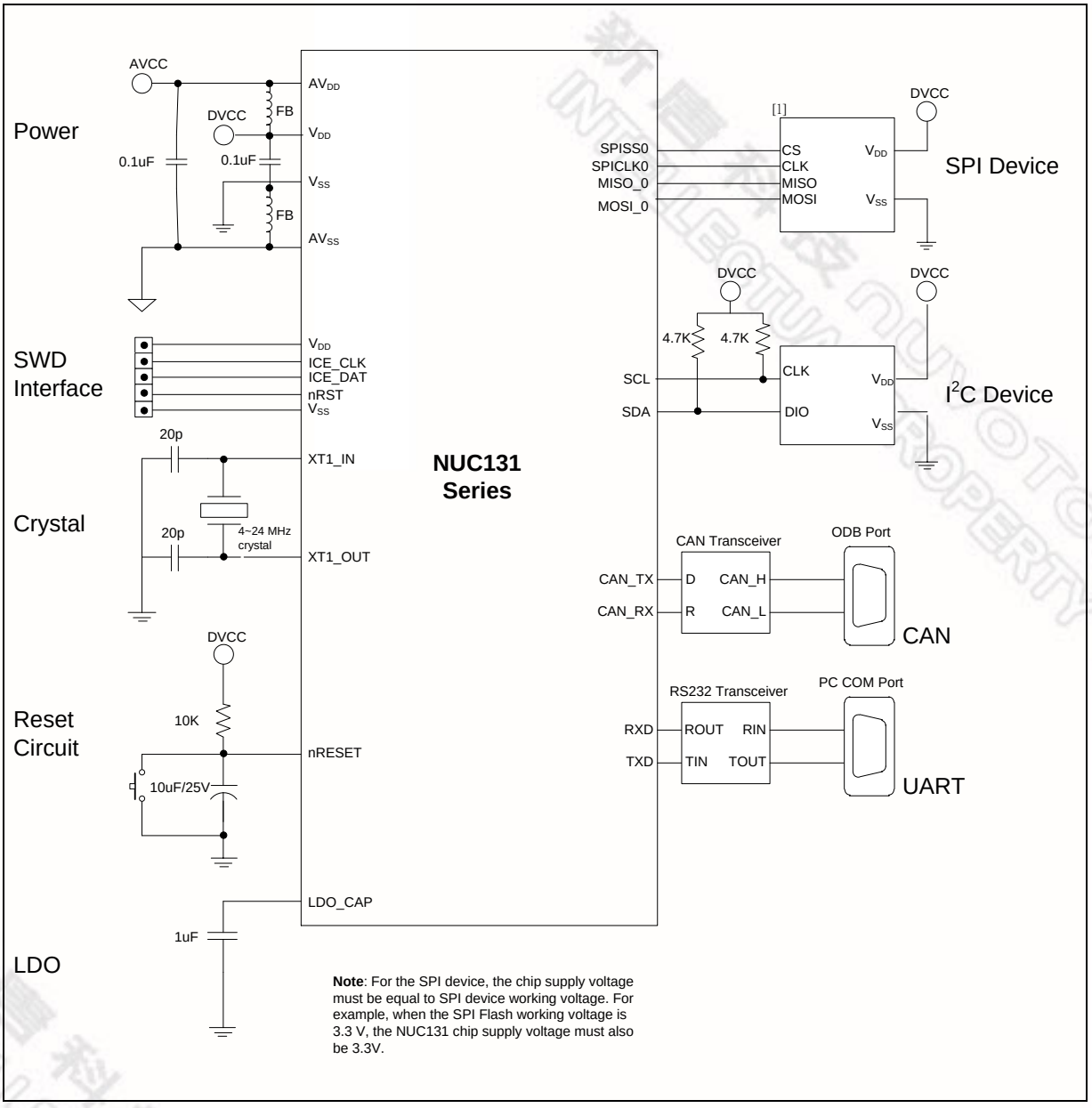
6.11.1 Overview

The NuMicro™ NUC131 series provides up to six channels of Universal Asynchronous Receiver/Transmitters (UART). UART0/UART1/UART2 supports 16 bytes entry FIFO and UART3/UART4/UART5 support 1 byte buffer for data payload. Besides, only UART0 and UART1 support the flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function. UART0/UART1 provides RS-485 function mode. UART0/UART1/UART2 provides LIN master/slave function.

6.11.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16/16 bytes (UART0/UART1/UART2 support) entry FIFO and 1/1 bytes buffer for data payloads (UART3/UART4/UART5 support)
- Supports hardware auto-flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0/UART1 support).
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0/UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- LIN function mode (UART0/UART1/UART2 support)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode. (UART0/UART1 support)
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin.

7 APPLICATION CIRCUIT



Note: For the SPI device, the chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the NUC131 chip supply voltage must also be 3.3V.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Normal Run Mode at 10 kHz while(1){} executed from flash VLDO =1.8 V						5.5V	X	10	X	V
	I_{DD22}		108		µA	5.5V	X	10	X	X
	I_{DD23}		98		µA	3.3V	X	10	X	V
	I_{DD24}		96		µA	3.3V	X	10	X	X
Operating Current Idle Mode at 50 MHz VLDO =1.8 V	I_{IDLE1}		21		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{IDLE2}		8		mA	5.5V	12 MHz	X	V	X
	I_{IDLE3}		20		mA	3.3V	12 MHz	X	V	V
	I_{IDLE4}		6.7		mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 22.1184 MHz VLDO =1.8 V	I_{IDLE5}	-	7.7	-	mA	5.5V	X	V	X	X
	I_{IDLE6}	-	2.1	-	mA	5.5V	X	V	X	X
	I_{IDLE7}	-	7.7	-	mA	3.3V	X	V	X	V
	I_{IDLE8}	-	2.1	-	mA	3.3V	X	V	X	X
Operating Current Idle Mode at 12 MHz V_{LDO} =1.8 V	I_{IDLE9}		7.3		mA	5.5V	12 MHz	X	X	V
	I_{IDLE10}		3.2		mA	5.5V	12 MHz	X	X	X
	I_{IDLE11}		5.8		mA	3.3V	12 MHz	X	X	V
	I_{IDLE12}		1.7		mA	3.3V	12 MHz	X	X	X
Operating Current Idle Mode at 4 MHz V_{LDO} =1.8 V	I_{IDLE13}		3.6		mA	5.5V	4 MHz	X	X	V
	I_{IDLE14}		2.2		mA	5.5V	4 MHz	X	X	X
	I_{IDLE15}		2.3		mA	3.3V	4 MHz	X	X	V
	I_{IDLE16}		0.96		mA	3.3V	4 MHz	X	X	X
Operating Current Idle Mode at 10 kHz	I_{IDLE21}		110		µA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{IDLE22}		107		µA	5.5V	X	10	X	X
	I_{IDLE23}		97		µA	3.3V	X	10	X	V
	I_{IDLE24}		95		µA	3.3V	X	10	X	X
Standby Current Power-down Mode (Deep Sleep Mode) V_{LDO} =1.6 V	I_{PWD1}		15		µA	V_{DD}	HXT/HIRC PLL	LXT (kHz)	RTC	RAM retension
						5.5V	X	X	X	V
	I_{PWD2}		15		µA	5.5V	X	X	X	V

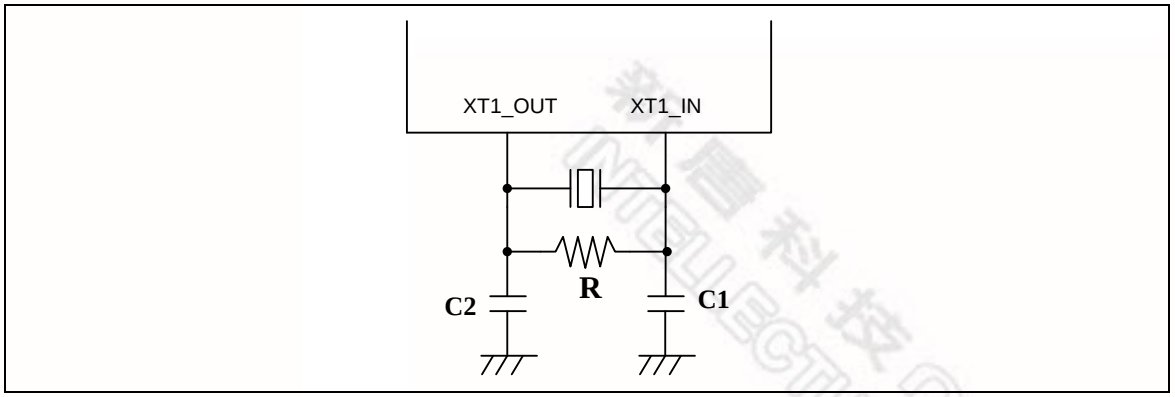


Figure 8-1 Typical Crystal Application Circuit

8.3.3 Internal 22.1184 MHz High Speed Oscillator

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HRC}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
f_{HRC}	Center Frequency	-	-	22.1184	-	MHz
	Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-1	-	+1	%
		-40℃~+105℃; V_{DD}=2.5 V~5.5 V	-2	-	+2	%
I_{HRC}	Operation Current	V_{DD} =5 V	-	744	-	uA

8.4.3 Low Voltage Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Quiescent Current	AV_{DD}=5.5 V	-	1	5	μA
I_{LVR}	Operation Temperature	-	-40	25	105	℃
V_{LVR}	Threshold Voltage	TA = 25 ℃	2.00	2.0	2.4	V
		TA = -40 ℃	1.95	1.98	2.02	V
		TA = 105 ℃	2.04	2.13	2.25	V

8.4.4 Brown-out Detector Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Temperature	-	-40	25	105	℃
I_{BOD}	Quiescent Current	AVDD=5.5 V	-	-	140	μA
V_{BOD}	Brown-out Voltage (Falling edge)	BOD_VL[1:0]=11	4.45	4.53	4.56	V
		BOD_VL [1:0]=10	3.74	3.8	3.84	V
		BOD_VL [1:0]=01	2.73	2.77	2.8	V
		BOD_VL [1:0]=00	2.22	2.25	2.28	V
V_{BOD}	Brown-out Voltage (Rising edge)	BOD_VL[1:0]=11	4.34	4.39	4.41	V
		BOD_VL [1:0]=10	3.65	3.69	3.71	V
		BOD_VL [1:0]=01	2.66	2.69	2.7	V
		BOD_VL [1:0]=00	2.16	2.19	2.2	V

8.4.5 Power-on Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
T_A	Operation Temperature	-	-40	25	105	℃
V_{POR}	Reset Voltage	V+	1.6	2	2.4	V
V_{POR}	VDD Start Voltage to Ensure Power-on Reset	-	-	-	100	mV
RR_{VDD}	VDD Raising Rate to Ensure Power-on Reset	-	0.025	-	-	V/ms
t_{POR}	Minimum Time for VDD Stays at VPOR to Ensure Power-on Reset	-	0.5	-	-	ms

10 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.00	Oct. 31, 2014	Preliminary version