Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	68KB (68K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc131sd2ae

List of Figures

新唐科技 NUVOTON INTELLECTUAL PROPERTY

- Supports Byte Suspend mode in 32-bit transmission
- Supports three wire, no slave select signal, bi-direction interface

- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function
- CAN 2.0
  - One set of CAN device
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Support power-down wake-up function
- ADC
  - 12-bit SAR ADC with 800 kSPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming or external input
- 96-bit unique ID (UID)
- 128-bit unique customer ID(UCID)
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40℃ ~ +105℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin / 48-pin (7mm x 7mm)

新唐科技 NUVOTON INTELLECTUAL PROPERTY

4.2 NuMicro™ NUC131 Series Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity					PWM (16-Bit)	ADC (12-Bit)	ISP/ICP/IAP	Package
							UART	SPI	I^2C	LIN	CAN				
NUC131LC2AE	36	8	Configurable	4	42	4	6	1	2	3	1	24	8 ch	√	LQFP48
NUC131LD2AE	68	8	Configurable	4	42	4	6	1	2	3	1	24	8 ch	√	LQFP48
NUC131SC2AE	36	8	Configurable	4	56	4	6	1	2	3	1	24	8 ch	√	LQFP64
NUC131SD2AE	68	8	Configurable	4	56	4	6	1	2	3	1	24	8 ch	√	LQFP64

新唐科技 NUVOTON INTELLECTUAL PROPERTY

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		XT1_IN	**I**	External 4~24 MHz (high speed) crystal input pin.
60	46	nRESET	**I**	External reset input: active LOW, with an internal pull-up. Set this pin low reset chip to initial state.
61		V_{SS}	**P**	Ground pin for digital circuit.
62		V_{DD}	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
63	47	PF.8	**I/O**	General purpose digital I/O pin.
		CLKO	**O**	Frequency divider clock output pin.
		BPWM1_CH4	**I/O**	BPWM1 CH4 output/Capture input.
64	48	PB.8	**I/O**	General purpose digital I/O pin.
		STADC	**I**	ADC external trigger input.
		TM0	**I/O**	Timer0 event counter input / toggle output.
		CLKO	**O**	Frequency divider clock output pin.
		BPWM1_CH2	**I/O**	BPWM1 CH2 output/Capture input.

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

新唐科技 NUVOTON INTELLECTUAL PROPERTY

6.2.4 System Memory Map

The NuMicro™ NUC131 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripheral. The NuMicro™ NUC131 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_0FFF	FLASH_BA	FLASH Memory Space (68 KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (8 KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	BPWM0_BA	BPWM0 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4005_4000 – 0x4005_7FFF	UART3_BA	UART3 Control Registers
0x4005_8000 – 0x4005_BFFF	UART4_BA	UART4 Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4014_0000 – 0x4014_3FFF	PWM1_BA	PWM1 Control Registers
0x4014_4000 – 0x4014_7FFF	BPWM1_BA	BPWM1 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers
0x4015_8000 – 0x4015_BFFF	UART5_BA	UART5 Control Registers
0x4018_0000 – 0x4018_3FFF	CAN0_BA	CAN0 Bus Control Registers

System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6-1 Address Space Assignments for On-Chip Controllers

新唐科技 NUVOTON INTELLECTUAL PROPERTY

30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**UART3_INT**	UART3	UART3 interrupt
32	16	**UART4_INT**	UART4	UART4 interrupt
33	17	**UART5_INT**	UART5	UART5 interrupt
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**CAN0_INT**	CAN0	CAN0 interrupt
37	21	**-**	-	Reserved
38	22	**PWM0_INT**	PWM0	PWM0 interrupt
39	23	**PWM1_INT**	PWM1	PWM1 interrupt
40	24	**BPWM0_INT**	BPWM0	BPWM0 interrupt
41	25	**BPWM1_INT**	BPWM1	BPWM1 interrupt
42	26	**BRAKE0_INT**	PWM0	PWM0 brake interrupt
43	27	**BRAKE1_INT**	PWM1	PWM1 brake interrupt
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state
45	29	**ADC_INT**	ADC	ADC interrupt
46	30	**CKD_INT**	CLKC	Clock detection interrupt
47	31	**-**	-	Reserved

Table 6-3 System Interrupt Map

新唐科技 NUVOTON INTELLECTUAL PROPERTY

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex™-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184 MHz internal high speed RC oscillator to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

The clock generator consists of 5 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency(PLL FOUT),PLL source can be from external 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC))
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

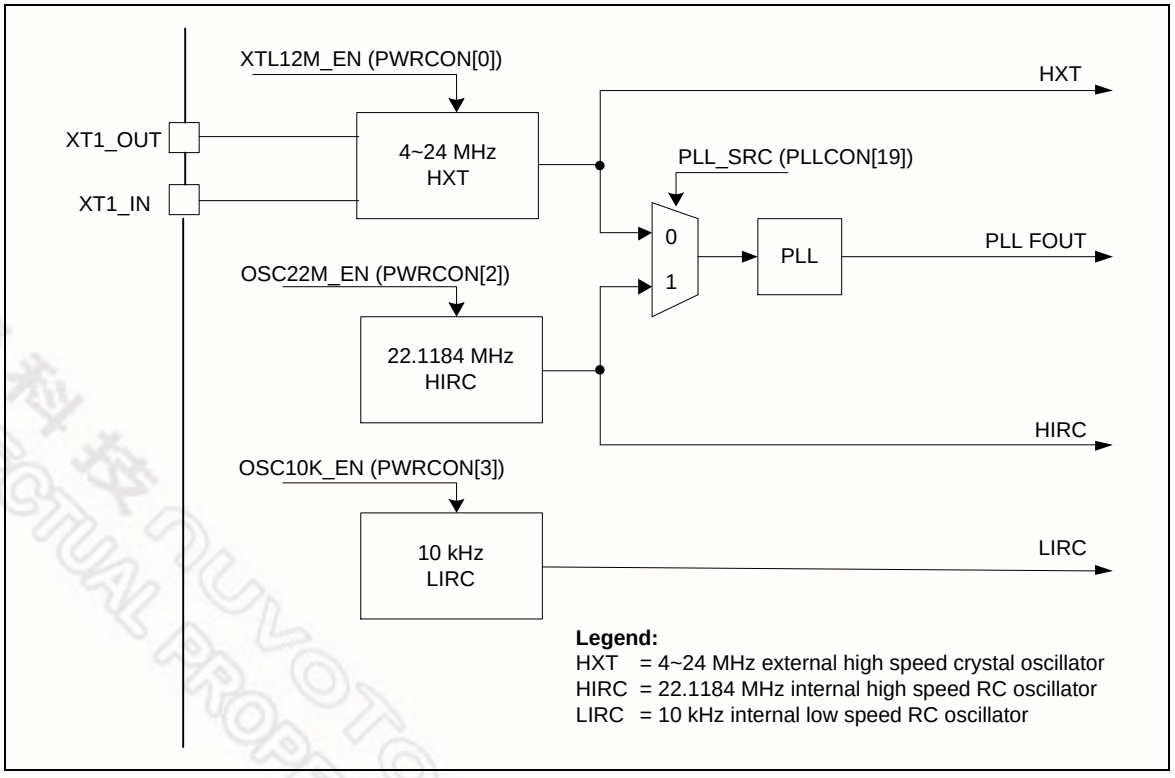


Figure 6-3 Clock Generator Block Diagram

6.3.3 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
- WDT/Timer Peripherals Clock (when 10 kHz intertnal low speed RC oscillator (LIRC) is adopted as clock source)

新唐科技 NUVOTON INTELLECTUAL PROPERTY

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro™ NUC131 series has 68/36K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro™ NUC131 series also provides additional Data Flash for user to store some application dependent data.

The NuMicro™ NUC131 supports another flexible feature: configurable Data Flash size. The Data Flash size is decided by Data Flash variable size enable (DFVSEN), Data Flash enable (DFEN) in Config0 and Data Flash base address (DFBADR) in Config1. When DFVSEN is set to 1, the Data Flash size is fixed at 4K and the address is started from 0x0001_f000, and the APROM size is become 64/32K. When DFVSEN is set to 0 and DFEN is set to 1, the Data Flash size is zero and the APROM size is 68/36K bytes. When DFVSEN is set to 0 and DFEN is set to 0, the APROM and Data Flash share 68/36K bytes continuous address and the start address of Data Flash is defined by (DFBADR) in Config1.

6.4.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 68/36 KB application program memory (APROM)
- 4KB In-System-Programming (ISP) loader program memory (LDROM)
- Configurable Data Flash size
- 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

新唐科技 NUVOTON INTELLECTUAL PROPERTY

6.6 Timer Controller (TIMER)

6.6.1 Overview

The timer controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external counter pin (TM0~TM3)
- Supports external pin capture (TM0_EXT~TM3_EXT) for interval measurement
- Supports external pin capture (TM0_EXT~TM3_EXT) for reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated

新唐科技 NUVOTON INTELLECTUAL PROPERTY

6.8.2.3 Compare table

Feature	PWM	BPWM
Counter number	2 channels share 1 timer, total 6 timers	6 channels share 1 timer, total 1 timer
Complementary mode	V	X
Dead-time function	V	X
Brake function	V	X
Capture reload	2 channels reload 1 timer	6 channels reload 1 timer

Table 6-6 PWM and BPWM Features Different Table

新唐科技 NUVOTON INTELLECTUAL PROPERTY

6.11 UART Interface Controller (UART)

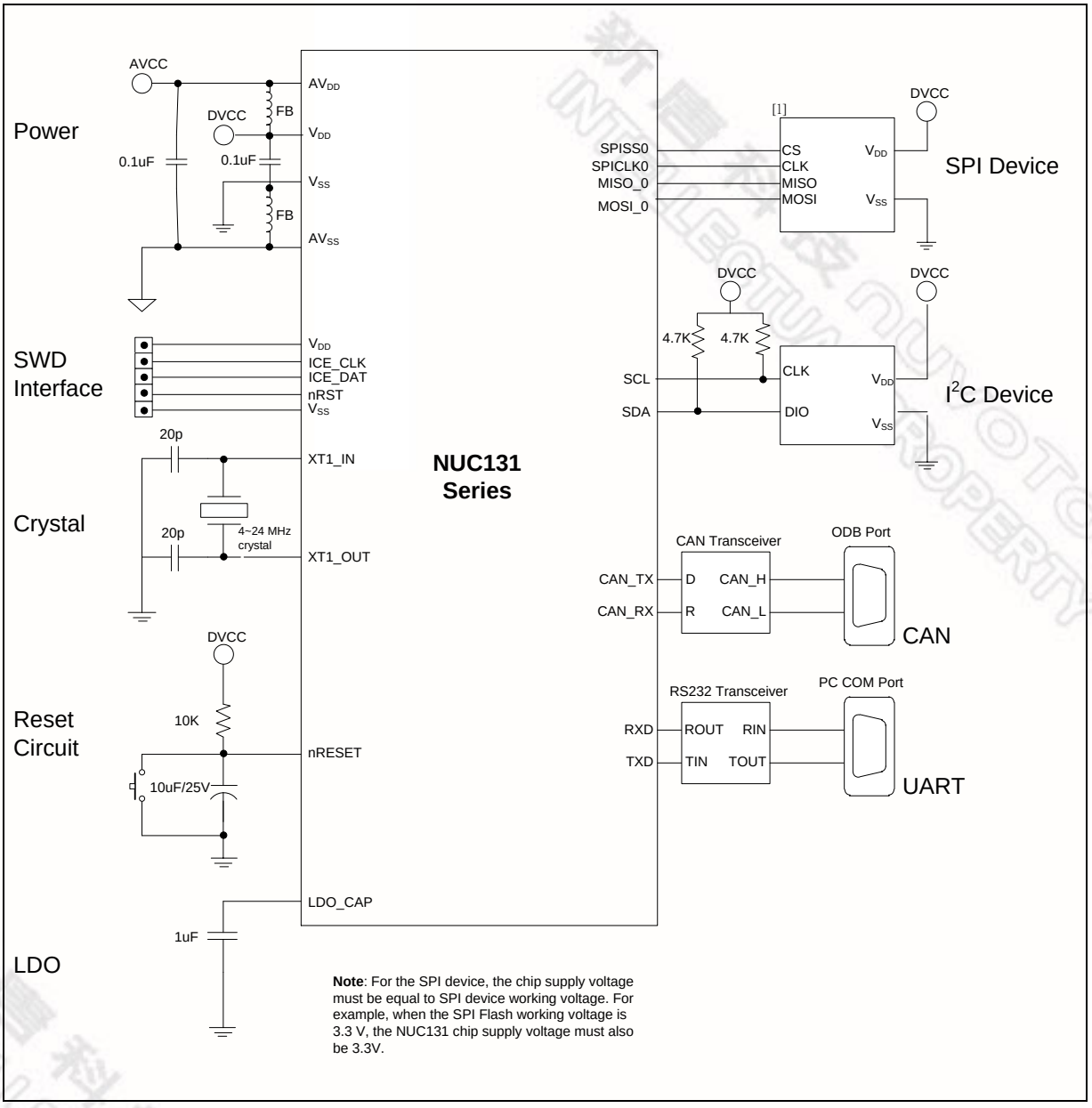
6.11.1 Overview

The NuMicro™ NUC131 series provides up to six channels of Universal Asynchronous Receiver/Transmitters (UART). UART0/UART1/UART2 supports 16 bytes entry FIFO and UART3/UART4/UART5 support 1 byte buffer for data payload. Besides, only UART0 and UART1 support the flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function. UART0/UART1 provides RS-485 function mode. UART0/UART1/UART2 provides LIN master/slave function.

6.11.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16/16 bytes (UART0/UART1/UART2 support) entry FIFO and 1/1 bytes buffer for data payloads (UART3/UART4/UART5 support)
- Supports hardware auto-flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0/UART1 support).
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0/UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- LIN function mode (UART0/UART1/UART2 support)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode. (UART0/UART1 support)
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin.

7 APPLICATION CIRCUIT



Note: For the SPI device, the chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the NUC131 chip supply voltage must also be 3.3V.

新唐科技 NUVOTON INTELLECTUAL PROPERTY

8.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=5.5 V, T_A = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation Voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5V ~ 5.5V up to 50 MHz				
Power Ground	V_{SS} AV_{SS}	-0.3	0	0.3	V					
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} ≥ 2.5V				
Band-gap Voltage	V_{BG}		1.20		V	V_{DD} = 2.5 V ~ 5.5 V, T_A = 25°C				
		1.19	1.20	1.22	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = -40°C~105°C				
Analog Operating Voltage	AV_{DD}		V_{DD}		V	When system used analog function, please refer to TRM chapter 6.5 for corresponding analog operating voltage				
Operating Current Normal Run Mode at 50 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD1}		26		mA	V_{DD}	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{DD2}		12		mA	5.5V	12 MHz	X	V	X
	I_{DD3}		24		mA	3.3V	12 MHz	X	V	V
	I_{DD4}		11		mA	3.3V	12 MHz	X	V	X
Operating Current Normal Run Mode at 22.1184 MHz while(1){} executed from flash VLDO =1.8 V	I_{DD5}	-	10	-	mA	5.5V	X	V	X	V
	I_{DD6}	-	4.1	-	mA	5.5V	X	V	X	X
	I_{DD7}	-	10	-	mA	3.3V	X	V	X	V
	I_{DD8}	-	4.1	-	mA	3.3V	X	V	X	X
Operating Current Normal Run Mode at 12 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD9}		8.3		mA	5.5V	12 MHz	X	X	V
	I_{DD10}		4.3		mA	5.5V	12 MHz	X	X	X
	I_{DD11}		6.8		mA	3.3V	12 MHz	X	X	V
	I_{DD12}		2.8		mA	3.3V	12 MHz	X	X	X
Operating Current Normal Run Mode at 4 MHz while(1){} executed from flash V_{LDO} =1.8 V	I_{DD13}		3.9		mA	5.5V	4 MHz	X	X	V
	I_{DD14}		2.6		mA	5.5V	4 MHz	X	X	X
	I_{DD15}		2.6		mA	3.3V	4 MHz	X	X	V
	I_{DD16}		1.3		mA	3.3V	4 MHz	X	X	X
Operating Current	I_{DD21}		111		μA	VDD	HXT/LXT	LIRC (kHz)	PLL	All digital module

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Normal Run Mode at 10 kHz while(1){} executed from flash VLDO =1.8 V						5.5V	X	10	X	V
	I_{DD22}		108		µA	5.5V	X	10	X	X
	I_{DD23}		98		µA	3.3V	X	10	X	V
	I_{DD24}		96		µA	3.3V	X	10	X	X
Operating Current Idle Mode at 50 MHz VLDO =1.8 V	I_{IDLE1}		21		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12 MHz	X	V	V
	I_{IDLE2}		8		mA	5.5V	12 MHz	X	V	X
	I_{IDLE3}		20		mA	3.3V	12 MHz	X	V	V
	I_{IDLE4}		6.7		mA	3.3V	12 MHz	X	V	X
Operating Current Idle Mode at 22.1184 MHz VLDO =1.8 V	I_{IDLE5}	-	7.7	-	mA	5.5V	X	V	X	X
	I_{IDLE6}	-	2.1	-	mA	5.5V	X	V	X	X
	I_{IDLE7}	-	7.7	-	mA	3.3V	X	V	X	V
	I_{IDLE8}	-	2.1	-	mA	3.3V	X	V	X	X
Operating Current Idle Mode at 12 MHz V_{LDO} =1.8 V	I_{IDLE9}		7.3		mA	5.5V	12 MHz	X	X	V
	I_{IDLE10}		3.2		mA	5.5V	12 MHz	X	X	X
	I_{IDLE11}		5.8		mA	3.3V	12 MHz	X	X	V
	I_{IDLE12}		1.7		mA	3.3V	12 MHz	X	X	X
Operating Current Idle Mode at 4 MHz V_{LDO} =1.8 V	I_{IDLE13}		3.6		mA	5.5V	4 MHz	X	X	V
	I_{IDLE14}		2.2		mA	5.5V	4 MHz	X	X	X
	I_{IDLE15}		2.3		mA	3.3V	4 MHz	X	X	V
	I_{IDLE16}		0.96		mA	3.3V	4 MHz	X	X	X
Operating Current Idle Mode at 10 kHz	I_{IDLE21}		110		µA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						5.5V	X	10	X	V
	I_{IDLE22}		107		µA	5.5V	X	10	X	X
	I_{IDLE23}		97		µA	3.3V	X	10	X	V
	I_{IDLE24}		95		µA	3.3V	X	10	X	X
Standby Current Power-down Mode (Deep Sleep Mode) V_{LDO} =1.6 V	I_{PWD1}		15		µA	V_{DD}	HXT/HIRC PLL	LXT (kHz)	RTC	RAM retension
						5.5V	X	X	X	V
	I_{PWD2}		15		µA	5.5V	X	X	X	V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{PWD3}		17		µA	3.3V	X	32.768	V	V
	I_{PWD4}		17		µA	3.3V	X	32.768	V	V
	I_{PWD5}		10		µA	5.5V	X	X	X	X
	I_{PWD6}		9		µA	3.3V	X	X	X	X
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-67	-75	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}				
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-1	-	+1	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD} Open-drain or input only mode.				
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]		-610	-650	µA	V_{DD} = 5.5V, V_{IN}=2.0V				
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V				
		-0.3	-	0.6		V_{DD} = 2.5V				
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V				
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V				
Input Low Voltage XT1_IN[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V				
		0	-	0.4		V_{DD} = 3.0V				
Input High Voltage XT1_IN[*2]	V_{IH3}	3.5	-	V_{DD} +0.3	V	V_{DD} = 5.5V				
		2.4	-	V_{DD} +0.3		V_{DD} = 3.0V				
Negative going threshold (Schmitt input), nRESET	V_{ILS}	-0.3	-	0.2V_{DD}	V					
Positive going threshold (Schmitt input), nRESET	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V					
Internal nRESET pin pull up resistor	R_{RST}	40		150	kΩ					
Negative going threshold (Schmitt input),	V_{ILS}	-0.3	-	0.3 VDD	V					
Positive going threshold (Schmitt input),	V_{IHS}	0.7 V_{DD}	-	V_{DD} +0.3	V					

8.4.3 Low Voltage Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Quiescent Current	AV_{DD}=5.5 V	-	1	5	μA
I_{LVR}	Operation Temperature	-	-40	25	105	℃
V_{LVR}	Threshold Voltage	TA = 25 ℃	2.00	2.0	2.4	V
		TA = -40 ℃	1.95	1.98	2.02	V
		TA = 105 ℃	2.04	2.13	2.25	V

8.4.4 Brown-out Detector Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AV_{DD}	Operation Voltage	-	0	-	5.5	V
T_A	Temperature	-	-40	25	105	℃
I_{BOD}	Quiescent Current	AVDD=5.5 V	-	-	140	μA
V_{BOD}	Brown-out Voltage (Falling edge)	BOD_VL[1:0]=11	4.45	4.53	4.56	V
		BOD_VL [1:0]=10	3.74	3.8	3.84	V
		BOD_VL [1:0]=01	2.73	2.77	2.8	V
		BOD_VL [1:0]=00	2.22	2.25	2.28	V
V_{BOD}	Brown-out Voltage (Rising edge)	BOD_VL[1:0]=11	4.34	4.39	4.41	V
		BOD_VL [1:0]=10	3.65	3.69	3.71	V
		BOD_VL [1:0]=01	2.66	2.69	2.7	V
		BOD_VL [1:0]=00	2.16	2.19	2.2	V

8.4.5 Power-on Reset Specification

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
T_A	Operation Temperature	-	-40	25	105	℃
V_{POR}	Reset Voltage	V+	1.6	2	2.4	V
V_{POR}	VDD Start Voltage to Ensure Power-on Reset	-	-	-	100	mV
RR_{VDD}	VDD Raising Rate to Ensure Power-on Reset	-	0.025	-	-	V/ms
t_{POR}	Minimum Time for VDD Stays at VPOR to Ensure Power-on Reset	-	0.5	-	-	ms

8.8 I2S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I^2S clock high time	42	-	ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I^2S clock low time	37	-		
$t_{v(WS)}$	WS valid time	7	-		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	34	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I^2S slave input clock duty cycle	25	75	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	0	-	ns	Master receiver
$t_{su(SD\_SR)}$		0	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	0	-		Master receiver
$t_{h(SD\_SR)}$		0	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	32		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	16	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	5		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

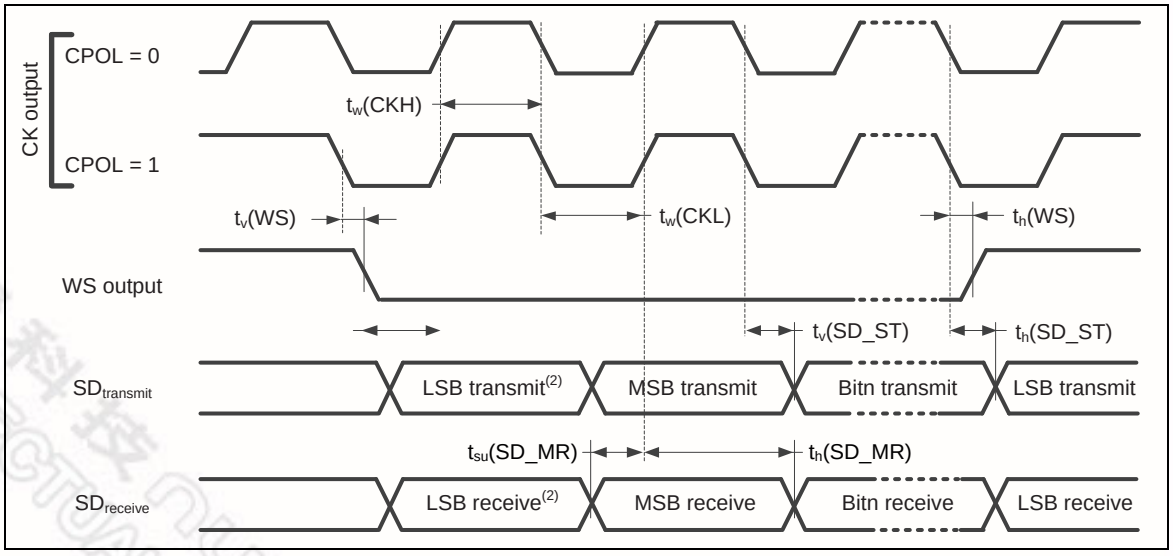


Figure 8-7 I2S Master Mode Timing Diagram

NUMICRO™ NUC131 SERIES DATASHEET

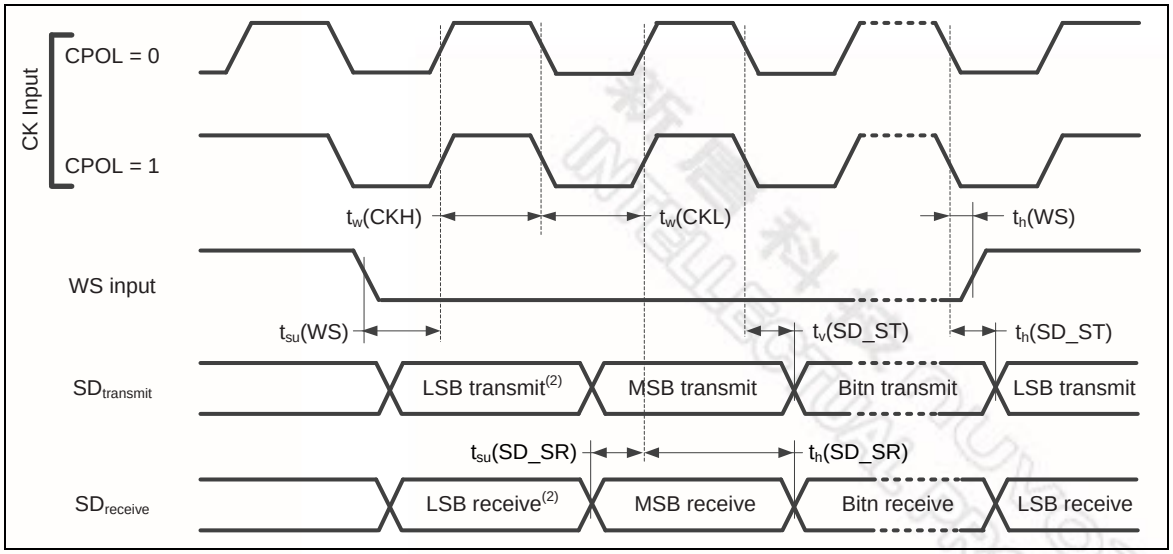


Figure 8-8 I2S Slave Mode Timing Diagram

NUMICRO™ NUC131 SERIES DATASHEET

新唐科技 NUVOTON INTELLECTUAL PROPERTY