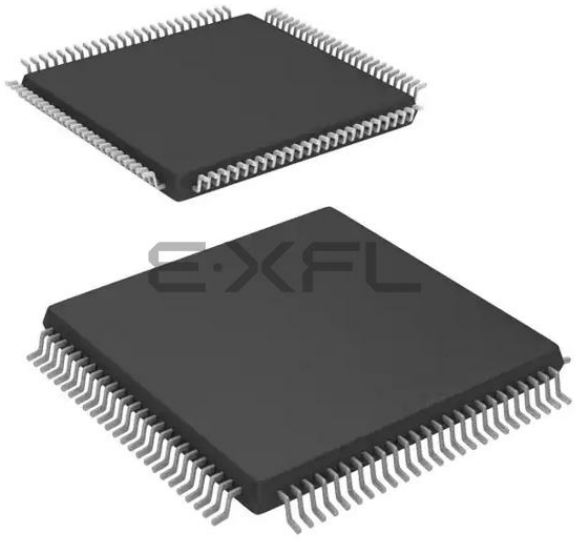

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Host/Peripheral Controller
Core Processor	CY16
Program Memory Type	ROM (8kB)
Controller Series	CY7C673xx
RAM Size	16K x 8
Interface	SPI Serial, USB, HPI
Number of I/O	32
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c67300-100axa

Table 1. Interface Options for GPIO Pins

GPIO Pins	HPI	IDE	PWM	HSS	SPI	UART	I2C	OTG
GPIO31							SCL/SDA	
GPIO30							SCL/SDA	
GPIO29								OTGID
GPIO28						TX		
GPIO27						RX		
GPIO26			PWM3	CTS[1]				
GPIO25								
GPIO24	INT	IOREADY						
GPIO23	nRD	IOR						
GPIO22	nWR	IOW						
GPIO21	nCS							
GPIO20	A1	CS1						
GPIO19	A0	CS0						
GPIO18		A2	PWM2	RTS[1]				
GPIO17		A1	PWM1	RXD[1]				
GPIO16		A0	PWM0	TXD[1]				
GPIO15	D15	D15						
GPIO14	D14	D14						
GPIO13	D13	D13						
GPIO12	D12	D12						
GPIO11	D11	D11			MOSI[1]			
GPIO10	D10	D10			SCK[1]			
GPIO9	D9	D9			nSSI[1]			
GPIO8	D8	D8			MISO[1]			
GPIO7	D7	D7						
GPIO6	D6	D6						
GPIO5	D5	D5						
GPIO4	D4	D4						
GPIO3	D3	D3						
GPIO2	D2	D2						
GPIO1	D1	D1						
GPIO0	D0	D0						

Table 2. Interface Options for External Memory Bus Pins

MEM Pins	HPI	IDE	PWM	HSS	SPI	UART	I2C	OTG
D15				CTS[2]				
D14				RTS[2]				
D13				RXD[2]				
D12				TXD[2]				
D11					MOSI[2]			
D10					SCK[2]			
D9					nSSI[2]			
D8					MISO[2]			
D[7:0]								
A[18:0]								
CONTROL								

Notes
1. Default interface location.
2. Alternate interface location.

USB Interface

EZ-Host has two built in Host/Peripheral SIEs and four USB transceivers that meet the USB 2.0 specification requirements for full and low speed (high speed is not supported). In Host mode, EZ-Host supports four downstream ports, each support control, interrupt, bulk, and isochronous transfers. In Peripheral mode, EZ-Host supports one peripheral port with eight endpoints for each of the two SIEs. Endpoint 0 is dedicated as the control endpoint and only supports control transfers. Endpoints 1 though 7 support interrupt, bulk (up to 64 bytes/packet), or isochronous transfers (up to 1023 Bytes/packet size). EZ-Host also supports a combination of Host and Peripheral ports simultaneously as shown in Table 3 on page 5.

Table 3. USB Port Configuration Options

Port Configurations	Port 1A	Port 1B	Port 2A	Port 2B
OTG	OTG	–	–	–
OTG + 2 Hosts	OTG	–	Host	Host
OTG + 1 Host	OTG	–	Host	–
OTG + 1 Host	OTG	–	–	Host
OTG + 1 Peripheral	OTG	–	Peripheral	–
OTG + 1 Peripheral	OTG	–	–	Peripheral
4 Hosts	Host	Host	Host	Host
3 Hosts	Any Combination of Ports			
2 Hosts	Any Combination of Ports			
1 Host	Any Port			
2 Hosts + 1 Peripheral	Host	Host	Peripheral	–
2 Hosts + 1 Peripheral	Host	Host	–	Peripheral
2 Hosts + 1 Peripheral	Peripheral	–	Host	Host
2 Hosts + 1 Peripheral	–	Peripheral	Host	Host
1 Host + 1 Peripheral	Host	–	Peripheral	–
1 Host + 1 Peripheral	Host	–	–	Peripheral
1 Host + 1 Peripheral	–	Host	–	Peripheral
1 Host + 1 Peripheral	–	Host	Peripheral	–
1 Host + 1 Peripheral	Peripheral	–	Host	–
1 Host + 1 Peripheral	Peripheral	–	–	Host
1 Host + 1 Peripheral	–	Peripheral	–	Host
1 Host + 1 Peripheral	–	Peripheral	Host	–
2 Peripherals	Peripheral	–	Peripheral	–
2 Peripherals	Peripheral	–	–	Peripheral
2 Peripherals	–	Peripheral	–	Peripheral
2 Peripherals	–	Peripheral	Peripheral	–
1 Peripheral	Any Port			

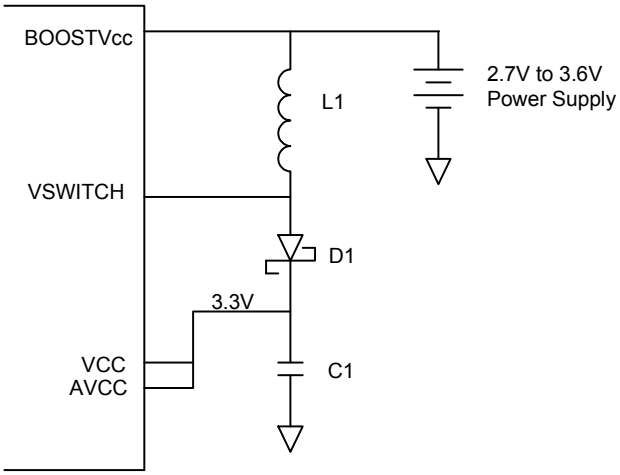
USB Features

- USB 2.0-compliant for full and low speed
- Up to four downstream USB host ports
- Up to two upstream USB peripheral ports
- Configurable endpoint buffers (pointer and length), must reside in internal RAM
- Up to eight available peripheral endpoints (one control endpoint)
- Supports control, interrupt, bulk, and isochronous transfers
- Internal DMA channels for each endpoint
- Internal pull up and pull down resistors
- Internal series termination resistors on USB data lines

Booster Interface

EZ-Host has an on chip power booster circuit for use with power supplies that range between 2.7V and 3.6V. The booster circuit boosts the power to 3.3V nominal to supply power for the entire chip. The booster circuit requires an external inductor, diode, and capacitor. During power down mode, the circuit is disabled to save power. Figure 6 shows how to connect the booster circuit.

Figure 6. Power Supply Connection With Booster

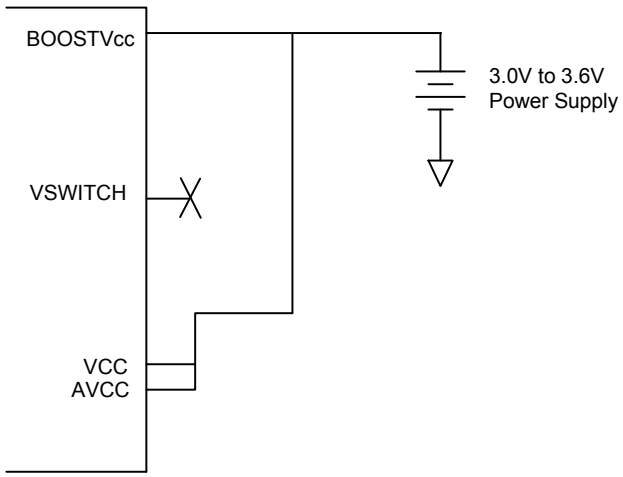


Component details:

- L1: Inductor with inductance of 10 µH and a current rating of at least 250 mA
- D1: Schottky diode with a current rating of at least 250 mA
- C1: Tantalum or ceramic capacitor with a capacitance of at least 2.2 µF

Figure 7 shows how to connect the power supply when the booster circuit is not being used.

Figure 7. Power Supply Connection Without Booster



Booster Pins

Table 17. Charge Pump Interface Pins

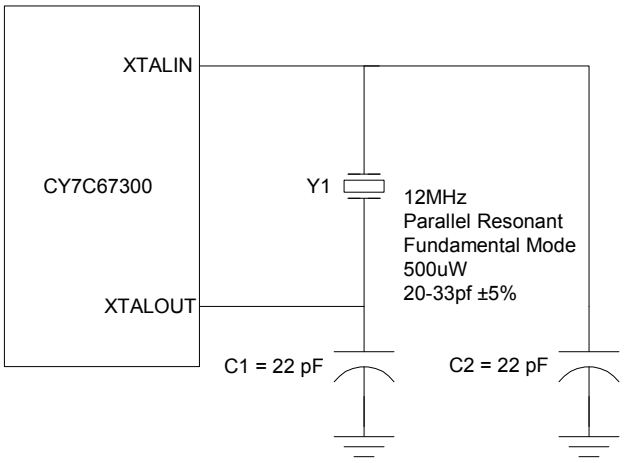
Pin Name	Pin Number
BOOSTVcc	16
VSWITCH	14

Crystal Interface

The recommended crystal circuit to be used with EZ-Host is shown in Figure 8 If an oscillator is used instead of a crystal circuit, connect it to XTALIN and leave XTALOUT unconnected. For further information about the crystal requirements, see Table 132 on page 90.

Noted that the CLKSEL pin (pin 38) is sampled after reset to determine what crystal or clock source frequency is used. For normal operation, 12 MHz is required so the CLKSEL pin must have a 47K ohm pull up resistor to V_{CC}.

Figure 8. Crystal Interface



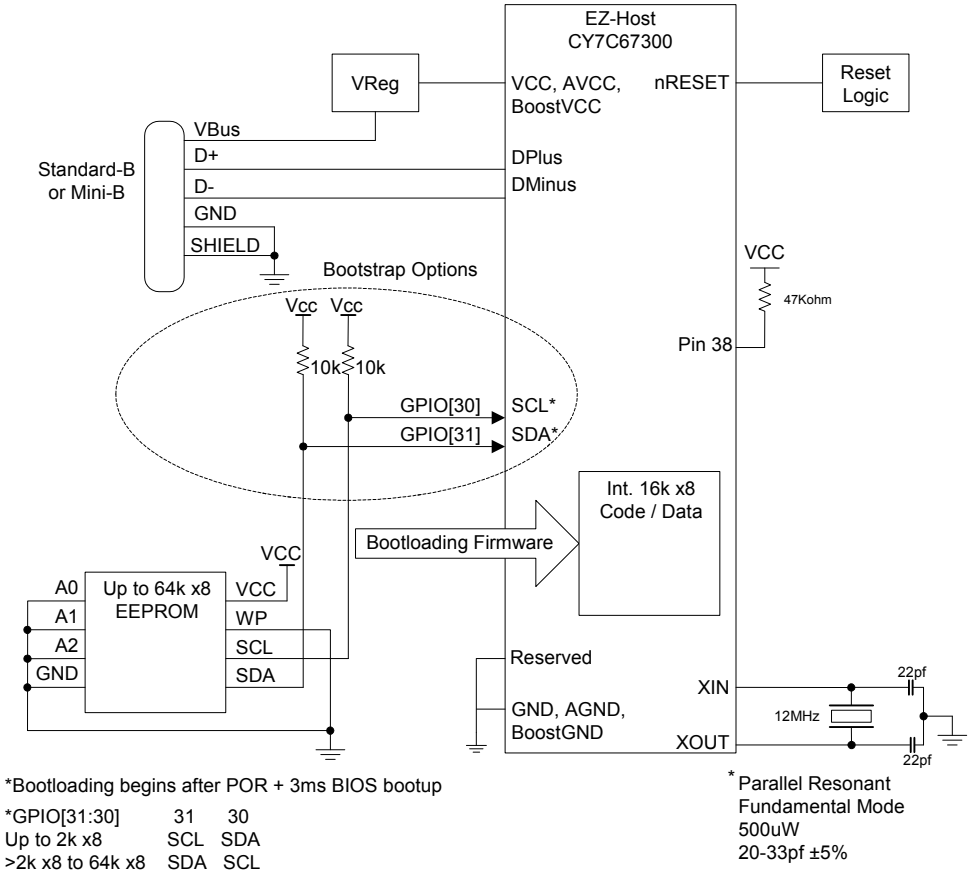
Crystal Pins

Table 18. Crystal Pins

Pin Name	Pin Number
XTALIN	29
XTALOUT	28

Minimum Hardware Requirements for Standalone Mode – Peripheral Only

Figure 9. Minimum Standalone Hardware Configuration – Peripheral Only



Power Savings and Reset Description

This sections describes the different modes for resetting the chip and ways to save power.

Power Saving Mode Description

EZ-Host has one main power saving mode, Sleep. For detailed information about Sleep mode, see the Sleep section that follows.

Sleep mode is used for USB applications to support USB suspend and non USB applications as the main chip power down mode.

In addition, EZ-Host is capable of slowing down the CPU clock speed through the CPU Speed register [0xC008] without affecting other peripheral timing. Reducing the CPU clock speed from 48 MHz to 24 MHz reduces the overall current draw by around 8 mA while reducing it from 48 MHz to 3 MHz reduces the overall current draw by approximately 15 mA.

Sleep

Sleep mode is the main chip power down mode and is also used for USB suspend. Sleep mode is entered by setting the Sleep Enable (bit 1) of the Power control register [0xC00A]. During Sleep mode (USB Suspend) the following events and states are true:

- GPIO pins maintain their configuration during sleep (in suspend)
- External Memory address pins are driven low
- XTALOUT is turned off
- Internal PLL is turned off
- Ensure that firmware disables the charge pump (OTG Control register [0xC098]) thereby causing OTGVBUS to drop below 0.2V. Otherwise OTGVBUS only drops to V_{CC} – (2 schottky diode drops).
- Booster circuit is turned off
- USB transceivers is turned off
- CPU goes into suspend mode until a programmable wakeup event

External (Remote) Wakeup Source

There are several possible events available to wake EZ-Host from Sleep mode as shown in Table 20. These may also be used as remote wakeup options for USB applications. See the Power Control Register [0xC00A] [R/W] on page 21 for details.

Upon wakeup, code begins executing within 200 µs, the time it takes the PLL to stabilize.

Table 20. Wakeup Sources [7, 8]

Wakeup Source (if enabled)	Event
USB Resume	D+/D– Signaling
OTGVBUS	Level
OTGID	Any Edge
HPI	Read
HSS	Read
SPI	Read
IRQ1 (GPIO 25)	Any Edge
IRQ0 (GPIO 24)	Any Edge

Power-On-Reset Description

The length of the power-on-reset event can be defined by (V_{CC} ramp to valid) + (Crystal startup). A typical application might use a 12 ms power-on-reset event = ~7 ms + ~5 ms, respectively.

Reset Pin

The Reset pin is active low and requires a minimum pulse duration of sixteen 12 MHz clock cycles (1.3 µs). A reset event restores all registers to their default POR settings. Code execution then begins 200 µs later at 0xFF00 with an immediate jump to 0xE000, the start of BIOS. Refer to BIOS documentation for additional details.

USB Reset

A USB Reset affects registers 0xC090 and 0xC0B0, all other registers remain unchanged.

Memory Map

The memory map is discussed in the following sections.

Mapping

The total memory space directly addressable by the CY16 processor is 64K (0x0000-0xFFFF). Program, data, and IO are contained within this 64K space. This memory space is byte addressable. Figure 10 on page 17 shows the various memory region address locations.

Internal Memory

Of the internal memory, 15K bytes are allocated for user's program and data. The lower memory space from 0x0000 to 0x04A2 is reserved for interrupt vectors, general purpose registers, USB control registers, stack, and other BIOS variables. The upper internal memory space contains EZ-Host control registers from 0xC000 to 0xC0FF and the BIOS ROM itself from 0xE000 to 0xFFFF. For more information about the reserved lower memory or the BIOS ROM, refer to the Programmer's documentation and/or the BIOS documentation.

During development with the EZ-Host toolset, leave the lower area of user's space (0x04A4 to 0x1000) available to load the GDB stub. The GDB stub is required to allow the toolset debug access into EZ-Host.

The chip select pins are not active during accesses to internal memory.

External Memory

Up to 32 KB of external memory from 0x4000 - 0xBFFF is available via one chip select line (nXRAMSEL) with RAM Merge enabled (BIOS default). Additionally, another 8 KB region from 0xC100 - 0xDFFF is available via a second chip select line (nXROMSEL) giving 40 KB of total available external memory. Together with the internal 15 KB, this gives a total of either ~48 KB (one chip select) or ~56 KB (two chip selects) of available memory for either code or data.

Note that the memory map and pin names (nXRAMSEL/ nXROMSEL) define specific memory regions for RAM vs. ROM. This allows the BIOS to look in the upper external memory space at 0xC100 for SCAN vectors (enabling code to be loaded/ executed from ROM). If no SCAN vectors are required in the design (external memory is used exclusively for data), then all external memory regions can be used for RAM. Similarly, the external memory can be used exclusively for code space (ROM).

If more external memory is required, EZ-Host has enough address lines to support up to 512 KB. However, this requires complex code banking/paging schemes via the Extended Page registers.

For further information about setting up the external memory, see the External Memory Interface on page 6.

Notes
7. Read data is discarded (dummy data).
8. HPI_INT asserts on a USB Resume.

Bank Register [0xC002] [R/W]

Table 23. Bank Register

Bit #	15	14	13	12	11	10	9	8
Field	Address...							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	...Address			Reserved				
Read/Write	R/W	R/W	R/W	-	-	-	-	-
Default	0	0	0	X	X	X	X	X

Register Description

The Bank register maps registers R0–R15 into RAM. The eleven MSBs of this register are used as a base address for registers R0–R15. A register address is automatically generated by:

1. Shifting the four LSBs of the register address left by 1.
2. ORing the four shifted bits of the register address with the twelve MSBs of the Bank register.
3. Forcing the LSB to zero.

For example, if the Bank register is left at its default value of 0x0100, and R2 is read, then the physical address 0x0102 is read. Refer to Table 24 for details.

Table 24. Bank Register Example

Register	Hex Value	Binary Value
Bank	0x0100	0000 0001 0000 0000
R14	0x000E << 1 = 0x001C	0000 0000 0001 1100
RAM Location	0x011C	0000 0001 0001 1100

Address (Bits [15:4])

The Address field is used as a base address for all register addresses to start from.

Reserved

Write all reserved bits with ’0’.

Hardware Revision Register [0xC004] [R]

Table 25. Revision Register

Bit #	15	14	13	12	11	10	9	8
Field	Revision...							
Read/Write	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	...Revision							
Read/Write	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Register Description

The Hardware Revision register is a read only register that indicates the silicon revision number. The first silicon revision is represented by 0x0101. This number is increased by one for each new silicon revision.

Revision (Bits [15:0])

The Revision field contains the silicon revision number.

Host n Control Register [R/W]

■ Host 1 Control Register 0xC080

■ Host 2 Control Register 0xC0A0

Table 48. Host n Control Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved							
Read/Write	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	Preamble Enable	Sequence Select	Sync Enable	ISO Enable	Reserved			Arm Enable
Read/Write	R/W	R/W	R/W	R/W	-	-	-	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The Host n Control register allows high level USB transaction control.

Preamble Enable (Bit 7)

The Preamble Enable bit enables or disables the transmission of a preamble packet before all low-speed packets. Set this bit only when communicating with a low-speed device.

1: Enable Preamble packet

0: Disable Preamble packet

Sequence Select (Bit 6)

The Sequence Select bit sets the data toggle for the next packet. This bit has no effect on receiving data packets; sequence checking must be handled in firmware.

1: Send DATA1

0: Send DATA0

Sync Enable (Bit 5)

The Sync Enable bit synchronizes the transfer with the SOF packet in full-speed mode and the EOP packet in low-speed mode.

1: The next enabled packet is transferred after the SOF or EOP packet is transmitted

0: The next enabled packet is transferred as soon as the SIE is free

ISO Enable (Bit 4)

The ISO Enable bit enables or disables an isochronous transaction.

1: Enable isochronous transaction

0: Disable isochronous transaction

Arm Enable (Bit 0)

The Arm Enable bit arms an endpoint and starts a transaction. This bit is automatically cleared to ‘0’ when a transaction is complete.

1: Arm endpoint and begin transaction

0: Endpoint disarmed

Reserved

Write all reserved bits with ’0’.

The ACK Flag bit indicates two different conditions depending on the transfer type. For non-isochronous transfers, this bit represents a transaction ending by receiving or sending an ACK packet. For isochronous transfers, this bit represents a successful transaction that is not represented by an ACK packet.

1: For non-isochronous transfers, the transaction was ACKed. For isochronous transfers, the transaction was completed successfully

0: For non-isochronous transfers, the transaction was not ACKed. For isochronous transfers, the transaction did not complete successfully

Host n PID Register [W]

- Host 1 PID Register 0xC086
- Host 2 PID Register 0xC0A6

Table 53. Host n PID Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved							
Read/Write	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	PID Select				Endpoint Select			
Read/Write	W	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

Register Description

The Host n PID register is a write only register that provides the PID and Endpoint information to the USB SIE to be used in the next transaction.

PID Select (Bits [7:4])

The PID Select field is defined in Table 54. ACK and NAK tokens are automatically sent based on settings in the Host n Control register and do not need to be written in this register.

Table 54. PID Select Definition

PID TYPE	PID Select [7:4]
SETUP	1101 (D Hex)
IN	1001 (9 Hex)
OUT	0001 (1 Hex)
SOF	0101 (5 Hex)
PREAMBLE	1100 (C Hex)
NAK	1010 (A Hex)
STALL	1110 (E Hex)
DATA0	0011 (3 Hex)
DATA1	1011 (B Hex)

Endpoint Select (Bits [3:0])

The Endpoint field allows addressing of up to 16 different endpoints.

Reserved

Write all reserved bits with ’0’.

Host n Count Result Register [R]

- Host 1 Count Result Register 0xC088
- Host 2 Count Result Register 0xC0A8

Table 55. Host n Count Result Register

Bit #	15	14	13	12	11	10	9	8
Field	Result...							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Result							
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Register Description

The Host n Count Result register is a read only register that contains the size difference in bytes between the Host Count Value specified in the Host n Count register and the last packet received. If an overflow or underflow condition occurs, that is the received packet length differs from the value specified in the Host n Count register, the Length Exception Flag bit in the Host n Endpoint Status register is set. The value in this register is only value when the Length Exception Flag bit is set and the Error Flag bit is not set, both bits are in the Host n Endpoint Status register.

Result (Bits [15:0])

The Result field contains the differences in bytes between the received packet and the value specified in the Host n Count register. If an overflow condition occurs, Result [15:10] is set to ‘111111’, a 2’s complement value indicating the additional byte count of the received packet. If an underflow condition occurs, Result [15:0] indicates the excess bytes count (number of bytes not used).

Reserved

Write all reserved bits with ’0’.

Device n Endpoint n Status Register [R/W]

- Device n Endpoint 0 Status Register [Device 1: 0x0206 Device 2: 0x0286]
- Device n Endpoint 1 Status Register [Device 1: 0x0216 Device 2: 0x0296]
- Device n Endpoint 2 Status Register [Device 1: 0x0226 Device 2: 0x02A6]
- Device n Endpoint 3 Status Register [Device 1: 0x0236 Device 2: 0x02B6]
- Device n Endpoint 4 Status Register [Device 1: 0x0246 Device 2: 0x02C6]
- Device n Endpoint 5 Status Register [Device 1: 0x0256 Device 2: 0x02D6]
- Device n Endpoint 6 Status Register [Device 1: 0x0266 Device 2: 0x02E6]
- Device n Endpoint 7 Status Register [Device 1: 0x0276 Device 2: 0x02F6]

Table 66. Device n Endpoint n Status Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved				Overflow Flag	Underflow Flag	OUT Exception Flag	IN Exception Flag
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

Bit #	7	6	5	4	3	2	1	0
Field	Stall Flag	NAK Flag	Length Exception Flag	Setup Flag	Sequence Flag	Timeout Flag	Error Flag	ACK Flag
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

Register Description

The Device n Endpoint n Status register provides packet status information for the last transaction received or transmitted. This register is updated in hardware and does not need to be cleared by firmware. There are a total of eight endpoints for each of the two ports. All endpoints have the same definition for their Device n Endpoint n Status register.

The Device n Endpoint n Status register is a memory based register that must be initialized to 0x0000 before USB Device operations are initiated. After initialization, do not write to this register again.

Overflow Flag (Bit 11)

The Overflow Flag bit indicates that the received data in the last data transaction exceeded the maximum length specified in the Device n Endpoint n Count register. The Overflow Flag must be checked in response to a Length Exception signified by the Length Exception Flag set to '1'.

1: Overflow condition occurred

0: Overflow condition did not occur

Underflow Flag (Bit 10)

The Underflow Flag bit indicates that the received data in the last data transaction was less then the maximum length specified in the Device n Endpoint n Count register. The Underflow Flag must be checked in response to a Length Exception signified by the Length Exception Flag set to '1'.

1: Underflow condition occurred

0: Underflow condition did not occur

OUT Exception Flag (Bit 9)

The OUT Exception Flag bit indicates when the device received an OUT packet when armed for an IN.

1: Received OUT when armed for IN

0: Received IN when armed for IN

IN Exception Flag (Bit 8)

The IN Exception Flag bit indicates when the device received an IN packet when armed for an OUT.

1: Received IN when armed for OUT

0: Received OUT when armed for OUT

Stall Flag (Bit 7)

The Stall Flag bit indicates that a Stall packet was sent to the host.

1: Stall packet was sent to the host

0: Stall packet was not sent

NAK Flag (Bit 6)

The NAK Flag bit indicates that a NAK packet was sent to the host.

1: NAK packet was sent to the host

0: NAK packet was not sent

Length Exception Flag (Bit 5)

The Length Exception Flag bit indicates the received data in the data stage of the last transaction does not equal the maximum Endpoint Count specified in the Device n Endpoint n Count register. A Length Exception can either mean an overflow or

Device n Interrupt Enable Register [R/W]

- Device 1 Interrupt Enable Register 0xC08C
- Device 2 Interrupt Enable Register 0xC0AC

Table 69. Device n Interrupt Enable Register

Bit #	15	14	13	12	11	10	9	8
Field	VBUS Interrupt Enable	ID Interrupt Enable	Reserved		SOF/EOP Timeout Interrupt Enable	Reserved	SOF/EOP Interrupt Enable	Reset Interrupt Enable
Read/Write	R/W	R/W	-	-	R/W	-	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	EP7 Interrupt Enable	EP6 Interrupt Enable	EP5 Interrupt Enable	EP4 Interrupt Enable	EP3 Interrupt Enable	EP2 Interrupt Enable	EP1 Interrupt Enable	EP0 Interrupt Enable
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description [12]

The Device n Interrupt Enable register provides control over device related interrupts including eight different endpoint interrupts.

VBUS Interrupt Enable (Bit 15)

The VBUS Interrupt Enable bit enables or disables the OTG VBUS interrupt. When enabled, this interrupt triggers on both the rising and falling edge of VBUS at the 4.4V status (only supported in Port 1A). This bit is only available for Device 1 and is a reserved bit in Device 2.

1: Enable VBUS interrupt

0: Disable VBUS interrupt

ID Interrupt Enable (Bit 14)

The ID Interrupt Enable bit enables or disables the OTG ID interrupt. When enabled, this interrupt triggers on both the rising and falling edge of the OTG ID pin (only supported in Port 1A). This bit is only available for Device 1 and is a reserved bit in Device 2.

1: Enable ID interrupt

0: Disable ID interrupt

SOF/EOP Timeout Interrupt Enable (Bit 11)

The SOF/EOP Timeout Interrupt Enable bit enables or disables the SOF/EOP Timeout Interrupt. When enabled this interrupt triggers when the USB host fails to send a SOF or EOP packet within the time period specified in the Device n SOF/EOP Count register. In addition, the Device n Frame register counts the number of times the SOF/EOP Timeout Interrupt triggers between receiving SOF/EOPs.

1: SOF/EOP timeout occurred

0: SOF/EOP timeout did not occur

SOF/EOP Interrupt Enable (Bit 9)

The SOF/EOP Interrupt Enable bit enables or disables the SOF/EOP received interrupt.

1: Enable SOF/EOP received interrupt

0: Disable SOF/EOP received interrupt

Reset Interrupt Enable (Bit 8)

The Reset Interrupt Enable bit enables or disables the USB Reset Detected interrupt

1: Enable USB Reset Detected interrupt

0: Disable USB Reset Detected interrupt

EP7 Interrupt Enable (Bit 7)

The EP7 Interrupt Enable bit enables or disables endpoint seven (EP7) Transaction Done interrupt. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied Endpoint: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, the NAK Interrupt Enable bit in the Device n Endpoint Control register can also be set so that NAK responses trigger this interrupt.

1: Enable EP7 Transaction Done interrupt

0: Disable EP7 Transaction Done interrupt

EP6 Interrupt Enable (Bit 6)

The EP6 Interrupt Enable bit enables or disables endpoint six (EP6) Transaction Done interrupt. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied Endpoint: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, the NAK Interrupt Enable bit in the Device n Endpoint Control register can also be set so that NAK responses trigger this interrupt.

1: Enable EP6 Transaction Done interrupt

0: Disable EP6 Transaction Done interrupt

Note

12. Errata: USB peripheral designs may miss endpoint interrupts when receiving Endpoint 0 (EP0) Control transfer requests mixed with other endpoint transfer type transactions. When an SIE is configured as a peripheral, data toggle corruption as specified in the USB 2.0 specification, section 8.6.4, does not work as specified. Please refer to Errata on page 107 for details and workaround.

IDE PIO Port Registers [0xC050 - 0xC06F] [R/W]

All IDE PIO Port registers [0xC050 - 0xC06F] in Table 88 are defined in detail in the Information Technology-AT Attachment -4 with Packet Interface Extension (ATA/ATAPI-4) Specification, T13/1153D Rev 18. The table Address column denotes the CY7C67300 register address for the corresponding ATA/ATAPI register. The IDE_nCS[1:0] field defines the ATA interface CS addressing bits and the IDE_A[2:0] field define the ATA interface address bits. The combination of IDE_nCS and IDE_A are the ATA interface register address.

Table 88. IDE PIO Port Registers

Address	ATA/ATAPI Register	IDE_nCS[1:0]	IDE_A[2:0]
0xC050	DATA Register	‘10’	‘000’
0xC052	Read: Error Register Write: Feature Register	‘10’	‘001’
0xC054	Sector Count Register	‘10’	‘010’
0xC056	Sector Number Register	‘10’	‘011’
0xC058	Cylinder Low Register	‘10’	‘100’
0xC05A	Cylinder High Register	‘10’	‘101’
0xC05C	Device/Head Register	‘10’	‘110’
0xC05E	Read: Status Register Write: Command Register	‘10’	‘111’
0xC060	Not Defined	‘01’	‘000’
0xC062	Not Defined	‘01’	‘001’
0xC064	Not Defined	‘01’	‘010’
0xC066	Not Defined	‘01’	‘011’
0xC068	Not Defined	‘01’	‘100’
0xC06A	Not Defined	‘01’	‘101’
0xC06C	Read: Alternate Status Register Write: Device Control Register	‘01’	‘110’
0xC06E	Not Defined	‘01’	‘111’

HSS Registers

There are eight registers dedicated to HSS operation. Each of these registers are covered in this section and summarized in Table 89.

Table 89. HSS Registers

Register Name	Address	R/W
HSS Control Register	0xC070	R/W
HSS Baud Rate Register	0xC072	R/W
HSS Transmit Gap Register	0xC074	R/W
HSS Data Register	0xC076	R/W
HSS Receive Address Register	0xC078	R/W
HSS Receive Length Register	0xC07A	R/W
HSS Transmit Address Register	0xC07C	R/W
HSS Transmit Length Register	0xC07E	R/W

HSS Control Register [0xC070] [R/W]

Table 90. HSS Control Register

Bit #	15	14	13	12	11	10	9	8
Field	HSS Enable	RTS Polarity Select	CTS Polarity Select	XOFF	XOFF Enable	CTS Enable	Receive Interrupt Enable	Done Interrupt Enable
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	Transmit Done Interrupt Enable	Receive Done Interrupt Enable	One Stop Bit	Transmit Ready	Packet Mode Select	Receive Overflow Flag	Receive Packet Ready Flag	Receive Ready Flag
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R	R
Default	0	0	0	0	0	0	0	0

Register Description

The HSS Control register provides high level status and control over the HSS port.

HSS Enable (Bit 15)

The HSS Enable bit enables or disables HSS operation.

1: Enables HSS operation

0: Disables HSS operation

RTS Polarity Select (Bit 14)

The RTS Polarity Select bit selects the polarity of RTS.

1: RTS is true when LOW

0: RTS is true when HIGH

CTS Polarity Select (Bit 13)

The CTS Polarity Select bit selects the polarity of CTS.

1: CTS is true when LOW

0: CTS is true when HIGH

XOFF (Bit 12)

The XOFF bit is a read only bit that indicates if an XOFF was received. This bit is automatically cleared when an XON is received.

1: XOFF received

0: XON received

XOFF Enable (Bit 11)

The XOFF Enable bit enables or disables XON/XOFF software handshaking.

1: Enable XON/XOFF software handshaking

0: Disable XON/XOFF software handshaking

CTS Enable (Bit 10)

The CTS Enable bit enables or disables CTS/RTS hardware handshaking.

1: Enable CTS/RTS hardware handshaking

0: Disable CTS/RTS hardware handshaking

Receive Interrupt Enable (Bit 9)

The Receive Interrupt Enable bit enables or disables the Receive Ready and Receive Packet Ready interrupts.

1: Enable the Receive Ready and Receive Packet Ready interrupts

0: Disable the Receive Ready and Receive Packet Ready interrupts

Done Interrupt Enable (Bit 8)

The Done Interrupt Enable bit enables or disables the Transmit Done and Receive Done interrupts.

1: Enable the Transmit Done and Receive Done interrupts

0: Disable the Transmit Done and Receive Done interrupts

Transmit Done Interrupt Flag (Bit 7)

The Transmit Done Interrupt Flag bit indicates the status of the Transmit Done Interrupt. It sets when a block transmit is finished. To clear the interrupt, write a '1' to this bit.

1: Interrupt triggered

0: Interrupt did not trigger

Receive Done Interrupt Flag (Bit 6)

The Receive Done Interrupt Flag bit indicates the status of the Receive Done Interrupt. It sets when a block transmit is finished. To clear the interrupt, write a '1' to this bit.

1: Interrupt triggered

0: Interrupt did not trigger

One Stop Bit (Bit 5)

The One Stop Bit bit selects between one and two stop bits for transmit byte mode. In receive mode, the number of stop bits may vary and does not need to be fixed.

1: One stop bit

0: Two stop bits

ID to HPI Enable (Bit 14)

The ID to HPI Enable bit routes the OTG ID interrupt to the HPI port instead of the on-chip CPU.

1: Route signal to HPI port

0: Do not route signal to HPI port

SOF/EOP2 to HPI Enable (Bit 13)

The SOF/EOP2 to HPI Enable bit routes the SOF/EOP2 interrupt to the HPI port.

1: Route signal to HPI port

0: Do not route signal to HPI port

SOF/EOP2 to CPU Enable (Bit 12)

The SOF/EOP2 to CPU Enable bit routes the SOF/EOP2 interrupt to the on-chip CPU. Since the SOF/EOP2 interrupt can be routed to both the on-chip CPU and the HPI port, the firmware must ensure only one of the two (CPU, HPI) resets the interrupt.

1: Route signal to CPU

0: Do not route signal to CPU

SOF/EOP1 to HPI Enable (Bit 11)

The SOF/EOP1 to HPI Enable bit routes the SOF/EOP1 interrupt to the HPI port.

1: Route signal to HPI port

0: Do not route signal to HPI port

SOF/EOP1 to CPU Enable (Bit 10)

The SOF/EOP1 to CPU Enable bit routes the SOF/EOP1 interrupt to the on-chip CPU. Since the SOF/EOP1 interrupt can be routed to both the on-chip CPU and the HPI port, the firmware must ensure only one of the two (CPU, HPI) resets the interrupt.

1: Route signal to CPU

0: Do not route signal to CPU

Reset2 to HPI Enable (Bit 9)

The Reset2 to HPI Enable bit routes the USB Reset interrupt that occurs on Device 2 to the HPI port instead of the on-chip CPU.

1: Route signal to HPI port

0: Do not route signal to HPI port

HPI Swap 1 Enable (Bit 8)

Both HPI Swap bits (bits 8 and 0) must be set to identical values. When set to ‘00’, the most significant data byte goes to HPI_D[15:8] and the least significant byte goes to HPI_D[7:0]. This is the default setting. By setting to ‘11’, the most significant data byte goes to HPI_D[7:0] and the least significant byte goes to HPI_D[15:8].

Resume2 to HPI Enable (Bit 7)

The Resume2 to HPI Enable bit routes the USB Resume interrupt that occurs on Host 2 to the HPI port instead of the on-chip CPU.

1: Route signal to HPI port

0: Do not route signal to HPI port

Resume1 to HPI Enable (Bit 6)

The Resume1 to HPI Enable bit routes the USB Resume interrupt that occurs on Host 1 to the HPI port instead of the on-chip CPU.

1: Route signal to HPI port

0: Do not route signal to HPI port

Done2 to HPI Enable (Bit 3)

The Done2 to HPI Enable bit routes the Done interrupt for Host/Device 2 to the HPI port instead of the on-chip CPU.

1: Route signal to HPI port

0: Do not route signal to HPI port

Done1 to HPI Enable (Bit 2)

The Done1 to HPI Enable bit routes the Done interrupt for Host/Device 1 to the HPI port instead of the on-chip CPU.

1: Route signal to HPI port

0: Do not route signal to HPI port

Reset1 to HPI Enable (Bit 1)

The Reset1 to HPI Enable bit routes the USB Reset interrupt that occurs on Device 1 to the HPI port instead of the on-chip CPU.

1: Route signal to HPI port

0: Do not route signal to HPI port

HPI Swap 0 Enable (Bit 0)

Both HPI Swap bits (bits 8 and 0) must be set to identical values. When set to ‘00’, the most significant data byte goes to HPI_D[15:8] and the least significant byte goes to HPI_D[7:0]. This is the default setting. By setting to ‘11’, the most significant data byte goes to HPI_D[7:0] and the least significant byte goes to HPI_D[15:8].

SIEXmsg Register [W]

- SIE1msg Register 0x0144 [15]
- SIE2msg Register 0x0148 [15]

Table 101. SIEXmsg Register

Bit #	15	14	13	12	11	10	9	8
Field	Data...							
Read/Write	W	W	W	W	W	W	W	W
Default	X	X	X	X	X	X	X	X

Bit #	7	6	5	4	3	2	1	0
Field	...Data							
Read/Write	W	W	W	W	W	W	W	W
Default	X	X	X	X	X	X	X	X

Register Description

The SIEXmsg register allows an interrupt to be generated on the HPI port. Any write to this register causes the SIEXmsg flag in the HPI Status Port to go high and also causes an interrupt on the HPI_INTR pin. The SIEXmsg flag is automatically cleared when the HPI port reads from this register.

Data (Bits [15:0])

The Data field[15:0] simply needs to have any value written to it to cause SIExmsg flag in the HPI Status Port to go high.

HPI Mailbox Register [0xC0C6] [R/W]

Table 102. HPI Mailbox Register

Bit #	15	14	13	12	11	10	9	8
Field	Message...							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Message							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The HPI Mailbox register provides a common mailbox between the CY7C67300 and the external host processor.

If enabled, the HPI Mailbox RX Full interrupt triggers when the external host processor writes to this register. When the CY7C67300 reads this register the HPI Mailbox RX Full interrupt is automatically cleared.

If enabled, the HPI Mailbox TX Empty interrupt triggers when the external host processor reads from this register. The HPI Mailbox TX Empty interrupt automatically clears when the CY7C67300 writes to this register.

In addition, when the CY7C67300 writes to this register, the HPI_INTR signal on the HPI port asserts, signaling the external processor that there is data in the mailbox to read. The HPI_INTR signal deasserts when the external host processor reads from this register.

Message (Bits [15:0])

The Message field contains the message that the host processor wrote to the HPI Mailbox register.

Note
15. Errata: The SIE1msg and SIE2msg Registers [0x0144 and 0x0148] are not initialized at power up. Please refer to Errata on page 107 for details and workaround.

Mode Select (Bit 8)

The Mode Select bit selects between continuous PWM cycling and one shot mode. The default is continuous repeat.

1: Enable One Shot mode. The mode runs the number of counter cycles set in the PWM Cycle Count register and then stops.

0: Enable Continuous mode. Runs in continuous mode and starts over after the PWM cycle count is reached.

PWM 3 Polarity Select (Bit 7)

The PWM 3 Polarity Select bit selects the polarity for PWM 3.

1: Sets the polarity to active HIGH or rising edge pulse

0: Sets the polarity to active LOW

PWM 2 Polarity Select (Bit 6)

The PWM 2 Polarity Select bit selects the polarity for PWM 2.

1: Sets the polarity to active HIGH or rising edge pulse

0: Sets the polarity to active LOW

PWM 1 Polarity Select (Bit 5)

The PWM 1 Polarity Select bit selects the polarity for PWM 1.

1: Sets the polarity to active HIGH or rising edge pulse

0: Sets the polarity to active LOW

PWM 0 Polarity Select (Bit 4)

The PWM 0 Polarity Select bit selects the polarity for PWM 0.

1: Sets the polarity to active HIGH or rising edge pulse

0: Sets the polarity to active LOW

PWM 3 Enable (Bit 3)

The PWM 3 Enable bit enables or disables PWM 3.

1: Enable PWM 3

0: Disable PWM 3

PWM 2 Enable (Bit 2)

The PWM 2 Enable bit enables or disables PWM 2.

1: Enable PWM 2

0: Disable PWM 2

PWM 1 Enable (Bit 1)

The PWM 1 Enable bit enables or disables PWM 1.

1: Enable PWM 1

0: Disable PWM 1

PWM 0 Enable (Bit 0)

The PWM 0 Enable bit enables or disables PWM 0.

1: Enable PWM 0

0: Disable PWM 0

PWM Maximum Count Register [0xC0E8] [R/W]

Table 127. PWM Maximum Count Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved						Count...	
Read/Write	-	-	-	-	-	-	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Count							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The PWM Maximum Count register designates the maximum window for each pulse cycle. Each count tick is based on the clock frequency set in the PWM Control register.

Count (Bits [9:0])

The Count field sets the maximum cycle time.

Reserved

Write all reserved bits with ’0’.

Absolute Maximum Ratings

This section lists the absolute maximum ratings. Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can affect device operation and reliability.

Storage Temperature ..... –40°C to +125°C
Ambient Temperature with Power Supplied.. –40°C to +85°C
Supply Voltage to Ground Potential.....0.0V to +3.6V
DC Input Voltage to Any General Purpose Input Pin..... 5.5V
DC Voltage Applied to XTALIN ..... –0.5V to V_{CC} + 0.5V
Static Discharge Voltage..... > 2000V
Max Output Current, per IO ..... 4 mA

Operating Conditions

T_A (Ambient Temperature Under Bias) ..... –40°C to +85°C
Supply Voltage (V_{CC}, AV_{CC}) .....+3.0V to +3.6V
Supply Voltage ($BoostV_{CC}$)[16] .....+2.7V to +3.6V
Ground Voltage..... 0V
F_{OSC} (Oscillator or Crystal Frequency).... 12 MHz ± 500 ppm
..... Parallel Resonant

Crystal Requirements (XTALIN, XTALOUT)

Table 132. Crystal Requirements

Crystal Requirements (XTALIN, XTALOUT)	Min	Typical	Max	Unit
Parallel Resonant Frequency		12		MHz
Frequency Stability	–500		+500	PPM
Load Capacitance	20		33	pF
Driver Level			500	µW
Startup Time			5	ms
Mode of Vibration: Fundamental				

DC Characteristics

Table 133. DC Characteristics [17]

Parameter	Description	Conditions	Min	Typ.	Max	Unit
V_{CC}, AV_{CC}	Supply Voltage		3.0	3.3	3.6	V
$BoosV_{CC}$	Supply Voltage		2.7		3.6	V
V_{IH}	Input HIGH Voltage		2.0		5.5	V
V_{IL}	Input LOW Voltage				0.8	V
I_I	Input Leakage Current	$0< V_{IN} < V_{CC}$	–10.0		+10.0	µA
V_{OH}	Output Voltage HIGH	I_{OUT} = 4 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OUT} = –4 mA			0.4	V
I_{OH}	Output Current HIGH			10	20	mA
I_{OL}	Output Current LOW			10	20	mA
C_{IN}	Input Pin Capacitance	Except D+/D–			10	pF
		D+/D–			15	pF
V_{HYS}	Hysteresis on nReset Pin		250			mV
I_{CC}[18, 19]	Supply Current	4 transceivers powered		80	100	mA
I_{CCB}[18, 19]	Supply Current with Booster Enabled	4 transceivers powered		135	180	mA

Notes
16. The on-chip voltage booster circuit boosts $BoostV_{CC}$ to provide a nominal 3.3V V_{CC} supply.
17. All tests were conducted with Charge pump off.

SRAM Read Cycle[24]

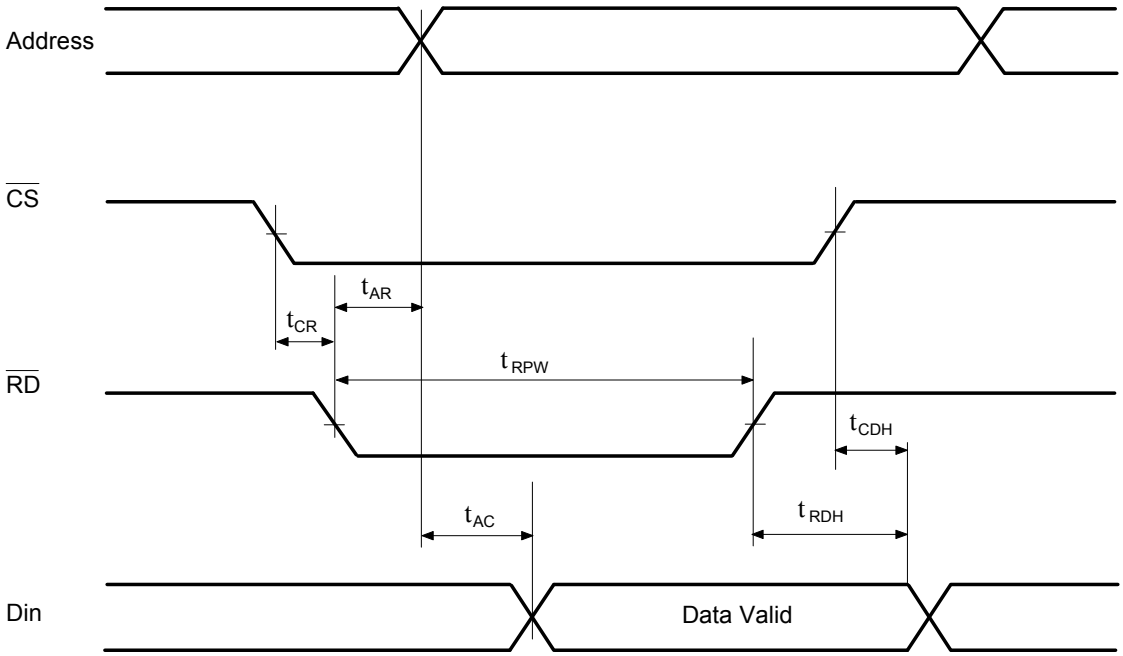


Table 137. SRAM Read Cycle Parameters

Parameter	Description	Min	Typical	Max	Unit
t_{CR}	$\overline{CS}$ LOW to $\overline{RD}$ LOW	1			ns
t_{RDH}	$\overline{RD}$ HIGH to Data Hold	0			ns
t_{CDH}	$\overline{CS}$ HIGH to Data Hold	0			ns
t_{RPW}[22]	$\overline{RD}$ LOW Time	38		45	ns
t_{AR}	$\overline{RD}$ LOW to Address Valid			0	ns
t_{AC}[23]	RAM Access to Data Valid			12	ns

Notes
22. 0 wait state cycle.
23. t_{AC} External SRAM access time = 12 ns for zero and one wait states. The External SRAM access time = 12 ns + (n – 1)*T for wait states = n, n > 1, T = 48 MHz clock period.
24. Read timing is applicable for nXMEMSEL, nXRAMSEL, and nXROMSEL.

HPI (Host Port Interface) Write Cycle Timing

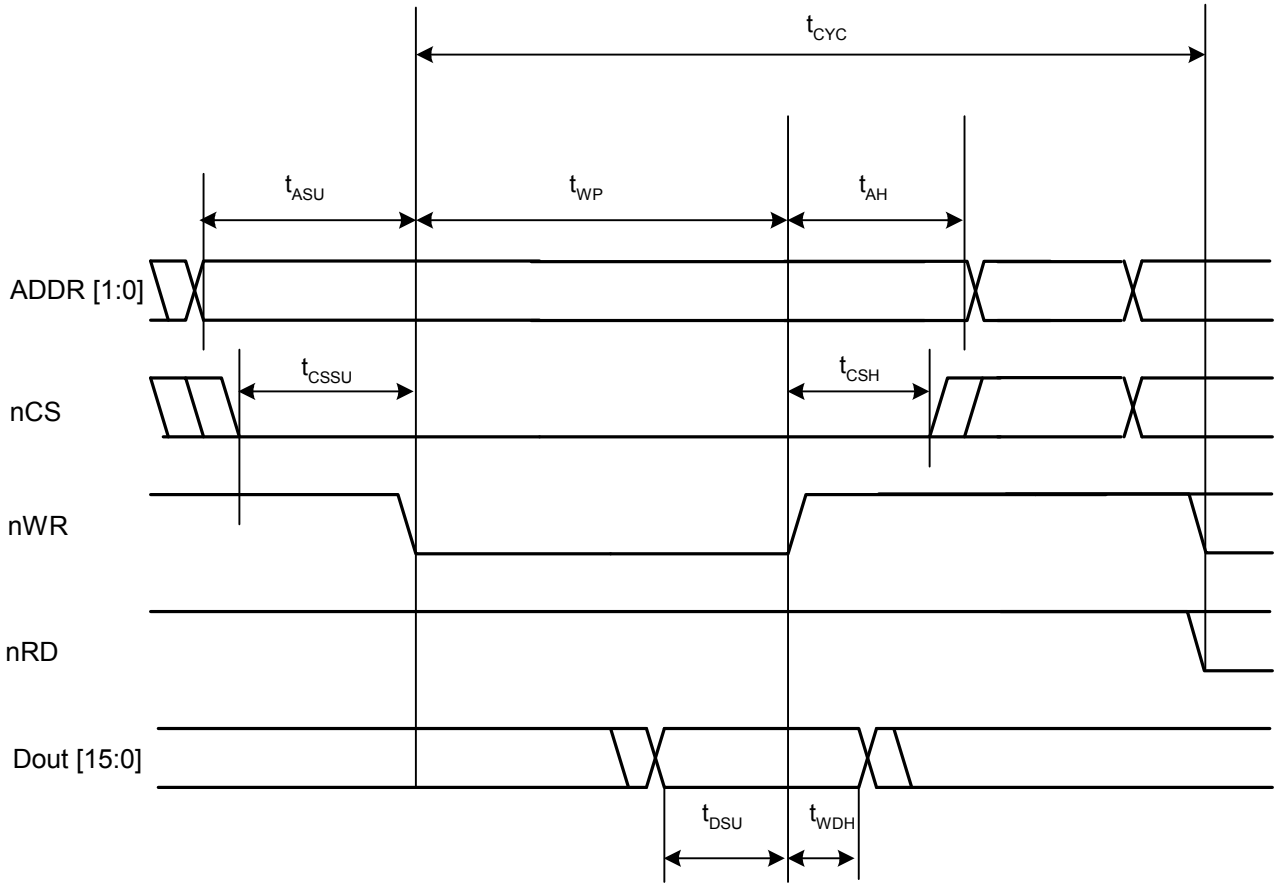


Table 140. HPI Write Cycle Timing Parameters

Parameter	Description	Min	Typical	Max	Unit
t_{ASU}	Address Setup	–1			ns
t_{AH}	Address Hold	–1			ns
t_{CSSU}	Chip Select Setup	–1			ns
t_{CSH}	Chip Select Hold	–1			ns
t_{DSU}	Data Setup	6			ns
t_{WDH}	Write Data Hold	2			ns
t_{WP}	Write Pulse Width	2			T[27]
t_{CYC}	Write Cycle Time	6			T[27]

Notes
27. T = system clock period = 1/48 MHz.

7. Coupled SIE Interrupt Enable Bits

■ **Problem Definition**

Host/Device 1 SIE events will still trigger an interrupt when only the Host/Device 2 SIE Interrupt Enable is set and vise versa.

■ **Parameters Affected**

Host/Device SIE Interrupts.

■ **Trigger Condition(S)**

Setting only 1 Host/Device SIE Interrupt Enable.

■ **Scope of Impact**

The Host/Device global Interrupt Enable bits cannot be used to disable each Host/Device SIE independently. These bits are found in the Interrupt Enable Register (0xC00E).

■ **Workaround**

If an SIE Interrupt is desired, both Host/Device 1 and Host/Device 2 Interrupt Enable bits should be set in the Global Interrupt Enable Register (0xC00E). To properly mask an SIE Interrupt to a single SIE, the lower level Host/Device Interrupt Enable Registers (0xC08C and 0xC0AC) must be used. For example, setting the Host/Device 2 IE Register to 0x0000 will prevent any Host/Device 2 events from generating a Host/Device Interrupt. To disable all SIE interrupts, both Host/Device Interrupt Enable bits in the Interrupt Enable Register should be cleared.

■ **Fix Status**

No silicon revision planned, use workaround.

8. Un-Initialized SIExmsg Registers

■ **Problem Definition**

The SIE1msg and SIE2msg Registers [0x0144 and 0x0148] are not initialized at power up.

■ **Parameters Affected**

HPI interrupts.

■ **Trigger Condition(S)**

Power up initialization.

■ **Scope of Impact**

If you are using the HPI interface in co-processor mode, random data will be written to the SIE1msg and SIE2msg Registers [0x0144 and 0x0148] at power up. This will cause two improper HPI interrupts (HPI_INTR) to occur, one for each of the two SIExmsg Registers.

■ **Workaround**

The external processor should clear the SIExmsg Registers [0x0144 and 0x0148] shortly after nRESET is de-asserted and prior to the expected processing of proper HPI interrupts (generally 10 ms after nRESET is de-asserted).

■ **Fix Status**

No silicon revision planned, use workaround.