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Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Host/Peripheral Controller
Core Processor	CY16
Program Memory Type	ROM (8kB)
Controller Series	CY7C673xx
RAM Size	16K x 8
Interface	SPI Serial, USB, HPI
Number of I/O	32
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c67300-100axit

Contents

Table 1. Interface Options for GPIO Pins

GPIO Pins	HPI	IDE	PWM	HSS	SPI	UART	I2C	OTG
GPIO31							SCL/SDA	
GPIO30							SCL/SDA	
GPIO29								OTGID
GPIO28						TX		
GPIO27						RX		
GPIO26			PWM3	CTS[1]				
GPIO25								
GPIO24	INT	IOREADY						
GPIO23	nRD	IOR						
GPIO22	nWR	IOW						
GPIO21	nCS							
GPIO20	A1	CS1						
GPIO19	A0	CS0						
GPIO18		A2	PWM2	RTS[1]				
GPIO17		A1	PWM1	RXD[1]				
GPIO16		A0	PWM0	TXD[1]				
GPIO15	D15	D15						
GPIO14	D14	D14						
GPIO13	D13	D13						
GPIO12	D12	D12						
GPIO11	D11	D11			MOSI[1]			
GPIO10	D10	D10			SCK[1]			
GPIO9	D9	D9			nSSI[1]			
GPIO8	D8	D8			MISO[1]			
GPIO7	D7	D7						
GPIO6	D6	D6						
GPIO5	D5	D5						
GPIO4	D4	D4						
GPIO3	D3	D3						
GPIO2	D2	D2						
GPIO1	D1	D1						
GPIO0	D0	D0						

Table 2. Interface Options for External Memory Bus Pins

MEM Pins	HPI	IDE	PWM	HSS	SPI	UART	I2C	OTG
D15				CTS[2]				
D14				RTS[2]				
D13				RXD[2]				
D12				TXD[2]				
D11					MOSI[2]			
D10					SCK[2]			
D9					nSSI[2]			
D8					MISO[2]			
D[7:0]								
A[18:0]								
CONTROL								

Notes
1. Default interface location.
2. Alternate interface location.

SPI Pins

The SPI port has a few different pin location options as shown in Table 9. The port location is selectable via the GPIO control register [0xC006].

Table 9. SPI Interface Pins

Pin Name	Pin Number
Default Location	
nSSI	56 or 65
SCK	61
MOSI	60
MISO	66
Alternate Location	
nSSI	73
SCK	72
MOSI	71
MISO	74

High-Speed Serial Interface

EZ-Host provides an HSS interface. The HSS interface is a programmable serial connection with baud rate from 9600 baud to 2.0M baud. The HSS interface supports both byte and block mode operations and also hardware and software handshaking. Complete control of EZ-Host can be accomplished through this interface via an extensible API and communication protocol. The HSS interface can be exposed through GPIO pins or the External Memory port.

HSS Features

- 8 bits, no parity code
- Programmable baud rate from 9600 baud to 2M baud
- Selectable 1- or 2-stop bit on transmit
- Programmable inter-character gap timing for Block Transmit
- 8-byte receive FIFO
- Glitch filter on receive
- Block mode transfer directly to/from EZ-Host internal memory (DMA transfer)
- Selectable CTS/RTS hardware signal handshake protocol
- Selectable XON/XOFF software handshake protocol
- Programmable Receive interrupt, Block Transfer Done interrupts
- Complete access to internal memory

HSS Pins

The HSS port has a few different pin location options as shown in Table 10. The port location is selectable via the GPIO control register [0xC006].

Table 10. HSS Interface Pins

Pin Name	Pin Number
Default Location	
CTS	44
RTS	53
RXD	54
TXD	55
Alternate Location	
CTS	67
RTS	68
RXD	69
TXD	70

Programmable Pulse/PWM Interface

EZ-Host has four built in PWM output channels. Each channel provides a programmable timing generator sequence that can be used to interface to various image sensors or other applications. The PWM interface is exposed through GPIO pins.

Programmable Pulse/PWM Features

- Four independent programmable waveform generators
- Programmable predefined frequencies ranging from 5.90 KHz to 48 MHz
- Configurable polarity
- Continuous and one-shot mode available

Programmable Pulse/PWM Pins.

Table 11. PWM Interface Pins

Pin Name	Pin Number
PWM3	44
PWM2	53
PWM1	54
PWM0	55

Host Port Interface

EZ-Host has an HPI interface. The HPI interface provides DMA access to the EZ-Host internal memory by an external host, plus a bidirectional mailbox register for supporting high level communication protocols. This port is designed to be the primary high-speed connection to a host processor. Complete control of EZ-Host can be accomplished through this interface via an extensible API and communication protocol. Other than the hardware communication protocols, a host processor has identical control over EZ-Host whether connecting to the HPI or HSS port. The HPI interface is exposed through GPIO pins.

HPI Features

- 16-bit data bus interface
- 16 MB/s throughput
- Auto-increment of address pointer for fast block mode transfers
- Direct memory access (DMA) to internal memory
- Bidirectional Mailbox register
- Byte swapping
- Complete access to internal memory
- Complete control of SIEs through HPI
- Dedicated HPI status register

HPI Pins

Table 12. HPI Interface Pins [5, 6]

Pin Name	Pin Number
INT	46
nRD	47
nWR	48
nCS	49
A1	50
A0	52
D15	56
D14	57
D13	58
D12	59
D11	60
D10	61
D9	65
D8	66
D7	86
D6	87
D5	89
D4	90
D3	91
D2	92
D1	93
D0	94

The two HPI address pins are used to address one of four possible HPI port registers as shown in Table 13.

Table 13. HPI Addressing

HPI A[1:0]	A1	A0
HPI Data	0	0
HPI Mailbox	0	1
HPI Address	1	0
HPI Status	1	1

IDE Interface

EZ-Host has an IDE interface. The IDE interface supports PIO mode 0-4 as specified in the Information Technology-AT Attachment–4 with Packet Interface Extension (ATA/ATAPI-4) Specification, T13/1153D Rev 18. There is no need for firmware to use programmable wait states. The CPU read/write cycle is automatically extended as needed for direct CPU to IDE read/write accesses.

The EZ-Host IDE interface also has a BLOCK transfer mode that allows EZ-Host to read/write large blocks of data to/from the IDE data register and move it to/from the EZ-Host on-chip memory directly without intervention of the CPU. The IDE interface is exposed through GPIO pins. Table 14 on page 12 lists the achieved throughput for maximum block mode data transfer rate (with IDE_IORDY true) for the various IDE PIO modes.

Notes
5. HPI_INT is for the Outgoing Mailbox interrupt.
6. HPI strobes are negative logic sampled on rising edge.

External (Remote) Wakeup Source

There are several possible events available to wake EZ-Host from Sleep mode as shown in Table 20. These may also be used as remote wakeup options for USB applications. See the Power Control Register [0xC00A] [R/W] on page 21 for details.

Upon wakeup, code begins executing within 200 µs, the time it takes the PLL to stabilize.

Table 20. Wakeup Sources [7, 8]

Wakeup Source (if enabled)	Event
USB Resume	D+/D– Signaling
OTGVBUS	Level
OTGID	Any Edge
HPI	Read
HSS	Read
SPI	Read
IRQ1 (GPIO 25)	Any Edge
IRQ0 (GPIO 24)	Any Edge

Power-On-Reset Description

The length of the power-on-reset event can be defined by (V_{CC} ramp to valid) + (Crystal startup). A typical application might use a 12 ms power-on-reset event = ~7 ms + ~5 ms, respectively.

Reset Pin

The Reset pin is active low and requires a minimum pulse duration of sixteen 12 MHz clock cycles (1.3 µs). A reset event restores all registers to their default POR settings. Code execution then begins 200 µs later at 0xFF00 with an immediate jump to 0xE000, the start of BIOS. Refer to BIOS documentation for additional details.

USB Reset

A USB Reset affects registers 0xC090 and 0xC0B0, all other registers remain unchanged.

Memory Map

The memory map is discussed in the following sections.

Mapping

The total memory space directly addressable by the CY16 processor is 64K (0x0000-0xFFFF). Program, data, and IO are contained within this 64K space. This memory space is byte addressable. Figure 10 on page 17 shows the various memory region address locations.

Internal Memory

Of the internal memory, 15K bytes are allocated for user's program and data. The lower memory space from 0x0000 to 0x04A2 is reserved for interrupt vectors, general purpose registers, USB control registers, stack, and other BIOS variables. The upper internal memory space contains EZ-Host control registers from 0xC000 to 0xC0FF and the BIOS ROM itself from 0xE000 to 0xFFFF. For more information about the reserved lower memory or the BIOS ROM, refer to the Programmer's documentation and/or the BIOS documentation.

During development with the EZ-Host toolset, leave the lower area of user's space (0x04A4 to 0x1000) available to load the GDB stub. The GDB stub is required to allow the toolset debug access into EZ-Host.

The chip select pins are not active during accesses to internal memory.

External Memory

Up to 32 KB of external memory from 0x4000 - 0xBFFF is available via one chip select line (nXRAMSEL) with RAM Merge enabled (BIOS default). Additionally, another 8 KB region from 0xC100 - 0xDFFF is available via a second chip select line (nXROMSEL) giving 40 KB of total available external memory. Together with the internal 15 KB, this gives a total of either ~48 KB (one chip select) or ~56 KB (two chip selects) of available memory for either code or data.

Note that the memory map and pin names (nXRAMSEL/ nXROMSEL) define specific memory regions for RAM vs. ROM. This allows the BIOS to look in the upper external memory space at 0xC100 for SCAN vectors (enabling code to be loaded/ executed from ROM). If no SCAN vectors are required in the design (external memory is used exclusively for data), then all external memory regions can be used for RAM. Similarly, the external memory can be used exclusively for code space (ROM).

If more external memory is required, EZ-Host has enough address lines to support up to 512 KB. However, this requires complex code banking/paging schemes via the Extended Page registers.

For further information about setting up the external memory, see the External Memory Interface on page 6.

Notes
7. Read data is discarded (dummy data).
8. HPI_INT asserts on a USB Resume.

Bank Register [0xC002] [R/W]

Table 23. Bank Register

Bit #	15	14	13	12	11	10	9	8
Field	Address...							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	...Address			Reserved				
Read/Write	R/W	R/W	R/W	-	-	-	-	-
Default	0	0	0	X	X	X	X	X

Register Description

The Bank register maps registers R0–R15 into RAM. The eleven MSBs of this register are used as a base address for registers R0–R15. A register address is automatically generated by:

1. Shifting the four LSBs of the register address left by 1.
2. ORing the four shifted bits of the register address with the twelve MSBs of the Bank register.
3. Forcing the LSB to zero.

For example, if the Bank register is left at its default value of 0x0100, and R2 is read, then the physical address 0x0102 is read. Refer to Table 24 for details.

Table 24. Bank Register Example

Register	Hex Value	Binary Value
Bank	0x0100	0000 0001 0000 0000
R14	0x000E << 1 = 0x001C	0000 0000 0001 1100
RAM Location	0x011C	0000 0001 0001 1100

Address (Bits [15:4])

The Address field is used as a base address for all register addresses to start from.

Reserved

Write all reserved bits with ’0’.

Hardware Revision Register [0xC004] [R]

Table 25. Revision Register

Bit #	15	14	13	12	11	10	9	8
Field	Revision...							
Read/Write	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	...Revision							
Read/Write	R	R	R	R	R	R	R	R
Default	X	X	X	X	X	X	X	X

Register Description

The Hardware Revision register is a read only register that indicates the silicon revision number. The first silicon revision is represented by 0x0101. This number is increased by one for each new silicon revision.

Revision (Bits [15:0])

The Revision field contains the silicon revision number.

CPU Speed Register [0xC008] [R/W]

Table 26. CPU Speed Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved...							
Read/Write	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Reserved				CPU Speed			
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

Register Description

The CPU Speed register allows the processor to operate at a user selected speed. This register only affects the CPU, all other peripheral timing is still based on the 48 MHz system clock (unless otherwise noted).

CPU Speed (Bits[3:0])

The CPU Speed field is a divisor that selects the operating speed of the processor as defined in Table 27.

Table 27. CPU Speed Definition

CPU Speed [3:0]	Processor Speed
0000	48 MHz/1
0001	48 MHz/2
0010	48 MHz/3
0011	48 MHz/4
0100	48 MHz/5
0101	48 MHz/6
0110	48 MHz/7
0111	48 MHz/8
1000	48 MHz/9
1001	48 MHz/10
1010	48 MHz/11
1011	48 MHz/12
1100	48 MHz/13
1101	48 MHz/14
1110	48 MHz/15
1111	48 MHz/16

Reserved

Write all reserved bits with ’0’.

HSS Interrupt Enable (Bit 7)

The HSS Interrupt Enable bit enables or disables the following High-speed Serial Interface hardware interrupts: HSS Block Done and HSS RX Full.

1: Enable HSS interrupt

0: Disable HSS interrupt

In Mailbox Interrupt Enable (Bit 6)

The In Mailbox Interrupt Enable bit enables or disables the HPI: Incoming Mailbox hardware interrupt.

1: Enable MBXI interrupt

0: Disable MBXI interrupt

Out Mailbox Interrupt Enable (Bit 5)

The Out Mailbox Interrupt Enable bit enables or disables the HPI: Outgoing Mailbox hardware interrupt.

1: Enable MBXO interrupt

0: Disable MBXO interrupt

UART Interrupt Enable (Bit 3)

The UART Interrupt Enable bit enables or disables the following UART hardware interrupts: UART TX, and UART RX.

1: Enable UART interrupt

0: Disable UART interrupt

GPIO Interrupt Enable (Bit 2)

The GPIO Interrupt Enable bit enables or disables the General Purpose IO pins interrupt (see the GPIO Control Register [0xC006] [R/W] on page 56). When the GPIO bit is reset, all pending GPIO interrupts are also cleared

1: Enable GPIO interrupt

0: Disable GPIO interrupt

Timer 1 Interrupt Enable (Bit 1)

The Timer 1 Interrupt Enable bit enables or disables the TImer1 Interrupt Enable. When this bit is reset, all pending Timer 1 interrupts are cleared.

1: Enable TM1 interrupt

0: Disable TM1 interrupt

Timer 0 Interrupt Enable (Bit 0)

The Timer 0 Interrupt Enable bit enables or disables the TImer0 Interrupt Enable. When this bit is reset, all pending Timer 0 interrupts are cleared.

1: Enable TM0 interrupt

0: Disable TM0 interrupt

Reserved

Write all reserved bits with ’0’.

Breakpoint Register [0xC014] [R/W]

Table 30. Breakpoint Register

Bit #	15	14	13	12	11	10	9	8
Field	Address...							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Address							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The Breakpoint register holds the breakpoint address. When the program counter matches this address, the INT127 interrupt occurs. To clear this interrupt, write a zero value to this register.

Address (Bits [15:0])

The Address field is a 16-bit field containing the breakpoint address.

underflow and the Overflow and Underflow flags (bits 11 and 10 respectively) must be checked to determine which event occurred.

1: An overflow or underflow condition occurred

0: An overflow or underflow condition did not occur

Setup Flag (Bit 4)

The Setup Flag bit indicates that a setup packet was received. In device mode setup packets are stored at memory location 0x0300 for Device 1 and 0x0308 for Device 2. Setup packets are always accepted regardless of the Direction Select and Arm Enable bit settings as long as the Device n EP n Control register Enable bit is set.

1: Setup packet was received

0: Setup packet was not received

Sequence Flag (Bit 3)

The Sequence Flag bit indicates whether the last data toggle received was a DATA1 or a DATA0. This bit has no effect on receiving data packets; sequence checking must be handled in firmware.

1: DATA1 was received

0: DATA0 was received

Timeout Flag (Bit 2)

The Timeout Flag bit indicates whether a timeout condition occurred on the last transaction. On the device side, a timeout can occur if the device sends a data packet in response to an IN request but then does not receive a handshake packet in a predetermined time. It can also occur if the device does not receive the data stage of an OUT transfer in time.

1: Timeout occurred

0: Timeout condition did not occur

Error Flag (Bit 2)

The Error Flag bit is set if a CRC5 and CRC16 error occurs, or if an incorrect packet type is received. Overflow and underflow are not considered errors and do not affect this bit.

1: Error occurred

0: Error did not occur

ACK Flag (Bit 0)

The ACK Flag bit indicates whether the last transaction was ACKed.

1: ACK occurred

0: ACK did not occur

Device n Endpoint n Count Result Register [R/W]

- Device n Endpoint 0 Count Result Register [Device 1: 0x0208 Device 2: 0x0288]
- Device n Endpoint 1 Count Result Register [Device 1: 0x0218 Device 2: 0x0298]
- Device n Endpoint 2 Count Result Register [Device 1: 0x0228 Device 2: 0x02A8]
- Device n Endpoint 3 Count Result Register [Device 1: 0x0238 Device 2: 0x02B8]
- Device n Endpoint 4 Count Result Register [Device 1: 0x0248 Device 2: 0x02C8]
- Device n Endpoint 5 Count Result Register [Device 1: 0x0258 Device 2: 0x02D8]
- Device n Endpoint 6 Count Result Register [Device 1: 0x0268 Device 2: 0x02E8]
- Device n Endpoint 7 Count Result Register [Device 1: 0x0278 Device 2: 0x02F8]

Table 67. Device n Endpoint n Count Result Register

Bit #	15	14	13	12	11	10	9	8
Field	Result...							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

Bit #	7	6	5	4	3	2	1	0
Field	...Result							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	X	X	X	X	X	X	X	X

Register Description

The Device n Endpoint n Count Result register contains the size difference in bytes between the Endpoint Count specified in the Device n Endpoint n Count register and the last packet received. If an overflow or underflow condition occurs, that is, the received packet length differs from the value specified in the Device n Endpoint n Count register, the Length Exception Flag bit in the Device n Endpoint n Status register is set. The value in this register is only valued when the Length Exception Flag bit is set and the Error Flag bit is not set; both bits are in the Device n Endpoint n Status register.

EP6 Interrupt Flag (Bit 6)

The EP6 Interrupt Flag bit indicates if the endpoint six (EP6) Transaction Done interrupt triggered. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied EP: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, if the NAK Interrupt Enable bit in the Device n Endpoint Control register is set, this interrupt also triggers when the device NAKs host requests.

1: Interrupt triggered

0: Interrupt did not trigger

EP5 Interrupt Flag (Bit 5)

The EP5 Interrupt Flag bit indicates if the endpoint five (EP5) Transaction Done interrupt triggered. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied EP: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, if the NAK Interrupt Enable bit in the Device n Endpoint Control register is set, this interrupt also triggers when the device NAKs host requests.

1: Interrupt triggered

0: Interrupt did not trigger

EP4 Interrupt Flag (Bit 4)

The EP4 Interrupt Flag bit indicates if the endpoint four (EP4) Transaction Done interrupt triggered. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied EP: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, if the NAK Interrupt Enable bit in the Device n Endpoint Control register is set, this interrupt also triggers when the device NAKs host requests.

1: Interrupt triggered

0: Interrupt did not trigger

EP3 Interrupt Flag (Bit 3)

The EP3 Interrupt Flag bit indicates if the endpoint three (EP3) Transaction Done interrupt triggered. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied EP: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, if the NAK Interrupt Enable bit in the Device n Endpoint Control register is set, this interrupt also triggers when the device NAKs host requests.

1: Interrupt triggered

0: Interrupt did not trigger

EP2 Interrupt Flag (Bit 2)

The EP2 Interrupt Flag bit indicates if the endpoint two (EP2) Transaction Done interrupt triggered. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied EP: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, if the NAK Interrupt Enable bit in the Device n Endpoint Control register is set, this interrupt also triggers when the device NAKs host requests.

1: Interrupt triggered

0: Interrupt did not trigger

EP1 Interrupt Flag (Bit 1)

The EP1 Interrupt Flag bit indicates if the endpoint one (EP1) Transaction Done interrupt triggered. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied EP: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, if the NAK Interrupt Enable bit in the Device n Endpoint Control register is set, this interrupt also triggers when the device NAKs host requests.

1: Interrupt triggered

0: Interrupt did not trigger

EP0 Interrupt Flag (Bit 0)

The EP0 Interrupt Flag bit indicates if the endpoint zero (EP0) Transaction Done interrupt triggered. An EPx Transaction Done interrupt triggers when any of the following responses or events occur in a transaction for the device's supplied EP: send/receive ACK, send STALL, Timeout occurs, IN Exception Error, or OUT Exception Error. In addition, if the NAK Interrupt Enable bit in the Device n Endpoint Control register is set, this interrupt also triggers when the device NAKs host requests.

1: Interrupt triggered

0: Interrupt did not trigger

Reserved

Write all reserved bits with '0'.

SPI Transmit Count Register [0xC0DA] [R/W]

Table 116. SPI Transmit Count Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved					Count...		
Read/Write	-	-	-	-	-	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Count							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The SPI Transmit Count register designates the block byte length for the SPI transmit DMA transfer.

Reserved

Write all reserved bits with ’0’.

Count (Bits [10:0])

The Count field sets the count for the SPI transmit DMA transfer.

SPI Receive Address Register [0xC0DC [R/W]

Table 117. SPI Receive Address Register

Bit #	15	14	13	12	11	10	9	8
Field	Address...							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Address							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The SPI Receive Address register is issued as the base address for the SPI Receive DMA.

Address (Bits [15:0])

The Address field sets the base address for the SPI receive DMA.

SPI Receive Count Register [0xC0DE] [R/W]

Table 118. SPI Receive Count Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved					Count...		
Read/Write	-	-	-	-	-	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Count							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

PWM n Start Register [R/W]

- PWM 0 Start Register 0xC0EA
- PWM 1 Start Register 0xC0EE
- PWM 2 Start Register 0xC0F2
- PWM 3 Start Register 0xC0F6

Table 128. PWM n Start Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved						Address...	
Read/Write	-	-	-	-	-	-	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Address							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The PWM n Start register designates where in the window defined by the PWM Maximum Count register to start the PWM pulse for a supplied channel.

Address (Bits [9:0])

The Address field designates when to start the PWM pulse. If this start value is equal to the Stop Count Value then the output stays at false.

Reserved

Write all reserved bits with ’0’.

PWM n Stop Register [R/W]

- PWM 0 Stop Register 0xC0EC
- PWM 1 Stop Register 0xC0F0
- PWM 2 Stop Register 0xC0F4
- PWM 3 Stop Register 0xC0F8

Table 129. PWM n Stop Register

Bit #	15	14	13	12	11	10	9	8
Field	Reserved						Address...	
Read/Write	-	-	-	-	-	-	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Field	...Address							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Description

The PWM n Stop register designates where in the window defined by the PWM Maximum Count register to stop the PWM pulse for a supplied channel.

Address (Bits [9:0])

The Address field designates when to stop the PWM pulse. If the PWM Start value is equal to the PWM Stop value then the output stays at ‘0’. If the PWM Stop value is greater then the PWM Maximum Count value then the output stays at true.

Reserved

Write all reserved bits with ’0’.

Absolute Maximum Ratings

This section lists the absolute maximum ratings. Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can affect device operation and reliability.

Storage Temperature ..... –40°C to +125°C
Ambient Temperature with Power Supplied.. –40°C to +85°C
Supply Voltage to Ground Potential.....0.0V to +3.6V
DC Input Voltage to Any General Purpose Input Pin..... 5.5V
DC Voltage Applied to XTALIN ..... –0.5V to V_{CC} + 0.5V
Static Discharge Voltage..... > 2000V
Max Output Current, per IO ..... 4 mA

Operating Conditions

T_A (Ambient Temperature Under Bias) ..... –40°C to +85°C
Supply Voltage (V_{CC}, AV_{CC}) .....+3.0V to +3.6V
Supply Voltage ($BoostV_{CC}$)[16] .....+2.7V to +3.6V
Ground Voltage..... 0V
F_{OSC} (Oscillator or Crystal Frequency).... 12 MHz ± 500 ppm
..... Parallel Resonant

Crystal Requirements (XTALIN, XTALOUT)

Table 132. Crystal Requirements

Crystal Requirements (XTALIN, XTALOUT)	Min	Typical	Max	Unit
Parallel Resonant Frequency		12		MHz
Frequency Stability	–500		+500	PPM
Load Capacitance	20		33	pF
Driver Level			500	µW
Startup Time			5	ms
Mode of Vibration: Fundamental				

DC Characteristics

Table 133. DC Characteristics [17]

Parameter	Description	Conditions	Min	Typ.	Max	Unit
V_{CC}, AV_{CC}	Supply Voltage		3.0	3.3	3.6	V
$BoosV_{CC}$	Supply Voltage		2.7		3.6	V
V_{IH}	Input HIGH Voltage		2.0		5.5	V
V_{IL}	Input LOW Voltage				0.8	V
I_I	Input Leakage Current	$0< V_{IN} < V_{CC}$	–10.0		+10.0	µA
V_{OH}	Output Voltage HIGH	I_{OUT} = 4 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OUT} = –4 mA			0.4	V
I_{OH}	Output Current HIGH			10	20	mA
I_{OL}	Output Current LOW			10	20	mA
C_{IN}	Input Pin Capacitance	Except D+/D–			10	pF
		D+/D–			15	pF
V_{HYS}	Hysteresis on nReset Pin		250			mV
I_{CC}[18, 19]	Supply Current	4 transceivers powered		80	100	mA
I_{CCB}[18, 19]	Supply Current with Booster Enabled	4 transceivers powered		135	180	mA

Notes
16. The on-chip voltage booster circuit boosts $BoostV_{CC}$ to provide a nominal 3.3V V_{CC} supply.
17. All tests were conducted with Charge pump off.

Table 133. DC Characteristics (Continued)[17]

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{SLEEP}	Sleep Current	USB Peripheral: includes 1.5K internal pull up		210	500	µA
		Without 1.5K internal pull up		5	30	µA
I_{SLEEPB}	Sleep Current with Booster Enabled	USB Peripheral: includes 1.5K internal pull up		190	500	µA
		Without 1.5K internal pull up		5	30	µA

Table 134. DC Characteristics: Charge Pump

Parameter	Description	Conditions	Min	Typ.	Max	Unit
$V_{A\_VBUS\_OUT}$	Regulated OTGVBUS Voltage	8 mA< I_{LOAD} < 10 mA	4.4		5.25	V
$T_{A\_VBUS\_RISE}$	V_{BUS} Rise Time	I_{LOAD} = 10 mA			100	ms
$I_{A\_VBUS\_OUT}$	Maximum Load Current		8		10	mA
C_{DRD_VBUS}	OUTVBUS Bypass Capacitance	4.4V< V_{BUS} < 5.25V	1.0		6.5	pF
$V_{A\_VBUS\_LKG}$	OTGVBUS Leakage Voltage	OTGVBUS not driven			200	mV
$V_{DRD\_DATA\_LKG}$	Dataline Leakage Voltage				342	mV
I_{CHARGE}	Charge Pump Current Draw	I_{LOAD} = 8 mA		20	20	mA
		I_{LOAD} = 0 mA		0	1	mA
$I_{CHARGEB}$	Charge Pump Current Draw with Booster Active	I_{LOAD} = 8 mA		30	45	mA
		I_{LOAD} = 0 mA		0	5	mA
$I_{B\_DSCHG\_IN}$	B-Device (SRP Capable) Discharge Current	0V< V_{BUS} < 5.25V			8	mA
$V_{A\_VBUS\_VALID}$	A-Device VBUS Valid		4.4			V
$V_{A\_SESS\_VALID}$	A-Device Session Valid		0.8		2.0	V
$V_{B\_SESS\_VALID}$	B-Device Session Valid		0.8		4.0	V
$V_{A\_SESS\_END}$	B-Device Session End		0.2		0.8	V
E	Efficiency When Loaded	I_{LOAD} = 8 mA, V_{CC} = 3.3V		75		%
R_{PD}	Data Line Pull Down		14.25		24.8	Ω
$R_{A\_BUS\_IN}$	A-device V_{BUS} Input Impedance to GND	V_{BUS} is not being driven	40		100	kΩ
$R_{B\_SRP\_UP}$	B-device V_{BUS} SRP Pull Up	Pull up voltage = 3.0V	281			Ω
$R_{B\_SRP\_DWN}$	B-device V_{BUS} SRP Pull Down		656			Ω

USB Transceiver

USB 2.0 certified in full- and low-speed modes.

Notes
18. I_{CC} and I_{CCB} values are the same regardless of USB host or peripheral configuration.
19. There is no appreciable difference in I_{CC} and I_{CCB} values when only two transceivers are powered.

SRAM Write Cycle [26]

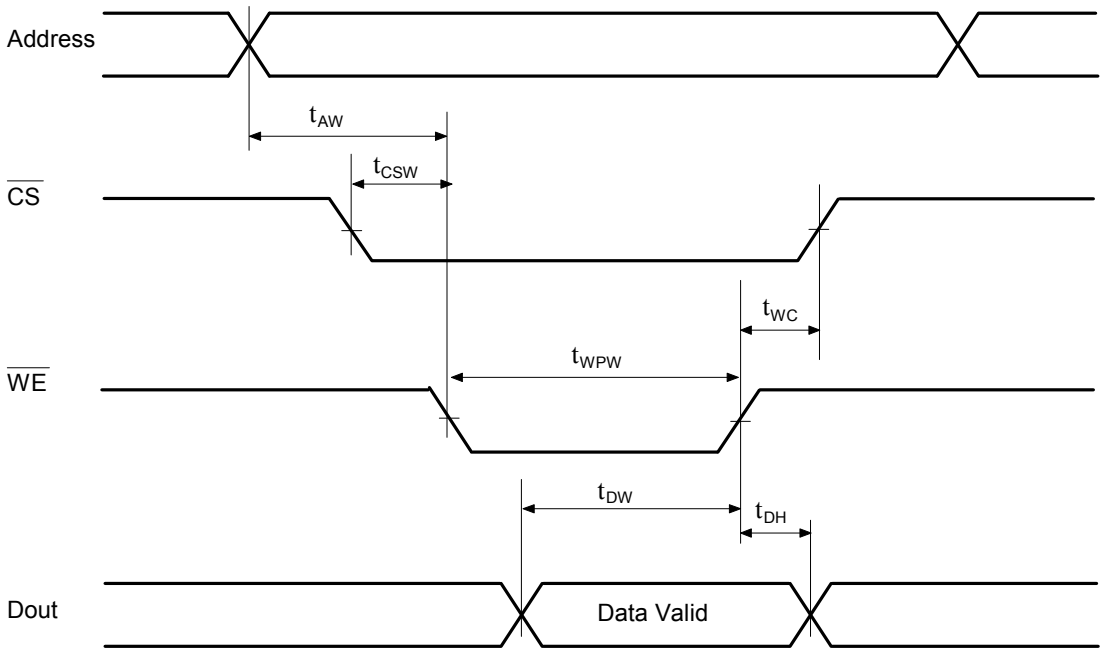


Table 138. SRAM Write Cycle Parameters

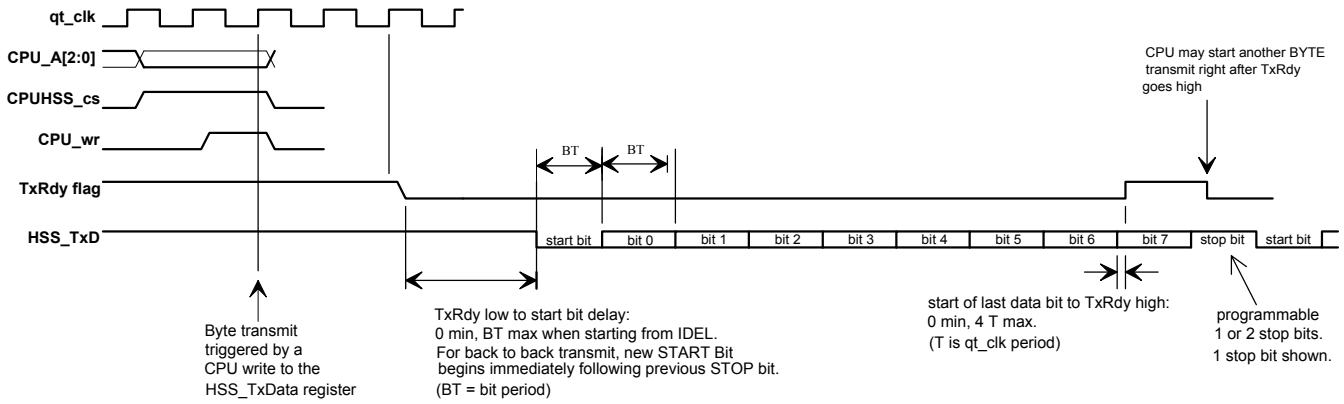
Parameter	Description	Min	Typical	Max	Unit
t_{AW}	Write Address Valid to $\overline{WE}$ LOW	7			ns
t_{CSW}	$\overline{CS}$ LOW to $\overline{WE}$ LOW	7			ns
t_{DW}	Data Valid to $\overline{WE}$ HIGH	15			ns
t_{WPW}[25]	$\overline{WE}$ Pulse Width	15			ns
t_{DH}	Data Hold from $\overline{WE}$ HIGH	4.5			ns
t_{WC}	$\overline{WE}$ HIGH to $\overline{CS}$ HIGH	13			ns

Notes
25. t_{WPW} The write pulse width = 18.8 ns min. for zero and one wait states. The write pulse = 18.8 ns + (n – 1)*T for wait states = n, n > 1, T = 48 MHz clock period.
26. Write timing is applicable for nXMEMSEL, nXRAMSEL and nXROMSEL.

IDE Timing

The IDE interface supports PIO mode 0-4 as specified in the Information Technology-AT Attachment–4 with Packet Interface Extension (ATA/ATAPI-4) Specification, T13/1153D Rev 18.

HSS BYTE Mode Transmit

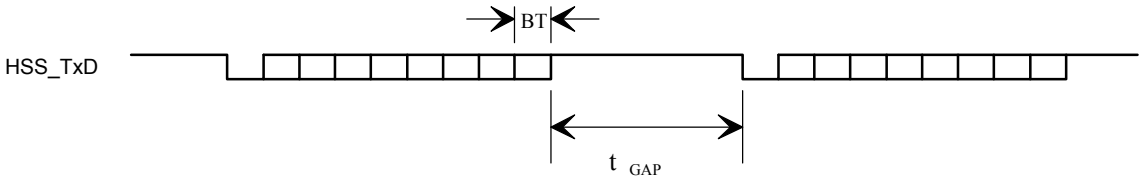


qt_clk, CPU_A, CPUHSS_cs, CPU_wr are internal signals, included in the diagram to illustrate the relationship between CPU operations and HSS port operations.

Bit 0 is LSB of data byte. Data bits are HIGH true: HSS_TxD HIGH = data bit value ‘1’.

BT = bit time = 1/baud rate.

HSS Block Mode Transmit



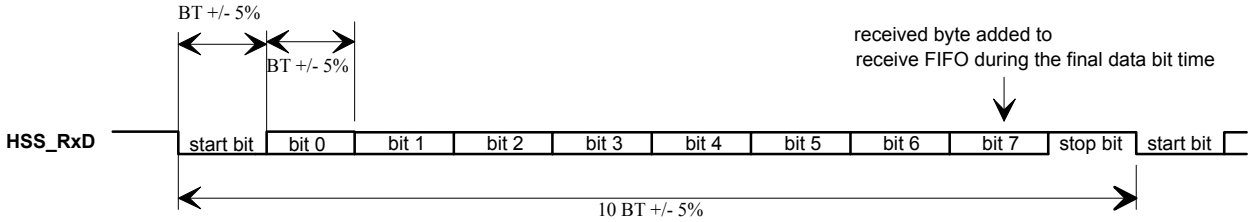
BLOCK mode transmit timing is similar to BYTE mode, except the STOP bit time is controlled by the HSS_GAP value.

The BLOCK mode STOP bit time, t_{GAP} = (HSS_GAP – 9) BT, where BT is the bit time, and HSS_GAP is the content of the HSS Transmit Gap register [0xC074].

The default t_{GAP} is 2 BT.

BT = bit time = 1/baud rate.

HSS BYTE and BLOCK Mode Receive



Receive data arrives asynchronously relative to the internal clock. Incoming data bit rate may deviate from the programmed baud rate clock by as much as ±5% (with HSS_RATE value of 23 or higher).

BYTE mode received bytes are buffered in a FIFO. The FIFO not empty condition becomes the RxRdy flag.

BLOCK mode received bytes are written directly to the memory system.

Bit 0 is LSB of data byte. Data bits are HIGH true: HSS_RxD HIGH = data bit value ‘1’.

BT = bit time = 1/baud rate.

Table 142. Register Summary (Continued)

R/W	Address	Register	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Default High
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Low
R/W	0xC07E	HSS Transmit Counter	Reserved						Counter...		0000 0000
			...Counter								0000 0000
R/W	0xC080 0xC0A0	Host n Control	Reserved								0000 0000
			Preamble Enable	Sequence Select	Sync Enable	ISO Enable	Reserved			Arm Enable	0000 0000
R/W	0xC082 0xC0A2	Host n Address	Address...								0000 0000
			...Address								0000 0000
R/W	0xC084 0xC0A4	Host n Count	Reserved	Port Select	Reserved				Count...		0000 0000
			...Count								0000 0000
R/W	0xC084 0xC0A4	Device n Port Select	Reserved	Port Select	Reserved...						0000 0000
			...Reserved								0000 0000
R	0xC086 0xC0A6	Host n PID	Reserved				Overflow Flag	Underflow Flag	Reserved		0000 0000
			Stall Flag	NAK Flag	Length Exception Flag	Reserved	Sequence Status	Timeout Flag	Error Flag	ACK Flag	0000 0000
W	0xC086 0xC0A4	Host n EP Status	Reserved								0000 0000
			PID Select				Endpoint Select				0000 0000
R	0xC088 0xC0A8	Host n Count Result	Result...								0000 0000
			...Result								0000 0000
W	0xC088 0xC0A8	Host n Device Address	Reserved...								0000 0000
			...Reserved	Address							0000 0000
R/W	0xC08A 0xC0AA	USB n Control	Port B D+ Status	Port B D– Status	Port A D+ Status	Port A D– Status	LOB	LOA	Mode Select	Port B Resistors Enable	xxxx 0000
			Port A Resistors Enable	Port B Force D+/- State		Port A Force D± State		Suspend Enable	Port B SOF/EOP Enable	Port A SOF/EOP Enable	0000 0000
R/W	0xC08C	Host 1 Interrupt Enable	VBUS Interrupt Enable	ID Interrupt Enable	Reserved				SOF/EOP Interrupt Enable	Reserved	0000 0000
			Port B Wake Interrupt Enable	Port A Wake Interrupt Enable	Port B Connect Change Interrupt Enable	Port A Connect Change Interrupt Enable	Reserved			Done Interrupt Enable	0000 0000
R/W	0xC08C	Device 1 Interrupt Enable	VBUS Interrupt Enable	ID Interrupt Enable	Reserved		SOF/EOP Timeout Interrupt Enable	Reserved	SOF/EOP Interrupt Enable	Reset Interrupt Enable	0000 0000
			EP7 Interrupt Enable	EP6 Interrupt Enable	EP5 Interrupt Enable	EP4 Interrupt Enable	EP3 Interrupt Enable	EP2 Interrupt Enable	EP1 Interrupt Enable	EP0 Interrupt Enable	0000 0000
R/W	0xC08E 0xC0AE	Device n Address	Reserved...								0000 0000
			...Reserved	Address							0000 0000
R/W	0xC090	Host 1 Status	VBUS Interrupt Flag	ID Interrupt Flag	Reserved				SOF/EOP Interrupt Flag	Reserved	xxxx xxxx
			Port B Wake Interrupt Flag	Port A Wake Interrupt Flag	Port B Connect Change Interrupt Flag	Port A Connect Change Interrupt Flag	Port B SE0 Status	Port A SE0 Status	Reserved	Done Interrupt Flag	xxxx xxxx
R/W	0xC090	Device 1 Status	VBUS Interrupt Flag	ID Interrupt Flag	Reserved				SOF/EOP Interrupt Flag	Reset Interrupt Flag	xxxx xxxx
			EP7 Interrupt Flag	EP6 Interrupt Flag	EP5 Interrupt Flag	EP4 Interrupt Flag	EP3 Interrupt Flag	EP2 Interrupt Flag	EP1 Interrupt Flag	EP0 Interrupt Flag	xxxx xxxx
R/W	0xC092 0xC0B2	Host n SOF/EOP Count	Reserved		Count...						0010 1110
			...Count								1110 0000
R	0xC092 0xC0B2	Device n Frame Number	SOF/EOP Timeout Flag	SOF/EOP Timeout Interrupt Count			Reserved	Frame...			0000 0000
			...Frame								0000 0000
R	0xC094 0xC0B4	Host n SOF/EOP Counter	Reserved		Counter...						xxxx xxxx
			...Counter								xxxx xxxx
W	0xC094 0xC0B4	Device n SOF/EOP Count	Reserved		Count...						0010 1110
			...Count								1110 0000
R	0xC096 0xC0B6	Host n Frame	Reserved					Frame...			0000 0000
			...Frame								0000 0000
R/W	0xC0AC	Host 2 Interrupt Enable	Reserved						SOF/EOP Interrupt Enable	Reserved	0000 0000
			Port B Wake Interrupt Enable	Port A Wake Interrupt Enable	Port B Connect Change Interrupt Enable	Port A Connect Change Interrupt Enable	Reserved			Done Interrupt Enable	0000 0000

Errata

This document describes the errata for the EZ-Host™ Programmable Embedded USB Host/Peripheral Controller, CY7C67300 Product Family. Details include errata trigger conditions, available workaround, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY7C67300	All Packages

CY7C67300 Qualification Status

Product status: In Production

CY7C67300 Errata Summary

The following table defines the errata applicability to available CY7C67300 family devices. An 'X' indicates that the errata pertains to the selected device.

Note Click on the errata table items to view their descriptions.

Items	CY7C67300	Silicon Revision	Fix Status
1. HPI write to SIE registers	X	A	No silicon revision planned, use workaround.
2. Hub and low-speed device attached to a root hub of the EZ-Host chip	X	A	No silicon revision planned, use workaround.
3. IDE register read when GPIO24 pin is low	X	A	No silicon revision planned, use workaround.
4. UART Does Not Recognize Framing Errors	X	A	No silicon revision planned, use workaround.
5. UART does not override GPIO Control Register	X	A	No silicon revision planned, use workaround.
6. VBUS Interrupt (VBUS Valid) Requires Debouncing	X	A	No silicon revision planned, use workaround.
7. Coupled SIE Interrupt Enable Bits	X	A	No silicon revision planned, use workaround.
8. Un-Initialized SIExmsg Registers	X	A	No silicon revision planned, use workaround.
9. BIOS USB Peripheral Mode: Descriptor Length	X	A	No silicon revision planned, use workaround.
10. Peripheral short packet issue	X	A	No silicon revision planned, use workaround.
11. Data toggle corruption issue	X	A	No silicon revision planned, use workaround.
12. Code fails to load from EEPROM	X	A	No silicon revision planned, use workaround.
13. ISOCH Endpoint Descriptor error	X	A	No silicon revision planned, use workaround.
14. Missing Endpoint Interrupts in USB Peripheral Mode	X	A	No silicon revision planned, use workaround.

7. Coupled SIE Interrupt Enable Bits

■ **Problem Definition**

Host/Device 1 SIE events will still trigger an interrupt when only the Host/Device 2 SIE Interrupt Enable is set and vise versa.

■ **Parameters Affected**

Host/Device SIE Interrupts.

■ **Trigger Condition(S)**

Setting only 1 Host/Device SIE Interrupt Enable.

■ **Scope of Impact**

The Host/Device global Interrupt Enable bits cannot be used to disable each Host/Device SIE independently. These bits are found in the Interrupt Enable Register (0xC00E).

■ **Workaround**

If an SIE Interrupt is desired, both Host/Device 1 and Host/Device 2 Interrupt Enable bits should be set in the Global Interrupt Enable Register (0xC00E). To properly mask an SIE Interrupt to a single SIE, the lower level Host/Device Interrupt Enable Registers (0xC08C and 0xC0AC) must be used. For example, setting the Host/Device 2 IE Register to 0x0000 will prevent any Host/Device 2 events from generating a Host/Device Interrupt. To disable all SIE interrupts, both Host/Device Interrupt Enable bits in the Interrupt Enable Register should be cleared.

■ **Fix Status**

No silicon revision planned, use workaround.

8. Un-Initialized SIExmsg Registers

■ **Problem Definition**

The SIE1msg and SIE2msg Registers [0x0144 and 0x0148] are not initialized at power up.

■ **Parameters Affected**

HPI interrupts.

■ **Trigger Condition(S)**

Power up initialization.

■ **Scope of Impact**

If you are using the HPI interface in co-processor mode, random data will be written to the SIE1msg and SIE2msg Registers [0x0144 and 0x0148] at power up. This will cause two improper HPI interrupts (HPI_INTR) to occur, one for each of the two SIExmsg Registers.

■ **Workaround**

The external processor should clear the SIExmsg Registers [0x0144 and 0x0148] shortly after nRESET is de-asserted and prior to the expected processing of proper HPI interrupts (generally 10 ms after nRESET is de-asserted).

■ **Fix Status**

No silicon revision planned, use workaround.

10.Peripheral short packet issue

■ **Problem Definition**

When an SIE is configured as a peripheral, the SUSBx_RECEIVE function does not invoke the callback function when it receives a short packet.

■ **Parameters Affected**

SIEx Endpoint x Interrupt (Interrupt 32-47).

■ **Trigger Condition(S)**

This issue is seen when an SIE is configured as a peripheral during an OUT data transfer when the host sends a zero length or short packet. If this occurs, the BIOS will behave as if a full packet was received and will continue to accept data until the Device n Endpoint n Count Register value is satisfied.

■ **Scope of Impact**

All peripheral functions are susceptible to this, as it is a normal occurrence with USB traffic.

■ **Workaround**

To fix this problem, the SIEx Endpoint x Interrupt must be replaced for any peripheral endpoint that is configured as an OUT endpoint.

1. Acquire the file called *susb1.s* from Cypress Support or download a newer version of the frameworks that has this fix applied and includes *susb1.s*.
2. Modify *fwxcfg.h* in your project to have the following flags and define/undef the fix for the endpoints you are using:

```
#define FIX_USB1_EP1
#define FIX_USB1_EP2
#undef  FIX_USB1_EP3
#undef  FIX_USB1_EP4
#undef  FIX_USB1_EP5
#undef  FIX_USB1_EP6
#undef  FIX_USB1_EP7

#undef FIX_USB2_EP1
#undef FIX_USB2_EP2
#undef FIX_USB2_EP3
#undef FIX_USB2_EP4
#undef FIX_USB2_EP5
#undef FIX_USB2_EP6
#undef FIX_USB2_EP7
```

3. Add the new *susb1.s* to the included assembly source files in the make file.
   For example : ASM_SRC := startup.s isrs.s susb1.s
4. Add usb_init somewhere in the startup code. This will likely be in *fwxmain.c* as demonstrated below:

```
void fwx_program_init(void)
{
void usb_init();/* define the prototype */
usb_init();
fwx_init();/* Initialize everything in the base framework. */
}
```

5. Build the project using the modified make file.

■ **Fix Status**

No silicon revision planned, use workaround.