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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Discontinued at Digi-Key
Module/Board Type	MCU, FPGA
Core Processor	ARM® Cortex®-A9
Co-Processor	Zynq-7000 (Z-7045)
Speed	-
Flash Size	32MB
RAM Size	1GB
Connector Type	Samtec UFPS
Size / Dimension	2.05" x 2.99" (52mm x 76mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0745-01-45-1c

1 Table of Contents

2 Overview

Refer to https://wiki.trenz-electronic.de/display/PD/TE0745+TRM for online version of this manual and the rest of the available documentation.
The Trenz Electronic TE0745 is an industrial-grade module integrating a Xilinx Zynq SoC (XC7Z-030, XC7Z-035 or XC7Z-045), 1 GByte DDR3/L SDRAM, 32 MByte SPI Flash memory for configuration and operation and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking strips.

2.1 Key Features

- Industrial grade Xilinx Zynq SoC (XCZ7030, XC7Z035, XC7Z045)
  - Dual-core ARM Cortex-A9 MPCore™ with CoreSight™
  - 250 FPGA PL I/Os (120 LVDS pairs possible)
  - 17 PS MIOs on B2B connector available
- 16-bit wide 1GB DDR3L SDRAM
- 32 MByte QSPI Flash memory
- 4 or 8 GTX transceiver lanes (XC7Z030 variant has 4)
- Gigabit Ethernet transceiver PHY
- EEPROM for storing Ethernet MAC Address
- Hi-speed USB 2.0 ULPI transceiver with full OTG support
- Programmable quad clock generator
- Temperature compensated RTC (real-time clock)
- Plug-on module with 3 × 160-pin high-speed hermaphroditic strips
- On-board high-efficiency DC-DC converters
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- User LED
- Evenly-spread supply pins for good signal integrity
- Rugged for shock and high vibration

Additional assembly options are available for cost or performance optimization upon request.

2.2 Block Diagram

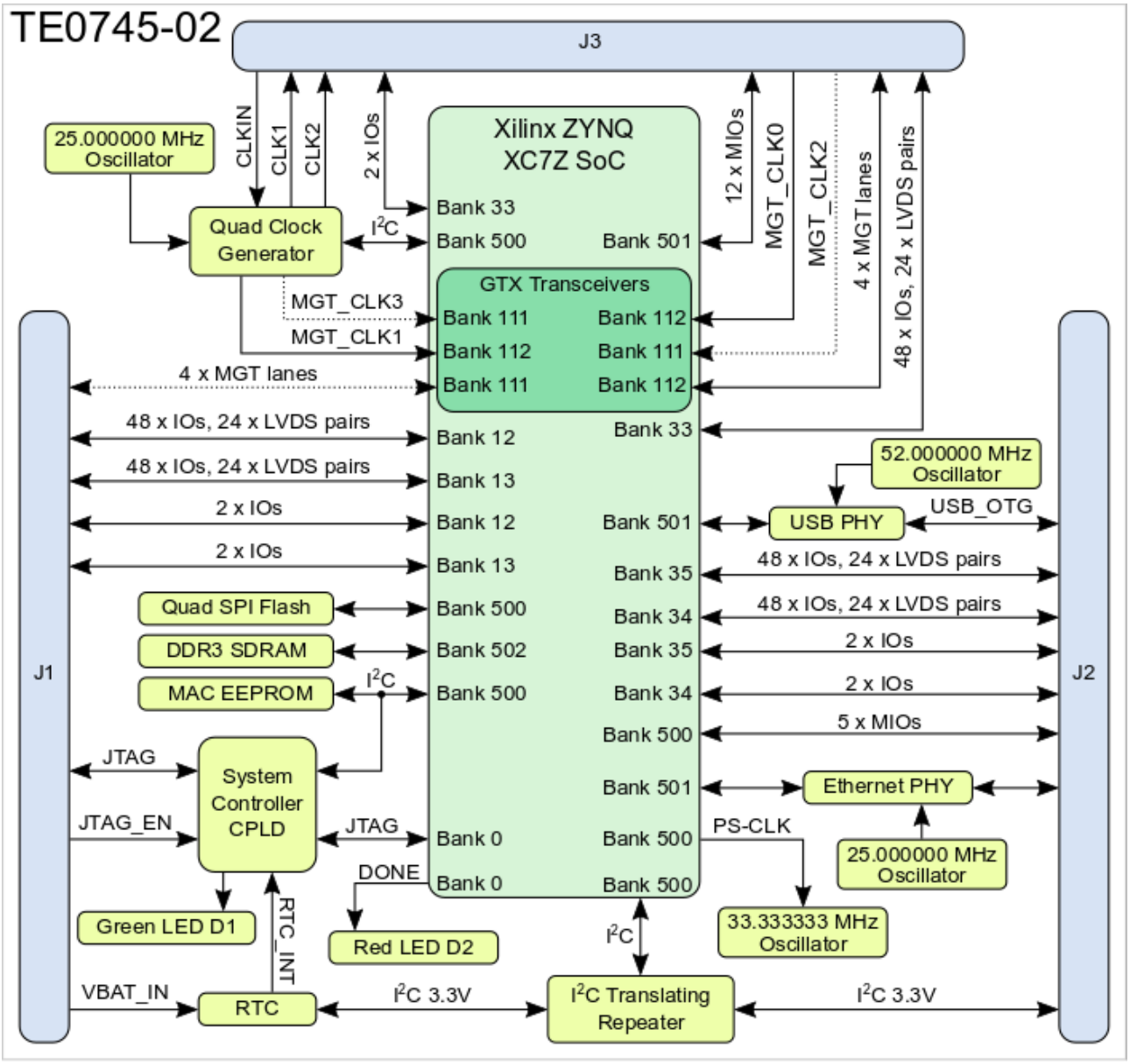

Figure 1: TE0745-02 Block Diagram.

2.3 Main Components

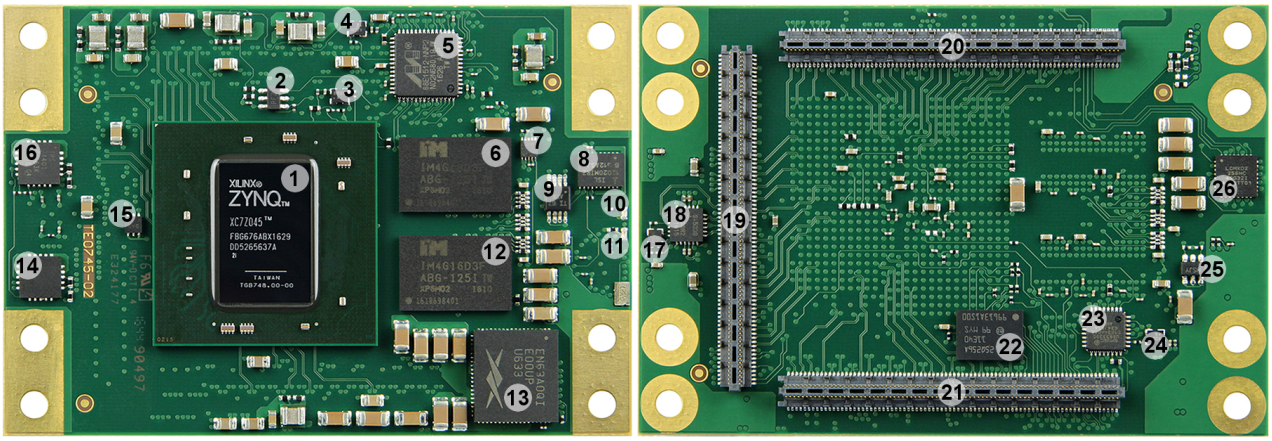

Figure 2: TE0745-02 SoC module.

1. Xilinx Zynq XC7Z family SoC, U1
2. 256 Mbit Quad SPI Flash memory Micron N25Q256A, U12
3. Reference clock signal oscillator SiTime SiT8008BI @33.333333 MHz, U12
4. Reference clock signal oscillator SiTime SiT8008BI @25.000000 MHz, U9
5. Marvell Alaska 88E1512 Gigabit Ethernet PHY, U3
6. Intelligent Memory 512 MByte DDR3L-1600 SDRAM (8 Banks a 32 MWords, 16-bit word width), U3
7. TI TPS51206 DDR3 memory termination regulator with buffered reference voltage VTTREF, U18
8. Intersil ISL12020MIRZ Real-Time-Clock, U24
9. TI TCA9517 level-shifting I^2C bus repeater, U17
10. Red LED, D2
11. Green LED, D1
12. Intelligent Memory 512 MByte DDR3L-1600 SDRAM (8 banks a 32 MWords, 16 Bit word width), U5
13. Altera Enpirion EN63A0QI 12A DC-DC PowerSoC @1.0V (VCCINT), U4
14. TI TPS74401RGW LDO DC-DC regulator @1.2V (MGTAVTT), U8
15. TI TPS72018DRVR LDO DC-DC regulator @1.8V (MGTAUX), U6
16. TI TPS74401RGW LDO DC-DC regulator @1.0V (MGTAVCC), U11
17. Silicon Labs Si5338A I^2C Programmable Quad Clock Generator, U13
18. Reference clock signal oscillator SiTime SiT8008BI @25.000 MHz, U21
19. Samtec ST5-80-1.50-L-D-P-TR 160-pin stacking strips (2 rows a 80 positions), J3
20. Samtec ST5-80-1.50-L-D-P-TR 160-pin stacking strips (2 rows a 80 positions), J1
21. Samtec ST5-80-1.50-L-D-P-TR 160-pin stacking strips (2 rows a 80 positions), J2
22. 256 Mbit Quad SPI Flash memory (Micron N25Q256A), U14
23. Microchip USB3320 USB transceiver PHY , U32
24. Reference clock signal oscillator SiTime SiT8008BI @52.000000 MHz, U33
25. Microchip 24AA025E48 EEPROM for MAC address, U23
26. Lattice Semiconductor MachXO2-256HC System Controller CPLD, U2

2.4 Initial Delivery State

Storage Device Name	Content	Notes
24AA025E48 EEPROM	User content, not programmed	Valid MAC Address from manufacturer.

Storage Device Name	Content	Notes
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	Not programmed	-
eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-
Si5338 OTP NVM	Not programmed	OTP not re-programmable after delivery from factory

Table 1: Initial delivery state.

Table 4: MGT reference clock sources.

[1] **Note:** MGT bank 111 not available at XC7Z030 Zynq SoC.

3.3 JTAG Interface

JTAG interface access is provided through the SoC's PS configuration bank 0 and is available on B2B connector J1.

JTAG Signal	B2B Connector Pin
TCK	J1-143
TDI	J1-142
TDO	J1-145
TMS	J1-144

Table 5: JTAG interface signals.

JTAG_EN pin 148 in B2B connector J1 should be kept low or grounded for normal operation!

3.4 System Controller I/O's

Following special purpose pins are connected to System Controller CPLD:

Pin Name	Mode	Function	B2B Connector Pin	Default Configuration
JTAG_EN	Input	JTAG select	J1-148	During normal operating mode the JTAG_EN pin should be in the low state for JTAG signals to be forwarded to the Zynq SoC. If JTAG_EN pin is set to high or left open the JTAG signals are forwarded to the System Controller CPLD.
RST_IN_N	Input	Reset	J2-131	Low-active Power-On reset pin, controls POR_B-signal (bank 500, pin C23) of Zynq chip.
PS_SRST	Input	Reset	J2-152	Low-active PS system-reset pin of Zynq chip.
BOOTMODE	Output	Boot mode	J2-133	Control line which sets in conjunction with signal 'BOOTMODE1' (B2B-pin J2-133) the boot source of the Zynq chip. See section "Boot Modes". Permanent logic high in standard SC-CPLD firmware.
PWR_PL_OK	Input	Power good	J2-135	Indicates stable state of PL supply voltage (low-active) after power-up sequence.
PWR_PS_OK	Input	Power good	J2-139	Indicates stable state of PS supply voltage (low-active) after power-up sequence.
EN_PL	Output	Enable signal	-	Low active Enable-signal for activating PL supply voltage. Permanent logic high in standard SC-CPLD firmware.

Pin Name	Mode	Function	B2B Connector Pin	Default Configuration
MIO8	Input	PS MIO	-	User I/O (pulled-up to PS_1.8V).
MIO0	Input	PS MIO	J2-137	User I/O.
RTC_INT	Input	Interrupt signal	-	Interrupt-signal from on-board RTC.
LED	Output	LED control	-	Green LED D1, indicates SC-CPLD activity by blinking.

Table 6: System Controller CPLD special purpose I/O pins.

3.5 Quad SPI Interface

Quad SPI Flash (U14) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO1 ... MIO6.

MIO	Signal Name	U14 Pin
1	SPI-CS	C2
2	SPI-DQ0/M0	D3
3	SPI-DQ1/M1	D2
4	SPI-DQ2/M2	C4
5	SPI-DQ3/M3	D4
6	SPI-SCK/M4	B2

Table 7: MIO-pin assignment of the Quad SPI Flash memory IC.

3.6 Gigabit Ethernet Interface

On-board Gigabit Ethernet PHY (U7) is provided with Marvell Alaska 88E1512 IC. The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator (U9). The 125MHz PHY output clock (PHY_CLK125M) is routed to the B2B connector J2 pin 150.

PHY Pin	ZYNQ PS	B2B	Notes
MDC/MDIO	MIO52, MIO53	-	-
PHY LEDs	-	PHY_LED0: J2-144 PHY_LED1: J2-146	-
PHY_LED2 / INTn:	-	J2-148	Active low interrupt line.
PHY_CLK125M	-	J2-150	125 MHz Ethernet PHY clock out.
CONFIG	-	-	Permanent logic high.
RESETn	MIO9	-	Active low reset line.
RGMII	MIO16 ... MIO27	-	Reduced Gigabit Media Independent Interface.

The schematics for the USB connector and required components is different depending on the USB usage. USB standard A or B connectors can be used for Host or Device modes. A Mini USB connector can be used for USB Device mode. A USB Micro connector can be used for Device mode, OTG Mode or Host Mode.

3.8 I2C Interface

The I^2C interface on B2B connector J2 has PS_3.3V as reference voltage and is connected to the Zynq SoC via voltage level translating (3.3V ↔ 1.8V) I^2C bus repeater (U17).:

B2B pin	Signal Schematic Name	Notes
J2-119	I2C_33_SCL	3.3V reference voltage
J2-121	I2C_33_SDA	3.3V reference voltage

Table 10: Pin assignment of the B2B I^2C interface.

The on-module I^2C interface works with reference voltage 1.8V:

PS Bank 500	Signal Schematic Name	Notes
MIO 10	I2C_SCL	1.8V reference voltage
MIO 11	I2C_SDA	1.8V reference voltage

Table 11: MIO-pin assignment of the on-module I^2C interface.

Except the on-module RTC (U24), all other on-module I^2C slave devices are operating with the reference voltage PS_1.8V.

I^2C addresses for on-module devices are listed in the table below:

I2C Device	I2C Address	Notes
Zynq chip U1, bank 500 (PS MIO), pins MIO10 (SCL), MIO11 (SDA)	User programmable.	Configured as I^2C by default.
Quad programmable PLL clock generator U16: pins 12 (SCL), 19 (SDA)	0x70	-
MAC Address EEPROM U23, pins 1 (SCL), 3 (SDA)	0x53	-
SC CPLD U2, bank 2, pins 16 (SDA), 17 (SCL)	User programmable.	-
RTC, U24	0x6F	-
RTC RAM, U24	0x57	-

Table 12: Module's I^2C-interfaces overview.

4 Boot Process

TE0745 module supports different boot modes which are configurable by the control line 'BOOTMODE' and 'BOOTMODE_1'. The line 'BOOTMODE' is available on B2B connector pin J2-133, the line 'BOOTMODE_1' is connected to the System Controller CPLD on bank 1, pin 21 (permanent logic high in standard SC-CPLD firmware).The boot mode selection will be set by the Zynq's PS MIO pins MIO3...MIO5.

Following table describes how to set the control lines to configure the boot mode:

Boot Mode	MIO5 (BOOTMODE_1), SC CPLD	MIO4 (BOOTMODE), J2-133	Note
JTAG	0	0	-
QSPI Flash Memory	1	0	standard mode in current configuration.
SD-Card	1	1	SD-Card on base board necessary.

Table 13: Selectable boot modes.

In delivery state of the SoM the boot mode depends on the configured SC-CPLD firmware. Basically MIO5 is set to 1 and JTAG is in cascade.

5 On-board Peripherals

5.1 System Controller CPLD

The System Controller CPLD (U2) is provided by Lattice Semiconductor LCMXO2-256HC (MachXO2 Product Family). The SC-CPLD is the central system management unit where essential control signals are logically linked by the implemented logic in CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG and I^2C between the on-board peripherals and to the FPGA-module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and to display the programming state of the FPGA module.

5.2 Quad SPI Flash Memory

On-board QSPI flash memory (U14) on the TE0745-02 is provided by Micron Serial NOR Flash Memory N25Q256A with 256 Mbit (32 MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

⚠ SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

5.3 Gigabit Ethernet PHY

On-board Gigabit Ethernet PHY (U7) is provided with Marvell Alaska 88E1512 IC (U8). The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (U9), the 125MHz output clock signal CLK_125MHZ is connected to the pin J2-150 of B2B connector J2.

5.4 High-speed USB ULPI PHY

Hi-speed USB ULPI PHY (U32) is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0 via MIO28..39, bank 501 (see also section). The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator (U33).

5.5 MAC Address EEPROM

A Microchip 24AA025E48 serial EEPROM (U23) contains a globally unique 48-bit node address, which is compatible with EUI-48(TM) specification. The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. It is accessible over I^2C bus with slave device address 0x53.

5.6 RTC - Real Time Clock

An temperature compensated Intersil ISL12020M is used as Real Time Clock (U24). Battery voltage must be supplied to the clock from the base board via pin 'VBAT_IN' (J1-146). Battery backed registers can be accessed over I^2C bus at slave address 0x6F. General purpose RAM of the RTC can be accessed at I^2C slave address 0x57. RTC IC is supported by Linux so it can be used as hwclock device. The interrupt line 'RTC_INT' of the RTC is connected to System Controller CPLD bank 3 pin 4.

5.7 Programmable PLL Clock (Phase-Locked Loop)

There is a Silicon Labs I^2C programmable quad PLL clock generator Si5338A (U16) on-board. It's output frequencies can be programmed by using the I^2C-bus with address 0x70.

A 25 MHz (U21) oscillator is connected to pin 3 (IN3) and is used to generate the output clocks.

Once running, the frequency and other parameters can be changed by programming the device using the I^2C-bus connected between the Zynq module (master) and reference clock signal generator (slave).

Si5338A Pin	Signal Name / Description	Connected To	Direction	Note
IN1	CLKIN_P	B2B, J3-76	Input	Reference input clock from base board.
IN2	CLKIN_N	B2B, J3-74	Input	
IN3	Reference input clock.	Oscillator U21, pin 3	Input	25.000000 MHz oscillator, Si8008BI.
IN4	-	GND	Input	I^2C slave device address LSB (0x70 default address).
IN5	-	Not connected.	Input	Not used.
IN6	-	GND	Input	Not used.
CLK0A	MGT_CLK1_P	Zynq Soc U1, pin U6	Output	MGT bank 112 reference clock.
CLK0B	MGT_CLK1_N	Zynq Soc U1, pin U5	Output	
CLK1A	CLK1_P	B2B, J3-80	Output	Reference clock output to base board.
CLK1B	CLK1_N	B2B, J3-82	Output	
CLK2A	CLK2_P	B2B, J3-86	Output	Reference clock output to base board.
CLK2B	CLK2_P	B2B, J3-88	Output	
CLK3A	MGT_CLK3_P	Zynq Soc U1, pin AA6	Output	MGT bank 111 reference clock.
CLK3B	MGT_CLK3_N	Zynq Soc U1, pin AA6	Output	

Table 14: Programmable quad PLL clock generator inputs and outputs.

6 Power and Power-On Sequence

6.1 Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input Pin	Typical Current
PL_VIN	TBD*
PS_VIN	TBD*
PS_3.3V	TBD*

Table 17: Typical power consumption. *to be determined soon with reference design setup.

Power supply with minimum current capability of 3A for system startup is recommended.

For the lowest power consumption and highest efficiency of on board DC-DC regulators it is recommended to powering the module from one single 3.3V supply. All input power supplies have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

The on-board voltages of the TE0745 SoC module will be powered-up in order of a determined sequence after the external voltages 'PL_VIN', 'PS_VIN' and 'PS_3.3V' are available. All those power-rails can be powered up, with 3.3V power sources, also shared.

> To avoid any damage to the module, check for stabilized on-board voltages should be carried out(i.e. power good and enable signals) before powering up any SoC's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good"-signals have to be asserted before other voltages like PL bank's I/O voltages can be powered up.

It is important that all baseboard I/Os are tri-stated at power-on until the "Power Good"-signals 'PWR_PS_OK' (J2-139) and 'PWR_PL_OK' (J2-135) are high, meaning that all on-module voltages have become stable and module is properly powered up.

6.2 Power Distribution Dependencies

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DCDC converters, which power up further DCDC converters and the particular on-board voltages:

6.5 Power Rails

Voltages on B2B Connectors	B2B J1 Pin	B2B J2 Pin	B2B J3 Pin	Input/ Output	Note
PL_VIN	147, 149, 151, 153, 155, 157, 159	-	-	Input	module supply voltage
PS_VIN	-	154, 156, 158	-	Input	module supply voltage
PS_3.3V	-	160	-	Input	module supply voltage
VCCIO12	54, 55	-	-	Input	high range bank I/O voltage
VCCIO13	112, 113	-	-	Input	high range bank I/O voltage
VCCIO33	-	-	115, 120	Input	high performance bank I/O voltage
VCCIO34	29, 30		-	Input	high performance bank I/O voltage
VCCIO35	87, 88		-	Input	high performance bank I/O voltage
VBAT_IN	146	-	-	Input	RTC (battery-backed) supply voltage
PS_1.8V	-	130	-	Output	internal 1.8V voltage level (Process System)

Table 18: Power rails of the SoC module on B2B connectors.

6.6 Bank Voltages

Bank	Schematic Name	Voltage	Voltage Range
0 (config)	VCCIO_0	PL_1.8V, if R67 is equipped PS_1.8V, if R68 is equipped	-
500 (MIO0)	PS_1.8V	1.8V	-
501 (MIO1)	PS_1.8V	1.8V	-
502 (DDR3)	1.35V	1.35V	-
12 HR	VCCIO_12	User	HR: 1.2V to 3.3V
13 HR	VCCIO_13	User	HR: 1.2V to 3.3V
33 HP	VCCIO_33	User	HP: 1.2V to 1.8V
34 HP	VCCIO_34	User	HP: 1.2V to 1.8V
35 HP	VCCIO_35	User	HP: 1.2V to 1.8V

Table 19: Range of SoC module's bank voltages.

7.4 Connector Speed Ratings

The connector speed rating depends on the stacking height:

Stacking height	Speed rating
4 mm, Single-Ended	13GHz/26Gbps
4 mm, Differential	13.5GHz/27Gbps
5 mm, Single-Ended	13.5GHz/27Gbps
5 mm, Differential	20GHz/40 Gbps

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

7.5 Manufacturer Documentation

8 Variants Currently In Production

Module Variant	Zynq SoC	SoC Junction Temperature	Operating Temperature Range
TE0745-02-30-1I	XC7Z030-1FBG676I	–40°C to +100°C	Industrial
TE0745-02-35-1C	XC7Z035-1FBG676C	0°C to +85°C	Commercial
TE0745-02-45-1C	XC7Z045-1FBG676C	0°C to +85°C	Commercial
TE0745-02-45-2I	XC7Z045-2FBG676I	–40°C to +100°C	Industrial

Table 20: Module variants.

Parameter	Min	Max	Units	Notes	Reference Document
PL I/O bank supply voltage for HR I/O banks (VCCO)	1.14	3.465	V	-	Xilinx datasheet DS191
PL I/O bank supply voltage for HP I/O banks (VCCO)	1.14	1.89	V	-	Xilinx datasheet DS191
I/O input voltage for HR I/O banks	-0.20	VCCO_X+ 0.20	V	-	Xilinx datasheet DS191
I/O input voltage for HP I/O banks	-0.20	VCCO_X+ 0.20	V	-	Xilinx datasheet DS191
GT receiver (RXP/RXN) and transmitter (TXP/TXN)	(*)	(*)	V	(*) Check datasheet	Xilinx datasheet DS191
Voltage on Module JTAG pins	3.135	3.6	V	JTAG signals forwarded to Zynq module config bank 0	MachX02 Family Data Sheet

Table 22: Module recommended operating conditions.

Please check Xilinx datasheet DS191 (for XC7Z030) for complete list of absolute maximum and recommended operating ratings.

9.3 Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

Extended grade: 0°C to +85°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

9.4 Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.

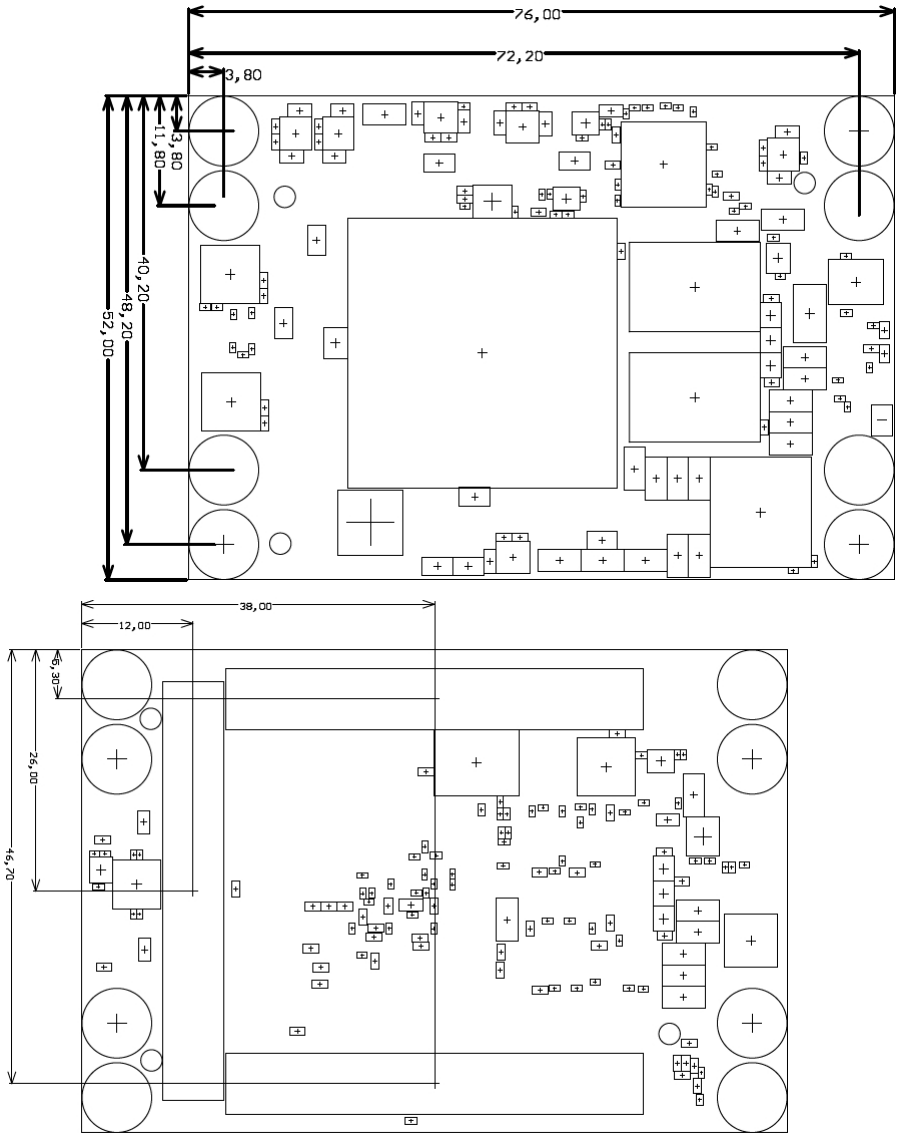

Figure 6: Physical dimensions of the TE0745 SoC module.

10 Revision History

10.1 Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
2016-10-11	02	• First Production release • Refer to Changes list in Schematic for further details in changes to REV01	-	TE0745-02
2016-04-18	01	• Prototypes	-	TE0745-01

Table 23: Module hardware revision history.

Hardware revision number is written on the PCB board together with the module model number separated by the dash.

Figure 7: TE0745 module revision number.

10.2 Document Change History

Date	Revision	Contributors	Description
2017-11-14	V.80	John Hartfiel	• Update B2B Section
2017-11-13	V.79	Ali Naseri, Jan Kumann, John Hartfiel	• First TRM release

Table 24: Document change history.

11 Disclaimer

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11.6 REACH, RoHS and WEEE

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WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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