# Trenz Electronic GmbH - TE0745-01-45-2I Datasheet

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**Applications of Embedded - Microcontroller,**

| **Details** | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Module/Board Type | MCU, FPGA |
| Core Processor | ARM® Cortex®-A9 |
| Co-Processor | Zynq-7000 (Z-7045) |
| Speed | - |
| Flash Size | 32MB |
| RAM Size | 1GB |
| Connector Type | Samtec UFPS |
| Size / Dimension | 2.05" x 2.99" (52mm x 76mm) |
| Operating Temperature | -40°C ~ 85°C |
| Purchase URL | https://www.e-xfl.com/product-detail/trenz-electronic/te0745-01-45-2i |

# 1 Table of Contents

# 2 Overview

Refer to https://wiki.trenz-electronic.de/display/PD/TE0745+TRM for online version of this manual and the rest of the available documentation.
The Trenz Electronic TE0745 is an industrial-grade module integrating a Xilinx Zynq SoC (XC7Z-030, XC7Z-035 or XC7Z-045), 1 GByte DDR3/L SDRAM, 32 MByte SPI Flash memory for configuration and operation and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking strips.

## 2.1 Key Features

- Industrial grade Xilinx Zynq SoC (XCZ7030, XC7Z035, XC7Z045)
  - Dual-core ARM Cortex-A9 MPCore™ with CoreSight™
  - 250 FPGA PL I/Os (120 LVDS pairs possible)
  - 17 PS MIOs on B2B connector available
- 16-bit wide 1GB DDR3L SDRAM
- 32 MByte QSPI Flash memory
- 4 or 8 GTX transceiver lanes (XC7Z030 variant has 4)
- Gigabit Ethernet transceiver PHY
- EEPROM for storing Ethernet MAC Address
- Hi-speed USB 2.0 ULPI transceiver with full OTG support
- Programmable quad clock generator
- Temperature compensated RTC (real-time clock)
- Plug-on module with 3 × 160-pin high-speed hermaphroditic strips
- On-board high-efficiency DC-DC converters
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- User LED
- Evenly-spread supply pins for good signal integrity
- Rugged for shock and high vibration

Additional assembly options are available for cost or performance optimization upon request.

## 2.2 Block Diagram

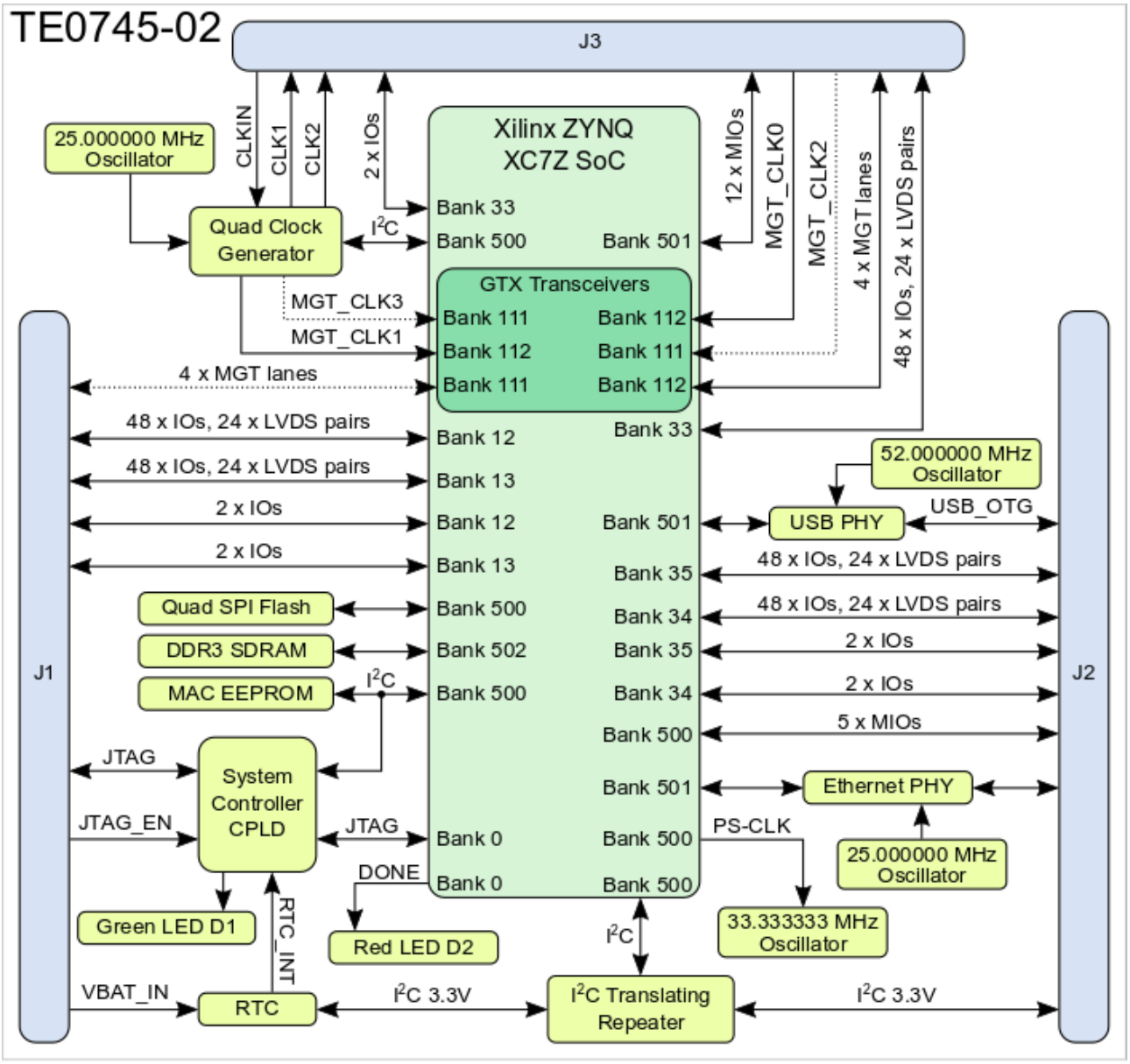


**Figure 1**: TE0745-02 Block Diagram.

| Storage Device Name | Content | Notes |
|---|---|---|
| SPI Flash OTP Area | Empty, not programmed | Except serial number programmed by flash vendor. |
| SPI Flash Quad Enable bit | Programmed | - |
| SPI Flash main array | Not programmed | - |
| eFUSE USER | Not programmed | - |
| eFUSE Security | Not programmed | - |
| Si5338 OTP NVM | Not programmed | OTP not re-programmable after delivery from factory |

**Table 1**: Initial delivery state.

# 3 Signals, Interfaces and Pins

## 3.1 Board to Board (B2B) I/O's

The B2B connectors are high-speed hermaphroditic stacking strips providing modular interface to the SoC's PL and PS I/Os. Both single ended and differential signaling LVDS pairs are supported.

| Bank | Type | B2B Connector | I/O Signal Count | LVDS Pairs Count | Bank Voltage | Notes |
|---|---|---|---|---|---|---|
| 12 | HR | J1 | 50 | 24 | VCCIO_12 pins J1-54, J1-55 | Voltage range 1.2V to 3.3V |
| 13 | HR | J1 | 50 | 24 | VCCIO_13 pins J1-112, J1-113 | Voltage range 1.2V to 3.3V |
| 33 | HP | J3 | 50 | 24 | VCCIO_33 pins J3-115, J3-120 | Voltage range 1.2V to 1.8V |
| 34 | HP | J2 | 50 | 24 | VCCIO_34 pins J2-29, J2-30 | Voltage range 1.2V to 1.8V |
| 35 | HP | J2 | 50 | 24 | VCCIO_35 pins J2-87, J2-88 | Voltage range 1.2V to 1.8V |
| 500 | MIO | J2 | 5 | - | 1.8V | MIO0, MIO12 ... MIO15, user configurable I/O's on B2B |
| 501 | MIO | J3 | 12 | - | 1.8V | MIO40 ... MIO51, user configurable I/O's on B2B |

**Table 2**: Count, type and voltage range of SoC's PL and PS I/O banks pins available through B2B connectors.

All MIO banks are powered from on-module DC-DC power rail. All PL I/O Banks have separate VCCO pins in the B2B connectors, valid VCCO should be supplied from the baseboard.

For detailed information about the pin-out, please refer to the Pin-out Table.

The configuration of the I/O's MIO0, MIO12 ... MIO15 and MIO40 ... MIO51 are depending on the base-board peripherals connected to these pins.

## 3.2 MGT Lanes

MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TX/RX) differential pair, two signals each or four signals total per one MGT lane. Following table lists lane number, MGT bank number, transceiver type, signal schematic name, board-to-board pin connection and FPGA pins connection:

| Lane | Bank | Type | Signal Name | B2B Pin | FPGA Pin |
|---|---|---|---|---|---|
| 0 | 112 | GTX | • MGT_RX0_P<br>• MGT_RX0_N<br>• MGT_TX0_P<br>• MGT_TX0_N | • J3-50<br>• J3-52<br>• J3-51<br>• J3-53 | • MGTHRXP0_112, AB4<br>• MGTHRXN0_112, AB3<br>• MGTHTXP0_112, AA2<br>• MGTHTXN0_112, AA1 |
| 1 | 112 | GTX | • MGT_RX1_P<br>• MGT_RX1_N<br>• MGT_TX1_P<br>• MGT_TX1_N | • J3-56<br>• J3-58<br>• J3-57<br>• J3-59 | • MGTHRXP1_112, Y4<br>• MGTHRXN1_112, Y3<br>• MGTHTXP1_112, W2<br>• MGTHTXN1_112, W1 |
| 2 | 112 | GTX | • MGT_RX2_P<br>• MGT_RX2_N<br>• MGT_TX2_P<br>• MGT_TX2_N | • J3-62<br>• J3-64<br>• J3-63<br>• J3-65 | • MGTHRXP2_112, V4<br>• MGTHRXN2_112, V3<br>• MGTHTXP2_112, U2<br>• MGTHTXN2_112, U1 |
| 3 | 112 | GTX | • MGT_RX3_P<br>• MGT_RX3_N<br>• MGT_TX3_P<br>• MGT_TX3_N | • J3-68<br>• J3-70<br>• J3-69<br>• J3-71 | • MGTHRXP3_112, T4<br>• MGTHRXN3_112, T3<br>• MGTHTXP3_112, R2<br>• MGTHTXN3_112, R1 |
| 4 | 111 [1)] | GTX | • MGT_RX4_P<br>• MGT_RX4_N<br>• MGT_TX4_P<br>• MGT_TX4_N | • J1-23<br>• J1-21<br>• J1-22<br>• J1-20 | • MGTHRXP0_111, AD8<br>• MGTHRXN0_111, AD7<br>• MGTHTXP0_111, AF8<br>• MGTHTXN0_111, AF7 |
| 5 | 111 [1)] | GTX | • MGT_RX5_P<br>• MGT_RX5_N<br>• MGT_TX5_P<br>• MGT_TX5_N | • J1-17<br>• J1-15<br>• J1-16<br>• J1-14 | • MGTHRXP1_111, AE6<br>• MGTHRXN1_111, AE5<br>• MGTHTXP1_111, AF4<br>• MGTHTXN1_111, AF3 |
| 6 | 111 [1)] | GTX | • MGT_RX6_P<br>• MGT_RX6_N<br>• MGT_TX6_P<br>• MGT_TX6_N | • J1-11<br>• J1-9<br>• J1-10<br>• J1-8 | • MGTHRXP2_111, AC6<br>• MGTHRXN2_111, AC5<br>• MGTHTXP2_111, AE2<br>• MGTHTXN2_111, AE1 |
| 7 | 111 [1)] | GTX | • MGT_RX7_P<br>• MGT_RX7_N<br>• MGT_TX7_P<br>• MGT_TX7_N | • J1-5<br>• J1-3<br>• J1-4<br>• J1-2 | • MGTHRXP3_111, AD4<br>• MGTHRXN3_111, AD3<br>• MGTHTXP3_111, AC2<br>• MGTHTXN3_111, AC1 |

**Table 3**: SoC's MGT lanes connections to the B2B connectors.

Below are listed MGT banks reference clock sources.

| Clock signal | Bank | Source | FPGA Pin | Notes |
|---|---|---|---|---|
| MGT_CLK0_P | 112 | B2B, J3-75 | MGTREFCLK0P_112, R6 | Supplied by the carrier board. |
| MGT_CLK0_N | 112 | B2B, J3-77 | MGTREFCLK0N_112, R5 | Supplied by the carrier board. |
| MGT_CLK1_P | 112 | U16, CLK0A | MGTREFCLK1P_112, U6 | On-module Si5338A. |
| MGT_CLK1_N | 112 | U16, CLK0B | MGTREFCLK1N_112, U5 | On-module Si5338A. |
| MGT_CLK2_P | 111 [1)] | B2B, J3-81 | MGTREFCLK0P_111, W6 | Supplied by the carrier board. |
| MGT_CLK2_N | 111 [1)] | B2B, J3-83 | MGTREFCLK0N_111, W5 | Supplied by the carrier board. |
| MGT_CLK3_P | 111 [1)] | U16, CLK3A | MGTREFCLK1P_111, AA6 | On-module Si5338A. |
| MGT_CLK3_N | 111 [1)] | U16, CLK3B | MGTREFCLK1N_111, AA5 | On-module Si5338A. |

**Table 4:** MGT reference clock sources.

[1] **Note:** MGT bank 111 not available at XC7Z030 Zynq SoC.

## 3.3 JTAG Interface

JTAG interface access is provided through the SoC's PS configuration bank 0 and is available on B2B connector J1.

| JTAG Signal | B2B Connector Pin |
|---|---|
| TCK | J1-143 |
| TDI | J1-142 |
| TDO | J1-145 |
| TMS | J1-144 |

**Table 5**: JTAG interface signals.

JTAG_EN pin 148 in B2B connector J1 should be kept low or grounded for normal operation!

## 3.4 System Controller I/O's

Following special purpose pins are connected to System Controller CPLD:

| Pin Name | Mode | Function | B2B Connector Pin | Default Configuration |
|---|---|---|---|---|
| JTAG_EN | Input | JTAG select | J1-148 | During normal operating mode the JTAG_EN pin should be in the low state for JTAG signals to be forwarded to the Zynq SoC. If JTAG_EN pin is set to high or left open the JTAG signals are forwarded to the System Controller CPLD. |
| RST_IN_N | Input | Reset | J2-131 | Low-active Power-On reset pin, controls POR_B-signal (bank 500, pin C23) of Zynq chip. |
| PS_SRST | Input | Reset | J2-152 | Low-active PS system-reset pin of Zynq chip. |
| BOOTMODE | Output | Boot mode | J2-133 | Control line which sets in conjunction with signal 'BOOTMODE1' (B2B-pin J2-133) the boot source of the Zynq chip. See section "Boot Modes".<br>Permanent logic high in standard SC-CPLD firmware. |
| PWR_PL_OK | Input | Power good | J2-135 | Indicates stable state of PL supply voltage (low-active) after power-up sequence. |
| PWR_PS_OK | Input | Power good | J2-139 | Indicates stable state of PS supply voltage (low-active) after power-up sequence. |
| EN_PL | Output | Enable signal | - | Low active Enable-signal for activating PL supply voltage.<br>Permanent logic high in standard SC-CPLD firmware. |

| Pin Name | Mode | Function | B2B Connector Pin | Default Configuration |
|---|---|---|---|---|
| MIO8 | Input | PS MIO | - | User I/O (pulled-up to PS_1.8V). |
| MIO0 | Input | PS MIO | J2-137 | User I/O. |
| RTC_INT | Input | Interrupt signal | - | Interrupt-signal from on-board RTC. |
| LED | Output | LED control | - | Green LED D1, indicates SC-CPLD activity by blinking. |

**Table 6**: System Controller CPLD special purpose I/O pins.

## 3.5 Quad SPI Interface

Quad SPI Flash (U14) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO1 ... MIO6.

| MIO | Signal Name | U14 Pin |
|---|---|---|
| 1 | SPI-CS | C2 |
| 2 | SPI-DQ0/M0 | D3 |
| 3 | SPI-DQ1/M1 | D2 |
| 4 | SPI-DQ2/M2 | C4 |
| 5 | SPI-DQ3/M3 | D4 |
| 6 | SPI-SCK/M4 | B2 |

**Table 7**: MIO-pin assignment of the Quad SPI Flash memory IC.

## 3.6 Gigabit Ethernet Interface

On-board Gigabit Ethernet PHY (U7) is provided with Marvell Alaska 88E1512 IC. The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from the on-board 25.000000 MHz oscillator (U9). The 125MHz PHY output clock (PHY_CLK125M) is routed to the B2B connector J2 pin 150.

| PHY Pin | ZYNQ PS | B2B | Notes |
|---|---|---|---|
| MDC/MDIO | MIO52, MIO53 | - | - |
| PHY LEDs | - | PHY_LED0: J2-144<br>PHY_LED1: J2-146 | - |
| PHY_LED2 / INTn: | - | J2-148 | Active low interrupt line. |
| PHY_CLK125M | - | J2-150 | 125 MHz Ethernet PHY clock out. |
| CONFIG | - | - | Permanent logic high. |
| RESETn | MIO9 | - | Active low reset line. |
| RGMII | MIO16 ... MIO27 | - | Reduced Gigabit Media Independent Interface. |

| PHY Pin | ZYNQ PS | B2B | Notes |
|---|---|---|---|
| SGMII | - | - | Serial Gigabit Media Independent Interface. |
| MDI | - | PHY_MDI0: J2-120 / J2-122<br>PHY_MDI1: J2-126 / J2-128<br>PHY_MDI2: J2-132 / J2-134<br>PHY_MDI3: J2-138 / J2-140 | Media Dependent Interface. |

**Table 8**: Ethernet PHY interface connections.

## 3.7 USB Interface

USB PHY (U32) is provided by USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0. I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator (U33).

| PHY Pin | ZYNQ PS | B2B | Notes |
|---|---|---|---|
| ULPI | MIO28 ... MIO39 | - | Zynq USB0 MIO pins are connected to the PHY. |
| REFCLK | - | - | 52MHz from on board oscillator (U33). |
| REFSEL[0..2] | - | - | All pins set to GND selects the external reference clock frequency (52.000000 MHz). |
| RESETB | MIO7 | - | Low active USB PHY Reset (pulled-up to PS_1.8V). |
| CLKOUT | MIO36 | - | Set to logic high to select reference clock (oscillator U33) operation mode. |
| DP, DM | - | OTG_D_P, OTG_D_N, pin J2-149 / J2-151 | USB data lines. |
| CPEN | - | VBUS_V_EN, pin J2-141 | External USB power switch active-high enable signal. |
| VBUS | - | USB_VBUS, pin J2-145 | Connect to USB VBUS via a series of resistors, see reference schematics. |
| ID | - | OTG_ID, pin J2-143 | For an A-device connect to the ground. For a B-device, leave floating. |

**Table 9**: USB PHY interface connections.

# 4 Boot Process

TE0745 module supports different boot modes which are configurable by the control line 'BOOTMODE' and 'BOOTMODE_1'. The line 'BOOTMODE' is available on B2B connector pin J2-133, the line 'BOOTMODE_1' is connected to the System Controller CPLD on bank 1, pin 21 (permanent logic high in standard SC-CPLD firmware).The boot mode selection will be set by the Zynq's PS MIO pins MIO3...MIO5.

Following table describes how to set the control lines to configure the boot mode:

| Boot Mode | MIO5 (BOOTMODE_1), SC CPLD | MIO4 (BOOTMODE), J2-133 | Note |
|---|---|---|---|
| JTAG | 0 | 0 | - |
| QSPI Flash Memory | 1 | 0 | standard mode in current configuration. |
| SD-Card | 1 | 1 | SD-Card on base board necessary. |

**Table 13**: Selectable boot modes.

In delivery state of the SoM the boot mode depends on the configured SC-CPLD firmware. Basically MIO5 is set to 1 and JTAG is in cascade.

# 5 On-board Peripherals

## 5.1 System Controller CPLD

The System Controller CPLD (U2) is provided by Lattice Semiconductor LCMXO2-256HC (MachXO2 Product Family). The SC-CPLD is the central system management unit where essential control signals are logically linked by the implemented logic in CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG and $I^2C$ between the on-board peripherals and to the FPGA-module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and to display the programming state of the FPGA module.

## 5.2 Quad SPI Flash Memory

On-board QSPI flash memory (U14) on the TE0745-02 is provided by Micron Serial NOR Flash Memory N25Q256A with 256 Mbit (32 MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

⚠ SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

## 5.3 Gigabit Ethernet PHY

On-board Gigabit Ethernet PHY (U7) is provided with Marvell Alaska 88E1512 IC (U8). The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (U9), the 125MHz output clock signal CLK_125MHZ is connected to the pin J2-150 of B2B connector J2.

## 5.4 High-speed USB ULPI PHY

Hi-speed USB ULPI PHY (U32) is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0 via MIO28..39, bank 501 (see also section). The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator (U33).

## 5.5 MAC Address EEPROM

A Microchip 24AA025E48 serial EEPROM (U23) contains a globally unique 48-bit node address, which is compatible with EUI-48(TM) specification. The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores the 48-bit node address and is write protected, the other block is available for application use. It is accessible over $I^2C$ bus with slave device address 0x53.

## 5.6 RTC - Real Time Clock

An temperature compensated Intersil ISL12020M is used as Real Time Clock (U24). Battery voltage must be supplied to the clock from the base board via pin 'VBAT_IN' (J1-146). Battery backed registers can be accessed over $I^2C$ bus at slave address 0x6F. General purpose RAM of the RTC can be accessed at $I^2C$ slave address 0x57. RTC IC is supported by Linux so it can be used as hwclock device. The interrupt line 'RTC_INT' of the RTC is connected to System Controller CPLD bank 3 pin 4.

## 5.7 Programmable PLL Clock (Phase-Locked Loop)

There is a Silicon Labs $I^2C$ programmable quad PLL clock generator Si5338A (U16) on-board. It's output frequencies can be programmed by using the $I^2C$-bus with address 0x70.

A 25 MHz (U21) oscillator is connected to pin 3 (IN3) and is used to generate the output clocks.

Once running, the frequency and other parameters can be changed by programming the device using the $I^2C$-bus connected between the Zynq module (master) and reference clock signal generator (slave).

| Si5338A Pin | Signal Name / Description | Connected To | Direction | Note |
|---|---|---|---|---|
| IN1 | CLKIN_P | B2B, J3-76 | Input | Reference input clock from base board. |
| IN2 | CLKIN_N | B2B, J3-74 | Input | |
| IN3 | Reference input clock. | Oscillator U21, pin 3 | Input | 25.000000 MHz oscillator, Si8008BI. |
| IN4 | - | GND | Input | $I^2C$ slave device address LSB (0x70 default address). |
| IN5 | - | Not connected. | Input | Not used. |
| IN6 | - | GND | Input | Not used. |
| CLK0A | MGT_CLK1_P | Zynq Soc U1, pin U6 | Output | MGT bank 112 reference clock. |
| CLK0B | MGT_CLK1_N | Zynq Soc U1, pin U5 | Output | |
| CLK1A | CLK1_P | B2B, J3-80 | Output | Reference clock output to base board. |
| CLK1B | CLK1_N | B2B, J3-82 | Output | |
| CLK2A | CLK2_P | B2B, J3-86 | Output | Reference clock output to base board. |
| CLK2B | CLK2_P | B2B, J3-88 | Output | |
| CLK3A | MGT_CLK3_P | Zynq Soc U1, pin AA6 | Output | MGT bank 111 reference clock. |
| CLK3B | MGT_CLK3_N | Zynq Soc U1, pin AA6 | Output | |

**Table 14:** Programmable quad PLL clock generator inputs and outputs.

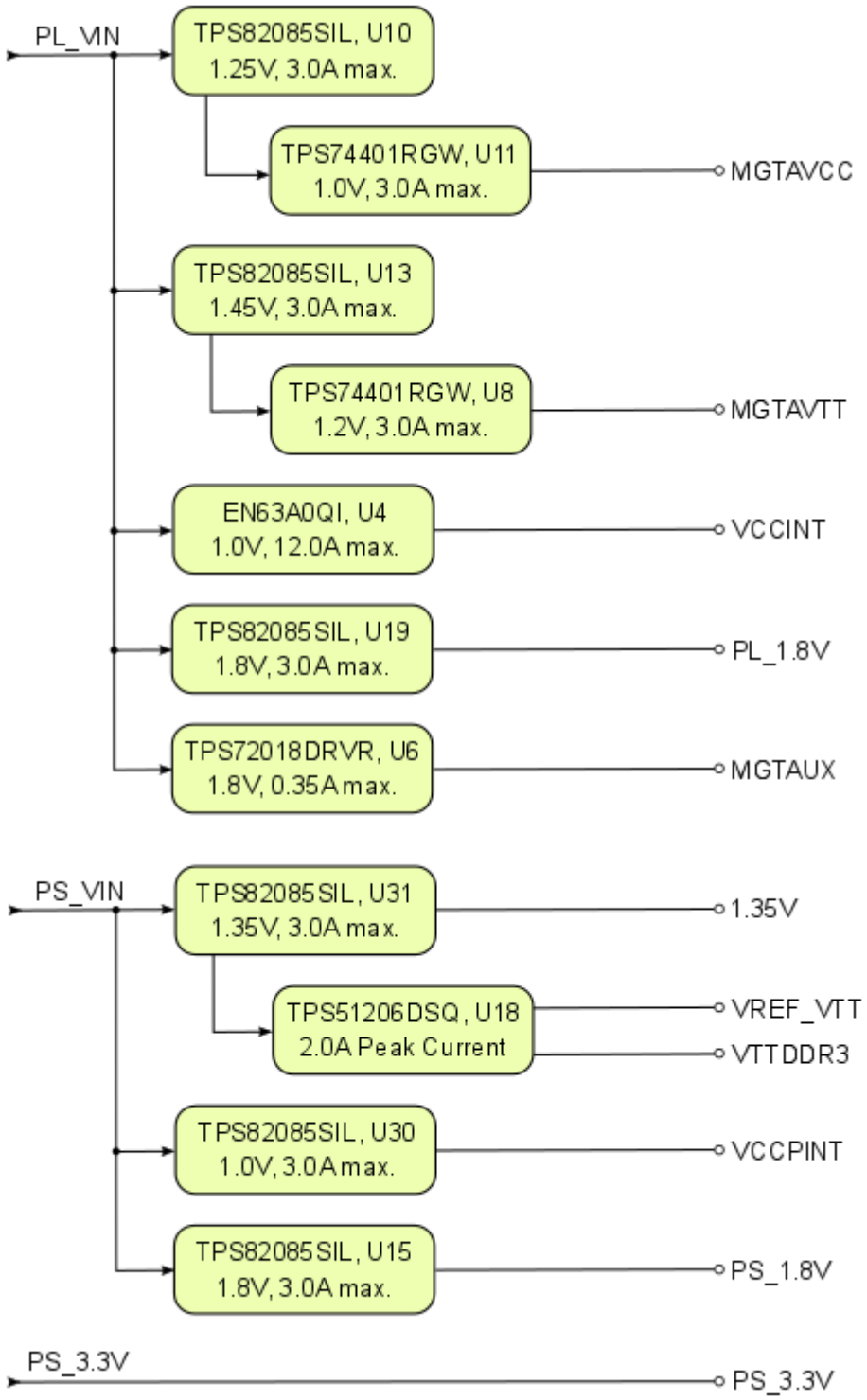


**Figure 3**: Power Distribution Diagram

See Xilinx data sheet DS191 for additional information. User should also check related base board documentation when intending base board design for TE0745 module.

⚠ Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

## 6.3 Power-On Sequence Diagram

The TE0745 SoM meets the recommended criteria to power up the Xilinx Zynq MPSoC properly by keeping a specific sequence of enabling the on-board DCDC converters dedicated to the particular functional units of the Zynq chip and powering up the on-board voltages.

Following diagram clarifies the sequence of enabling the particular on-board voltages, which will power-up in descending order as listed in the blocks of the diagram:

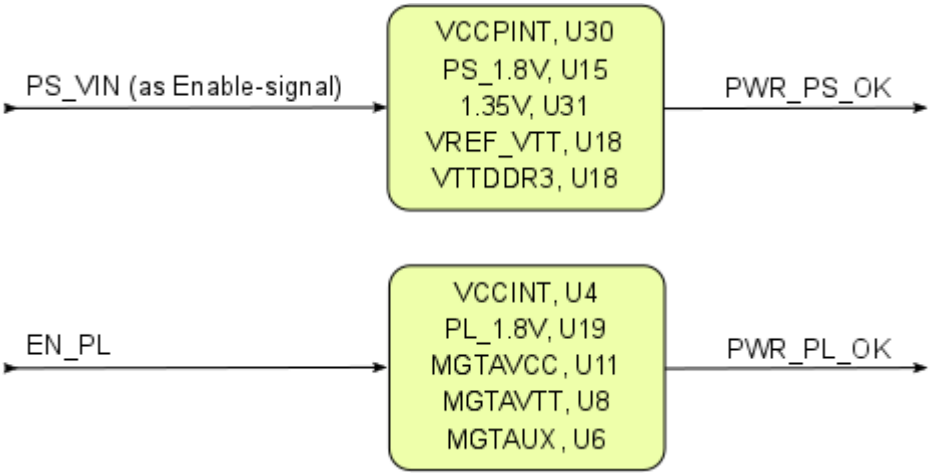


**Figure 4**: Power-On Sequence

The Enable-Signal 'EN_PL' is permanently logic high in standard SC-CPLD firmware. The "Power Good"-signals 'PWR_PS_OK' and 'PWR_PL_OK' (latter low-active, extern pull-up needed) are available B2B-connector J2 (pins J2-139, J2-135) and on the SC-CPLD.

## 6.4 Voltage Monitor Circuit

The voltages 'VCCPINT' and 'PS_1.8V' are monitored by the voltage monitor circuit U41, which generates the POR_B reset signal at Power-On. A manual reset is also possible by driving the MR-pin (available on J2-131 or SC-CPLD) to GND. Leave this pin unconnected or connect to VDD (PS_1.8V) when unused.

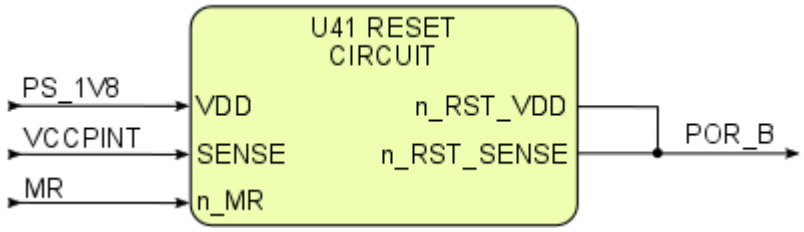


**Figure 5**: Voltage monitor circuit.

## 7.4 Connector Speed Ratings

The connector speed rating depends on the stacking height:

| Stacking height | Speed rating |
|---|---|
| 4 mm, Single-Ended | 13GHz/26Gbps |
| 4 mm, Differential | 13.5GHz/27Gbps |
| 5 mm, Single-Ended | 13.5GHz/27Gbps |
| 5 mm, Differential | 20GHz/40 Gbps |

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

## 7.5 Manufacturer Documentation

# 9 Technical Specification

## 9.1 Absolute Maximum Ratings

| Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|
| PL_VIN | -0.3 | 5 | V | TI TPS720 data sheet |
| PS_VIN | -0.3 | 7 | V | TI TPS82085 data sheet |
| PS_3.3V | 3.135 | 3.465 | V | 3.3V nominal ± 5%<br>**Attention**: PS_3.3V is directly connected to numerous on-board peripherals as supply and I/O voltage. |
| VBAT supply voltage | -1 | 6.0 | V | ISL12020MIRZ data sheet |
| PL IO bank supply voltage for HR I/O banks (VCCO) | -0.5 | 3.6 | V | - |
| PL IO bank supply voltage for HP I/O banks (VCCO) | -0.5 | 2.0 | V | - |
| I/O input voltage for HR I/O banks | -0.4 | VCCO_X +0.55 | V | - |
| I/O input voltage for HP I/O banks | -0.55 | VCCO_X +0.55 | V | - |
| GT receiver (RXP/RXN) and transmitter (TXP/TXN) | -0.5 | 1.26 | V | - |
| Voltage on module JTAG pins | -0.3 | 3.6 | V | MachX02 Family data sheet |
| Storage temperature | -40 | +85 | °C | Limits of ISL12020MIRZ RTC chp. |
| Storage temperature without the ISL12020MIRZ | -55 | +100 | °C | Limits of DDR3 memory chips. |

**Table 21:** Module absolute maximum ratings.

Assembly variants for higher storage temperature range are available on request.

## 9.2 Recommended Operating Conditions

| Parameter | Min | Max | Units | Notes | Reference Document |
|---|---|---|---|---|---|
| PL_VIN | 3.3 | 4.5 | V | - | TI TPS720 data sheet |
| PS_VIN | 3.3 | 6.0 | V | - | TI TPS82085 data sheet |
| PS_3.3V | 3.135 | 3.465 | V | - | 3.3V nominal ± 5% |
| VBAT_IN supply voltage | 2.7 | 5.5 | V | - | ISL12020MIRZ data sheet |

| Parameter | Min | Max | Units | Notes | Reference Document |
|---|---|---|---|---|---|
| PL I/O bank supply voltage for HR I/O banks (VCCO) | 1.14 | 3.465 | V | - | Xilinx datasheet DS191 |
| PL I/O bank supply voltage for HP I/O banks (VCCO) | 1.14 | 1.89 | V | - | Xilinx datasheet DS191 |
| I/O input voltage for HR I/O banks | -0.20 | VCCO_X+ 0.20 | V | - | Xilinx datasheet DS191 |
| I/O input voltage for HP I/O banks | -0.20 | VCCO_X+ 0.20 | V | - | Xilinx datasheet DS191 |
| GT receiver (RXP/RXN) and transmitter (TXP/TXN) | (*) | (*) | V | (*) Check datasheet | Xilinx datasheet DS191 |
| Voltage on Module JTAG pins | 3.135 | 3.6 | V | JTAG signals forwarded to Zynq module config bank 0 | MachX02 Family Data Sheet |

**Table 22:** Module recommended operating conditions.

Please check Xilinx datasheet DS191 (for XC7Z030) for complete list of absolute maximum and recommended operating ratings.

## 9.3 Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

Extended grade: 0°C to +85°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

## 9.4 Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.

# 10 Revision History

## 10.1 Hardware Revision History

| Date | Revision | Notes | Link to PCN | Documentation Link |
|---|---|---|---|---|
| 2016-10-11 | 02 | • First Production release<br>• Refer to Changes list in Schematic for further details in changes to REV01 | - | TE0745-02 |
| 2016-04-18 | 01 | • Prototypes | - | TE0745-01 |

**Table 23:** Module hardware revision history.

Hardware revision number is written on the PCB board together with the module model number separated by the dash.


**Figure 7**: TE0745 module revision number.

## 10.2 Document Change History

| Date | Revision | Contributors | Description |
|---|---|---|---|
| 2017-11-14 | V.80 | John Hartfiel | • Update B2B Section |
| 2017-11-13 | V.79 | Ali Naseri, Jan Kumann, John Hartfiel | • First TRM release |

**Table 24:** Document change history.

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