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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	MCU, FPGA
Core Processor	ARM® Cortex®-A9
Co-Processor	Zynq-7000 (Z-7030)
Speed	-
Flash Size	64MB
RAM Size	1GB
Connector Type	-
Size / Dimension	2.99" x 2.05" (76mm x 52mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0745-02-30-2ia

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2 Overview

Refer to https://wiki.trenz-electronic.de/display/PD/TE0745+TRM for online version of this manual and the rest of the available documentation.
The Trenz Electronic TE0745 is an industrial-grade module integrating a Xilinx Zynq SoC (XC7Z-030, XC7Z-035 or XC7Z-045), 1 GByte DDR3/L SDRAM, 32 MByte SPI Flash memory for configuration and operation and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking strips.

2.1 Key Features

- Industrial grade Xilinx Zynq SoC (XCZ7030, XC7Z035, XC7Z045)
  - Dual-core ARM Cortex-A9 MPCore™ with CoreSight™
  - 250 FPGA PL I/Os (120 LVDS pairs possible)
  - 17 PS MIOs on B2B connector available
- 16-bit wide 1GB DDR3L SDRAM
- 32 MByte QSPI Flash memory
- 4 or 8 GTX transceiver lanes (XC7Z030 variant has 4)
- Gigabit Ethernet transceiver PHY
- EEPROM for storing Ethernet MAC Address
- Hi-speed USB 2.0 ULPI transceiver with full OTG support
- Programmable quad clock generator
- Temperature compensated RTC (real-time clock)
- Plug-on module with 3 × 160-pin high-speed hermaphroditic strips
- On-board high-efficiency DC-DC converters
- System management
- eFUSE bit-stream encryption
- AES bit-stream encryption
- User LED
- Evenly-spread supply pins for good signal integrity
- Rugged for shock and high vibration

Additional assembly options are available for cost or performance optimization upon request.

Storage Device Name	Content	Notes
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-
SPI Flash main array	Not programmed	-
eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-
Si5338 OTP NVM	Not programmed	OTP not re-programmable after delivery from factory

Table 1: Initial delivery state.

Table 4: MGT reference clock sources.

[1] **Note:** MGT bank 111 not available at XC7Z030 Zynq SoC.

3.3 JTAG Interface

JTAG interface access is provided through the SoC's PS configuration bank 0 and is available on B2B connector J1.

JTAG Signal	B2B Connector Pin
TCK	J1-143
TDI	J1-142
TDO	J1-145
TMS	J1-144

Table 5: JTAG interface signals.

JTAG_EN pin 148 in B2B connector J1 should be kept low or grounded for normal operation!

3.4 System Controller I/O's

Following special purpose pins are connected to System Controller CPLD:

Pin Name	Mode	Function	B2B Connector Pin	Default Configuration
JTAG_EN	Input	JTAG select	J1-148	During normal operating mode the JTAG_EN pin should be in the low state for JTAG signals to be forwarded to the Zynq SoC. If JTAG_EN pin is set to high or left open the JTAG signals are forwarded to the System Controller CPLD.
RST_IN_N	Input	Reset	J2-131	Low-active Power-On reset pin, controls POR_B-signal (bank 500, pin C23) of Zynq chip.
PS_SRST	Input	Reset	J2-152	Low-active PS system-reset pin of Zynq chip.
BOOTMODE	Output	Boot mode	J2-133	Control line which sets in conjunction with signal 'BOOTMODE1' (B2B-pin J2-133) the boot source of the Zynq chip. See section "Boot Modes". Permanent logic high in standard SC-CPLD firmware.
PWR_PL_OK	Input	Power good	J2-135	Indicates stable state of PL supply voltage (low-active) after power-up sequence.
PWR_PS_OK	Input	Power good	J2-139	Indicates stable state of PS supply voltage (low-active) after power-up sequence.
EN_PL	Output	Enable signal	-	Low active Enable-signal for activating PL supply voltage. Permanent logic high in standard SC-CPLD firmware.

The schematics for the USB connector and required components is different depending on the USB usage. USB standard A or B connectors can be used for Host or Device modes. A Mini USB connector can be used for USB Device mode. A USB Micro connector can be used for Device mode, OTG Mode or Host Mode.

3.8 I2C Interface

The I^2C interface on B2B connector J2 has PS_3.3V as reference voltage and is connected to the Zynq SoC via voltage level translating (3.3V ↔ 1.8V) I^2C bus repeater (U17).:

B2B pin	Signal Schematic Name	Notes
J2-119	I2C_33_SCL	3.3V reference voltage
J2-121	I2C_33_SDA	3.3V reference voltage

Table 10: Pin assignment of the B2B I^2C interface.

The on-module I^2C interface works with reference voltage 1.8V:

PS Bank 500	Signal Schematic Name	Notes
MIO 10	I2C_SCL	1.8V reference voltage
MIO 11	I2C_SDA	1.8V reference voltage

Table 11: MIO-pin assignment of the on-module I^2C interface.

Except the on-module RTC (U24), all other on-module I^2C slave devices are operating with the reference voltage PS_1.8V.

I^2C addresses for on-module devices are listed in the table below:

I2C Device	I2C Address	Notes
Zynq chip U1, bank 500 (PS MIO), pins MIO10 (SCL), MIO11 (SDA)	User programmable.	Configured as I^2C by default.
Quad programmable PLL clock generator U16: pins 12 (SCL), 19 (SDA)	0x70	-
MAC Address EEPROM U23, pins 1 (SCL), 3 (SDA)	0x53	-
SC CPLD U2, bank 2, pins 16 (SDA), 17 (SCL)	User programmable.	-
RTC, U24	0x6F	-
RTC RAM, U24	0x57	-

Table 12: Module's I^2C-interfaces overview.

4 Boot Process

TE0745 module supports different boot modes which are configurable by the control line 'BOOTMODE' and 'BOOTMODE_1'. The line 'BOOTMODE' is available on B2B connector pin J2-133, the line 'BOOTMODE_1' is connected to the System Controller CPLD on bank 1, pin 21 (permanent logic high in standard SC-CPLD firmware).The boot mode selection will be set by the Zynq's PS MIO pins MIO3...MIO5.

Following table describes how to set the control lines to configure the boot mode:

Boot Mode	MIO5 (BOOTMODE_1), SC CPLD	MIO4 (BOOTMODE), J2-133	Note
JTAG	0	0	-
QSPI Flash Memory	1	0	standard mode in current configuration.
SD-Card	1	1	SD-Card on base board necessary.

Table 13: Selectable boot modes.

In delivery state of the SoM the boot mode depends on the configured SC-CPLD firmware. Basically MIO5 is set to 1 and JTAG is in cascade.

5.6 RTC - Real Time Clock

An temperature compensated Intersil ISL12020M is used as Real Time Clock (U24). Battery voltage must be supplied to the clock from the base board via pin 'VBAT_IN' (J1-146). Battery backed registers can be accessed over I^2C bus at slave address 0x6F. General purpose RAM of the RTC can be accessed at I^2C slave address 0x57. RTC IC is supported by Linux so it can be used as hwclock device. The interrupt line 'RTC_INT' of the RTC is connected to System Controller CPLD bank 3 pin 4.

5.7 Programmable PLL Clock (Phase-Locked Loop)

There is a Silicon Labs I^2C programmable quad PLL clock generator Si5338A (U16) on-board. It's output frequencies can be programmed by using the I^2C-bus with address 0x70.

A 25 MHz (U21) oscillator is connected to pin 3 (IN3) and is used to generate the output clocks.

Once running, the frequency and other parameters can be changed by programming the device using the I^2C-bus connected between the Zynq module (master) and reference clock signal generator (slave).

Si5338A Pin	Signal Name / Description	Connected To	Direction	Note
IN1	CLKIN_P	B2B, J3-76	Input	Reference input clock from base board.
IN2	CLKIN_N	B2B, J3-74	Input	
IN3	Reference input clock.	Oscillator U21, pin 3	Input	25.000000 MHz oscillator, Si8008BI.
IN4	-	GND	Input	I^2C slave device address LSB (0x70 default address).
IN5	-	Not connected.	Input	Not used.
IN6	-	GND	Input	Not used.
CLK0A	MGT_CLK1_P	Zynq Soc U1, pin U6	Output	MGT bank 112 reference clock.
CLK0B	MGT_CLK1_N	Zynq Soc U1, pin U5	Output	
CLK1A	CLK1_P	B2B, J3-80	Output	Reference clock output to base board.
CLK1B	CLK1_N	B2B, J3-82	Output	
CLK2A	CLK2_P	B2B, J3-86	Output	Reference clock output to base board.
CLK2B	CLK2_P	B2B, J3-88	Output	
CLK3A	MGT_CLK3_P	Zynq Soc U1, pin AA6	Output	MGT bank 111 reference clock.
CLK3B	MGT_CLK3_N	Zynq Soc U1, pin AA6	Output	

Table 14: Programmable quad PLL clock generator inputs and outputs.

5.8 Oscillators

The SoC module has following reference clocking signals provided by external baseboard sources and on-board oscillators:

Clock Source	Schematic Name	Frequency	Clock Input Destination
SiTime SiT8008BI oscillator, U21	-	25.000000 MHz	Quad PLL clock generator U16, pin 3
SiTime SiT8008BI oscillator, U12	PS_CLK	33.333333 MHz	Bank 500 (MIO0 bank), pin B24
SiTime SiT8008BI oscillator, U33	OTG-RCLK	52.000000 MHz	USB 2.0 transceiver PHY U32, pin 26
SiTime SiT8008BI oscillator, U9	ETH_CLKIN	25.000000 MHz	Gigabit Ethernet PHY U7, pin 34

Table 15: Clock sources overview.

5.9 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Green	System Controller CPLD, bank 3, pin 5	System main status LED, blinking indicates system activity
D2	Red	Zynq chip (U1), bank 0 (config bank), 'DONE' (pin W9)	Reflects inverted DONE signal. ON when FPGA is not configured, OFF as soon as PL is configured. This LED remains OFF if System Controller CPLD can not power up the PL supply voltage.

Table 16: LEDs of the module.

6 Power and Power-On Sequence

6.1 Power Consumption

The maximum power consumption of a module mainly depends on the design which is running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input Pin	Typical Current
PL_VIN	TBD*
PS_VIN	TBD*
PS_3.3V	TBD*

Table 17: Typical power consumption. *to be determined soon with reference design setup.

Power supply with minimum current capability of 3A for system startup is recommended.

For the lowest power consumption and highest efficiency of on board DC-DC regulators it is recommended to powering the module from one single 3.3V supply. All input power supplies have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

The on-board voltages of the TE0745 SoC module will be powered-up in order of a determined sequence after the external voltages 'PL_VIN', 'PS_VIN' and 'PS_3.3V' are available. All those power-rails can be powered up, with 3.3V power sources, also shared.

> To avoid any damage to the module, check for stabilized on-board voltages should be carried out(i.e. power good and enable signals) before powering up any SoC's I/O bank voltages VCCO_x. All I/Os should be tri-stated during power-on sequence.

Core voltages and main supply voltages have to reach stable state and their "Power Good"-signals have to be asserted before other voltages like PL bank's I/O voltages can be powered up.

It is important that all baseboard I/Os are tri-stated at power-on until the "Power Good"-signals 'PWR_PS_OK' (J2-139) and 'PWR_PL_OK' (J2-135) are high, meaning that all on-module voltages have become stable and module is properly powered up.

6.2 Power Distribution Dependencies

There are following dependencies how the initial voltages of the power rails on the B2B connectors are distributed to the on-board DCDC converters, which power up further DCDC converters and the particular on-board voltages:

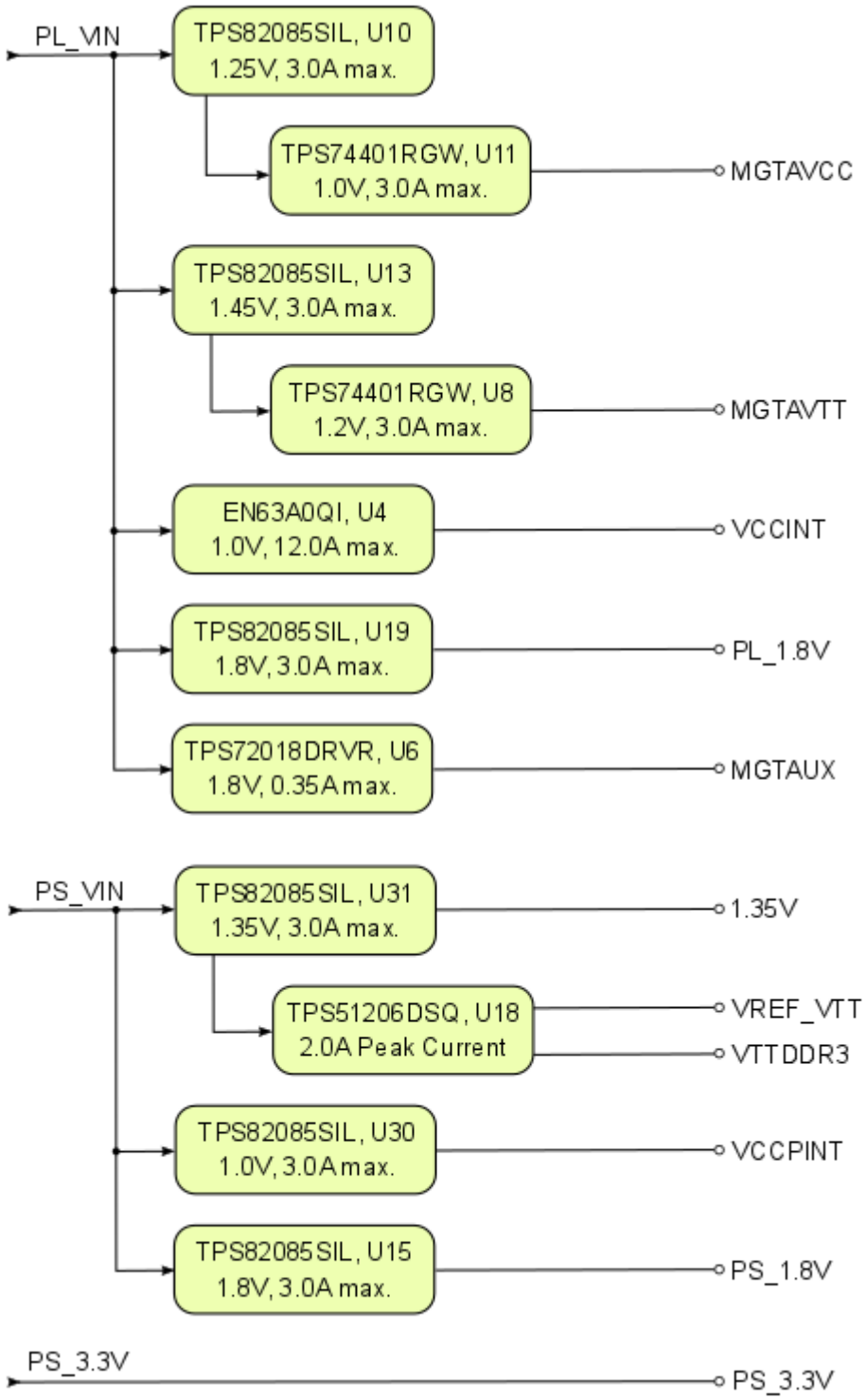

Figure 3: Power Distribution Diagram

See Xilinx data sheet DS191 for additional information. User should also check related base board documentation when intending base board design for TE0745 module.

⚠ Current rating of Samtec Razor Beam LP Terminal/Socket Strip ST5/SS5 B2B connectors is 1.5 A per pin (1 pin powered per row).

6.3 Power-On Sequence Diagram

The TE0745 SoM meets the recommended criteria to power up the Xilinx Zynq MPSoC properly by keeping a specific sequence of enabling the on-board DCDC converters dedicated to the particular functional units of the Zynq chip and powering up the on-board voltages.

Following diagram clarifies the sequence of enabling the particular on-board voltages, which will power-up in descending order as listed in the blocks of the diagram:

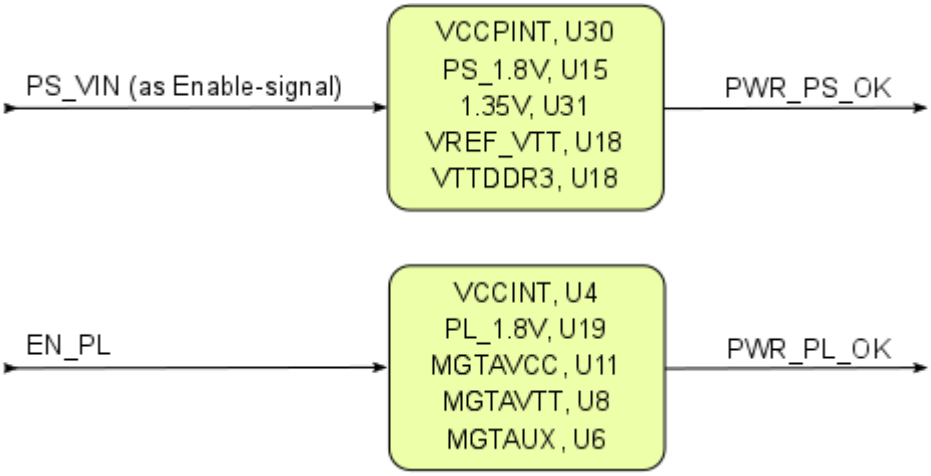

Figure 4: Power-On Sequence

The Enable-Signal 'EN_PL' is permanently logic high in standard SC-CPLD firmware. The "Power Good"-signals 'PWR_PS_OK' and 'PWR_PL_OK' (latter low-active, extern pull-up needed) are available B2B-connector J2 (pins J2-139, J2-135) and on the SC-CPLD.

6.4 Voltage Monitor Circuit

The voltages 'VCCPINT' and 'PS_1.8V' are monitored by the voltage monitor circuit U41, which generates the POR_B reset signal at Power-On. A manual reset is also possible by driving the MR-pin (available on J2-131 or SC-CPLD) to GND. Leave this pin unconnected or connect to VDD (PS_1.8V) when unused.

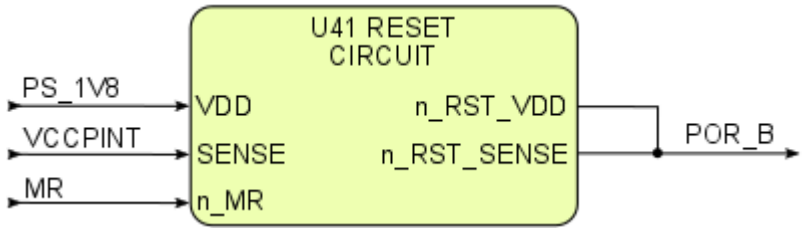

Figure 5: Voltage monitor circuit.

7.4 Connector Speed Ratings

The connector speed rating depends on the stacking height:

Stacking height	Speed rating
4 mm, Single-Ended	13GHz/26Gbps
4 mm, Differential	13.5GHz/27Gbps
5 mm, Single-Ended	13.5GHz/27Gbps
5 mm, Differential	20GHz/40 Gbps

The SS5/ST5 series board-to-board spacing is currently available in 4mm (0.157"), 4.5mm (0.177") and 5mm (0.197") stack heights.

The data in the reports is applicable only to the 4mm and 5mm board-to-board mated connector stack height.

7.5 Manufacturer Documentation

8 Variants Currently In Production

Module Variant	Zynq SoC	SoC Junction Temperature	Operating Temperature Range
TE0745-02-30-1I	XC7Z030-1FBG676I	–40°C to +100°C	Industrial
TE0745-02-35-1C	XC7Z035-1FBG676C	0°C to +85°C	Commercial
TE0745-02-45-1C	XC7Z045-1FBG676C	0°C to +85°C	Commercial
TE0745-02-45-2I	XC7Z045-2FBG676I	–40°C to +100°C	Industrial

Table 20: Module variants.

9 Technical Specification

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
PL_VIN	-0.3	5	V	TI TPS720 data sheet
PS_VIN	-0.3	7	V	TI TPS82085 data sheet
PS_3.3V	3.135	3.465	V	3.3V nominal ± 5% **Attention**: PS_3.3V is directly connected to numerous on-board peripherals as supply and I/O voltage.
VBAT supply voltage	-1	6.0	V	ISL12020MIRZ data sheet
PL IO bank supply voltage for HR I/O banks (VCCO)	-0.5	3.6	V	-
PL IO bank supply voltage for HP I/O banks (VCCO)	-0.5	2.0	V	-
I/O input voltage for HR I/O banks	-0.4	VCCO_X +0.55	V	-
I/O input voltage for HP I/O banks	-0.55	VCCO_X +0.55	V	-
GT receiver (RXP/RXN) and transmitter (TXP/TXN)	-0.5	1.26	V	-
Voltage on module JTAG pins	-0.3	3.6	V	MachX02 Family data sheet
Storage temperature	-40	+85	°C	Limits of ISL12020MIRZ RTC chp.
Storage temperature without the ISL12020MIRZ	-55	+100	°C	Limits of DDR3 memory chips.

Table 21: Module absolute maximum ratings.

Assembly variants for higher storage temperature range are available on request.

9.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Notes	Reference Document
PL_VIN	3.3	4.5	V	-	TI TPS720 data sheet
PS_VIN	3.3	6.0	V	-	TI TPS82085 data sheet
PS_3.3V	3.135	3.465	V	-	3.3V nominal ± 5%
VBAT_IN supply voltage	2.7	5.5	V	-	ISL12020MIRZ data sheet

Parameter	Min	Max	Units	Notes	Reference Document
PL I/O bank supply voltage for HR I/O banks (VCCO)	1.14	3.465	V	-	Xilinx datasheet DS191
PL I/O bank supply voltage for HP I/O banks (VCCO)	1.14	1.89	V	-	Xilinx datasheet DS191
I/O input voltage for HR I/O banks	-0.20	VCCO_X+ 0.20	V	-	Xilinx datasheet DS191
I/O input voltage for HP I/O banks	-0.20	VCCO_X+ 0.20	V	-	Xilinx datasheet DS191
GT receiver (RXP/RXN) and transmitter (TXP/TXN)	(*)	(*)	V	(*) Check datasheet	Xilinx datasheet DS191
Voltage on Module JTAG pins	3.135	3.6	V	JTAG signals forwarded to Zynq module config bank 0	MachX02 Family Data Sheet

Table 22: Module recommended operating conditions.

Please check Xilinx datasheet DS191 (for XC7Z030) for complete list of absolute maximum and recommended operating ratings.

9.3 Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

Extended grade: 0°C to +85°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

9.4 Physical Dimensions

- Module size: 52 mm × 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.

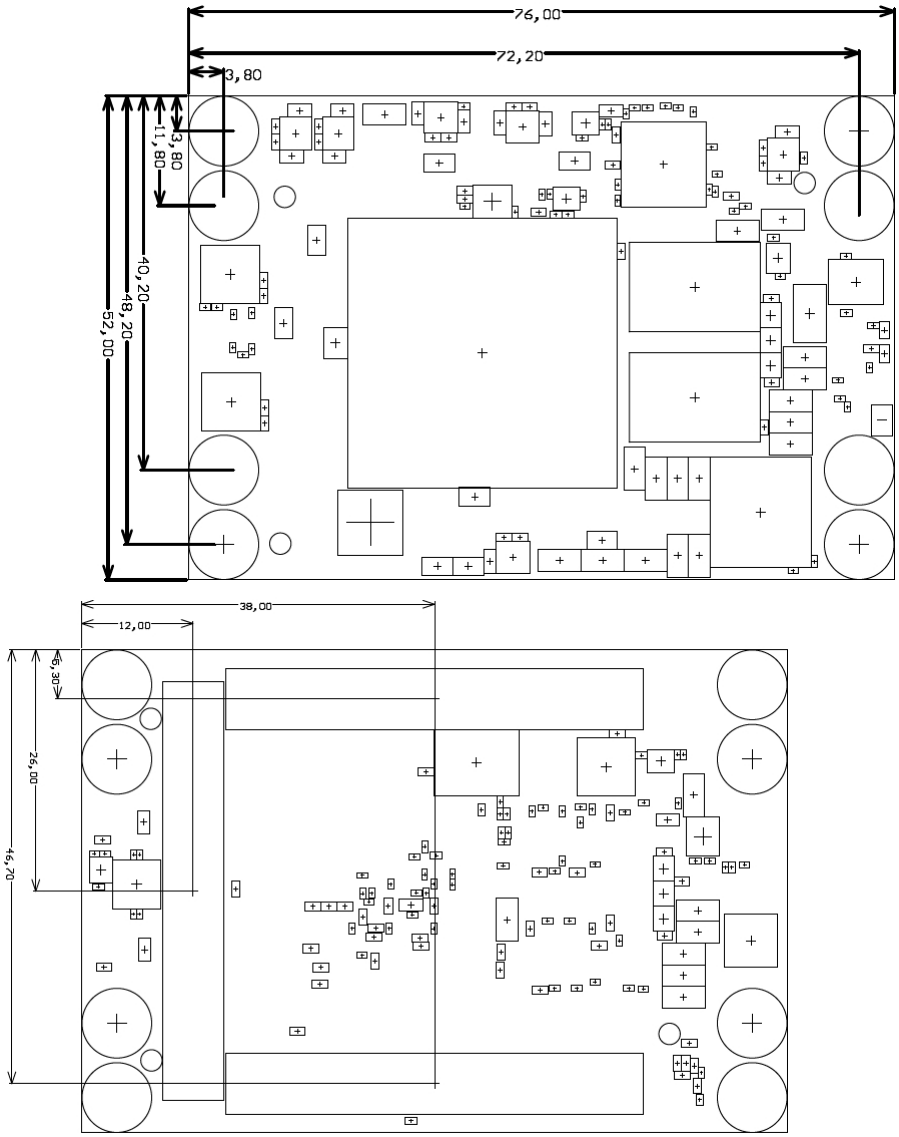

Figure 6: Physical dimensions of the TE0745 SoC module.

10 Revision History

10.1 Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
2016-10-11	02	• First Production release • Refer to Changes list in Schematic for further details in changes to REV01	-	TE0745-02
2016-04-18	01	• Prototypes	-	TE0745-01

Table 23: Module hardware revision history.

Hardware revision number is written on the PCB board together with the module model number separated by the dash.

Figure 7: TE0745 module revision number.

10.2 Document Change History

Date	Revision	Contributors	Description
2017-11-14	V.80	John Hartfiel	• Update B2B Section
2017-11-13	V.79	Ali Naseri, Jan Kumann, John Hartfiel	• First TRM release

Table 24: Document change history.

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11.6 REACH, RoHS and WEEE

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Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

02.09.2017