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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s005c6t6tr

4 Product overview

The following section intends to give an overview of the basic features of the STM8S005C6/K6 value line functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.14.1 UART2

Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

LIN master mode

- Emission: generates 13-bit synch. break frame
- Reception: detects 11-bit break frame

LIN slave mode

- Autonomous header handling - one-single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ± 15%
- Synch. delimiter checking
- 11-bit LIN synch. break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.14.2 SPI

- Maximum speed: 8 Mbit/s ($f_{MASTER}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

4.14.3 I^2C

- I^2C master features
  - Clock generation
  - Start and stop generation
- I^2C slave features
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50CC	CLK	CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CD		CLK_SWIMCCR	SWIM clock control register	0bXXXX XXX0
0x00 50CE to 0x00 50D0	Reserved area (3 bytes)			
0x00 50D1	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D2		WWDG_WR	WWDR window register	0x7F
0x00 50D3 to 0x00 50DF	Reserved area (13 bytes)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX(2)
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR1	AWU control/status register 1	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 50FF	Reserved area (12 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205		SPI_CRCPR	SPI CRC polynomial register	0x07
0x00 5206		SPI_RXCRCR	SPI Rx CRC register	0xFF
0x00 5207		SPI_TXCRCR	SPI Tx CRC register	0xFF
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I^2C	I2C_CR1	I^2C control register 1	0x00
0x00 5211		I2C_CR2	I^2C control register 2	0x00
0x00 5212		I2C_FREQR	I^2C frequency register	0x00
0x00 5213		I2C_OARL	I^2C own address register low	0x00
0x00 5214		I2C_OARH	I^2C own address register high	0x00
0x00 5215		Reserved		

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5302		TIM2_SR1	TIM2 status register 1	0x00
0x00 5303		TIM2_SR2	TIM2 status register 2	0x00
0x00 5304		TIM2_EGR	TIM2 event generation register	0x00
0x00 5305		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5306		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5307		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 5308		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 5309		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530A		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530B		TIM2_CNTRL	TIM2 counter low	0x00
00 530C0x		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530D		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 530E		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 530F		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5310		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5311		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5312		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5313		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5314		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5315 to 0x00 531F	Reserved area (11 bytes)			
0x00 5320	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5321		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5322		TIM3_SR1	TIM3 status register 1	0x00
0x00 5323		TIM3_SR2	TIM3 status register 2	0x00
0x00 5324		TIM3_EGR	TIM3 event generation register	0x00
0x00 5325		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5326		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 5327		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 5328		TIM3_CNTRH	TIM3 counter high	0x00
0x00 5329		TIM3_CNTRL	TIM3 counter low	0x00
0x00 532A		TIM3_PSCR	TIM3 prescaler register	0x00

1. Depends on the previous reset source.
2. Write only register.

Table 9. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register Label	Register Name	Reset Status
0x00 7F00	CPU(1)	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x17
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC	ITC_SPR1	Interrupt software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			

Table 12. Option byte description (continued)

Option byte no.	Description
OPT5	**HSECNT[7:0]:** *HSE crystal oscillator stabilization time* This configures the stabilization time. 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles
OPT6	Reserved
OPT7	Reserved
OPTBL	**BL[7:0]** *Bootloader option byte* For STM8S products, this option is checked by the boot ROM code after reset. Depending on the content of addresses 0x487E, 0x487F, and 0x8000 (reset vector), the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 (STM8L/S bootloader manual) for more details. For STM8L products, the bootloader option bytes are on addresses 0xXXXX and 0xXXXX+1 (2 bytes). These option bytes control whether the bootloader is active or not. For more details, refer to the UM0560 (STM8L/S bootloader manual) for more details.

Table 13. Description of alternate function remapping bits [7:0] of OPT2

Option byte number	Description(1)
OPT2	**AFR7***Alternate function remapping option 7* 0: AFR7 remapping option inactive: default alternate function(2) 1: Port D4 alternate function = BEEP **AFR6** *Alternate function remapping option 6* 0: AFR6 remapping option inactive: default alternate function(2) 1: Port B5 alternate function = I^2C_SDA; port B4 alternate function = I^2C_SCL **AFR5** *Alternate function remapping option 5* 0: AFR5 remapping option inactive: default alternate function(2) 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N **AFR4** *Alternate function remapping option 4* 0: AFR4 remapping option inactive: default alternate function(2) 1: Port D alternate function = TIM1_CH4 **AFR3** *Alternate function remapping option 3* 0: AFR3 remapping option inactive: default alternate function(2) 1: Port D0 alternate function = TIM1_BKIN **AFR2** *Alternate function remapping option 2* 0: AFR2 remapping option inactive: default alternate function(2) 1: Port D0 alternate function = CLK_CCO Note: AFR2 option has priority over AFR3 if both are activated **AFR1** *Alternate function remapping option 1* 0: AFR1 remapping option inactive: default alternate function(2) 1: Port A3 alternate function = TIM3_CH1; port D2 alternate function TIM2_CH3 **AFR0** *Alternate function remapping option 0* 0: AFR0 remapping option inactive: default alternate function(2) 1: Port D3 alternate function = ADC_ETR

1. Do not use more than one remapping option in the same port.
2. Refer to the pinout description.

Figure 9. f_{CPUmax} versus V_{DD}

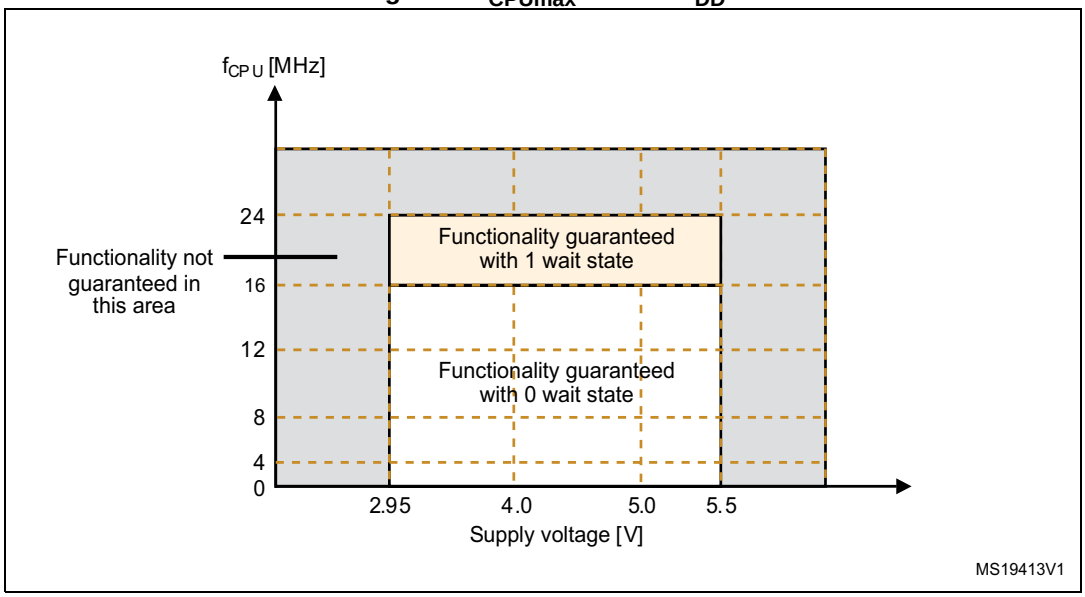


Table 18. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2(1)	-	∞	µs/V
	V_{DD} fall time rate	-	2(1)	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7(1)	ms
V_{IT+}	Power-on reset threshold(2)	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.73	2.88	V
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Guaranteed by design, not tested in production.
2. If V_{DD} is below 2.95 V, the code execution is guaranteed above the V_{IT-} and $_{VIT+}$ thresholds. RAM content is kept. The EEPROM programming sequence must not be initiated.

Table 19. Total current consumption with code execution in run mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max (1)	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	3.2	-	mA
			HSE user ext. clock (16 MHz)	2.6	3.2	
			HSI RC osc. (16 MHz)	2.5	3.2	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	1.6	2.2	
			HSI RC osc. (16 MHz)	1.3	2.0	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.55	-	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	7.7	-	
			HSE user ext. clock (16 MHz)	7.0	8.0	
			HSI RC osc.(16 MHz)	7.0	8.0	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	1.5	-	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.35	2.0	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.75	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.6	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Total current consumption in wait mode

Table 21. Total current consumption in wait mode at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	2.15	-	mA
			HSE user ext. clock (16 MHz)	1.55	2.0	
			HSI RC osc. (16 MHz)	1.5	1.9	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.3	-	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.7	-	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.5	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Table 22. Total current consumption in wait mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(WFI)}$	Supply current in wait mode	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.75	-	mA
			HSE user ext. clock (16 MHz)	1.55	2.0	
			HSI RC osc. (16 MHz)	1.5	1.9	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	1.3	-	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)(2)	0.7	-	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	LSI RC osc. (128 kHz)	0.5	-	

1. Data based on characterization results, not tested in production.
2. Default clock configuration measured with all peripherals off.

Total current consumption in active halt mode

Table 23. Total current consumption in active halt mode at V_{DD} = 5 V, T_A -40 to 85° C

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source			
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal oscillator (16 MHz)	1080	-	µA
				LSI RC oscillator (128 kHz)	200	320	
			Power-down mode	HSE crystal oscillator (16 MHz)	1030	-	
				LSI RC oscillator (128 kHz)	140	270	
		Off	Operating mode	LSI RC oscillator (128 kHz)	68	120	
			Power-down mode		12	60	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 24. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85° C (1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source			
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	680	-	µA
				LSI RC osc. (128 kHz)	200	320	
			Power-down mode	HSE crystal osc. (16 MHz)	630	-	
				LSI RC osc. (128 kHz)	140	270	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	120	
			Power-down mode		10	60	

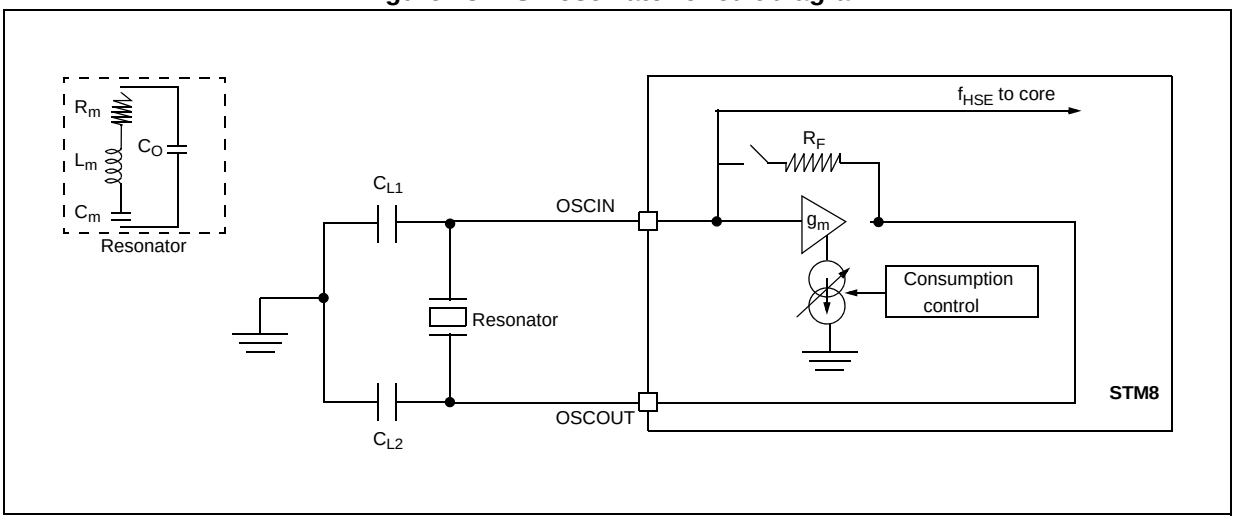
1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
C(1)	Recommended load capacitance (2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.6 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 24 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 36. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5 V	-0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	V
V_{hys}	Hysteresis(1)		-	700	-	mV
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	30	55	80	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	35(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	ns
I_{lkg}	Input leakage current, analog and digital	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1(3)	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±250 (3)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O	Injection current ±4 mA	-	-	±1(3)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

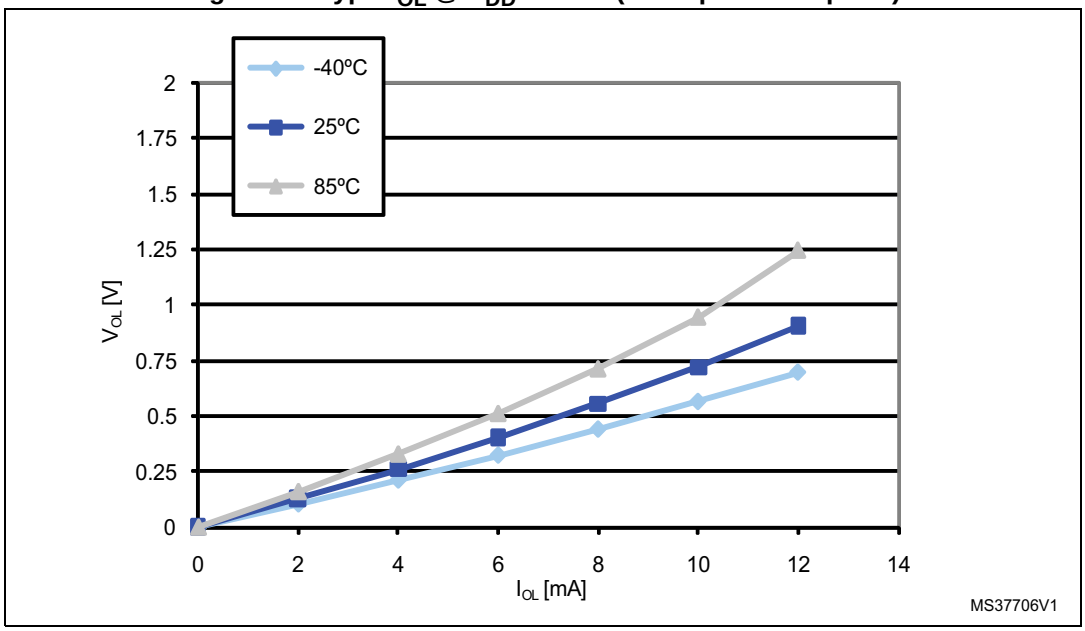
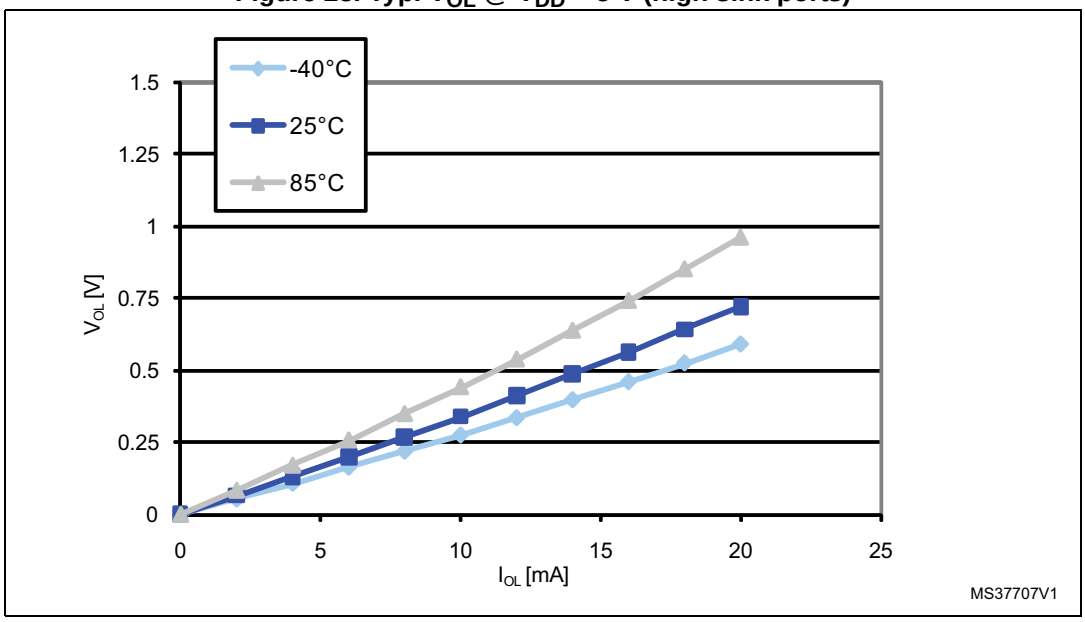


Figure 28. Typ. V_{OL} @ V_{DD} = 5 V (high sink ports)



9.3.7 Reset pin characteristics

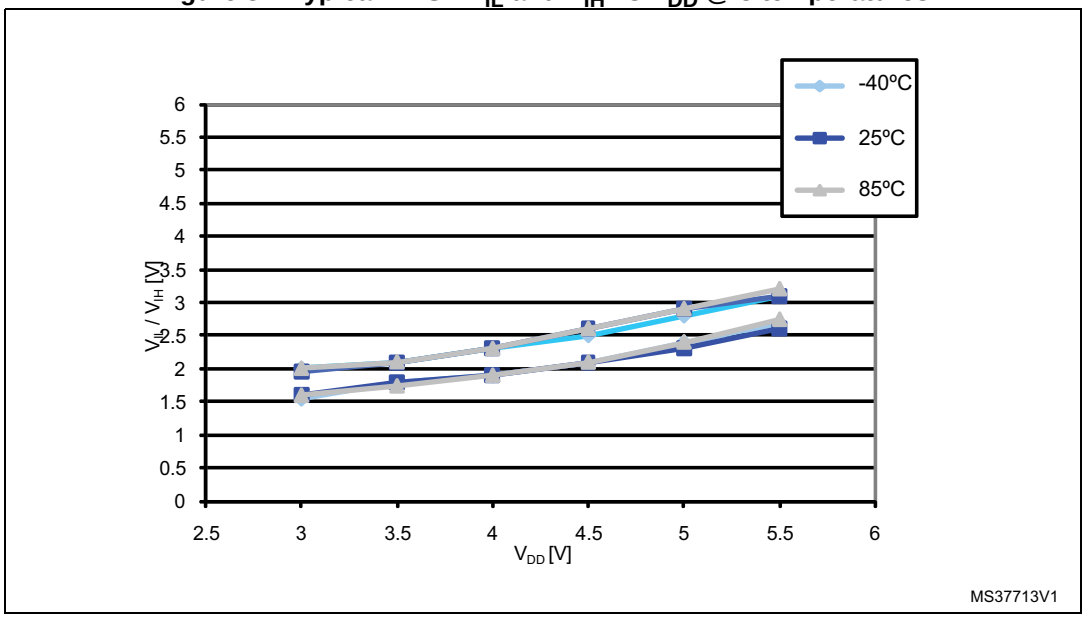
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 40. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	-0.3 V	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	0.7 x V_{DD}	-	V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage (1)	I_{OL}= 2 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor (2)	-	30	55	80	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse (3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST Input not filtered pulse (3)	-	500	-	-	ns
$t_{OP(NRST)}$	NRST output pulse (1)	-	15	-	-	µs

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
3. Data guaranteed by design, not tested in production.

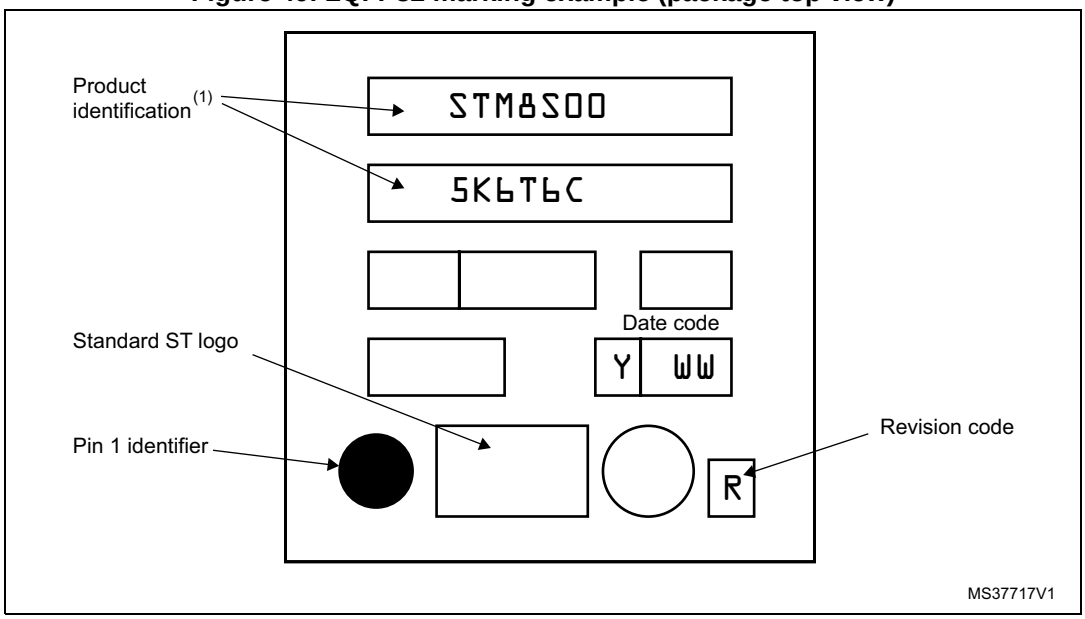
Figure 34. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 3 temperatures



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 49. LQFP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

13 Revision history

Table 53. Document revision history

Date	Revision	Changes
14-Oct-2011	1	Initial release.
09-Jan-2012	2	Updated: – t_{RET} in *Table 35: Flash program memory/data EEPROM memory*, – R_{PU} in *Table 40: NRST pin characteristics* and *Table 36: I/O static characteristics*, – the notes related to V_{CAP} in *Section 9.3: Operating conditions*.
13-Jun-2012	3	Updated the temperature condition for factory calibrated ACC_{HSI} in *Table 32: HSI oscillator characteristics*. Changed SCK input to SCK output in *Figure 40: SPI timing diagram - master mode(1)*.
26-Mar-2015	4	Updated: – the buffer size in *Section 4.13: Analog-to-digital converter (ADC1)*, – the disclaimer. Added: – the note to Power-on reset threshold in *Table 18: Operating conditions at power-up/power-down*, – *Figure 46: LQFP48 marking example (package top view)*, – *Figure 49: LQFP32 marking example (package top view)*.