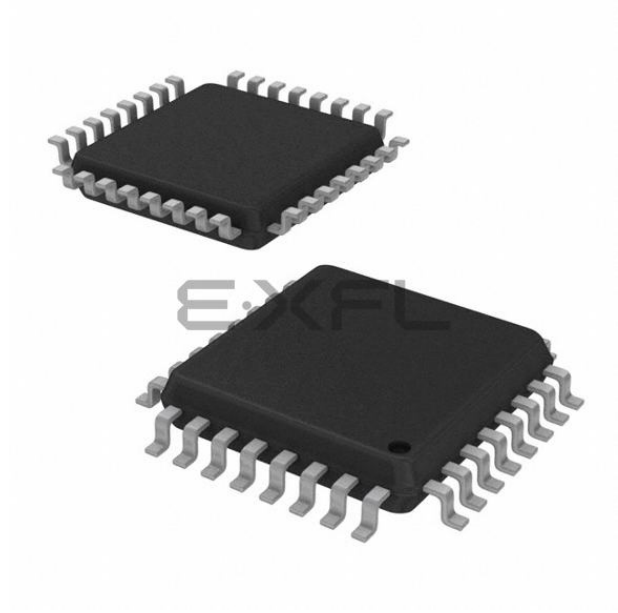


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

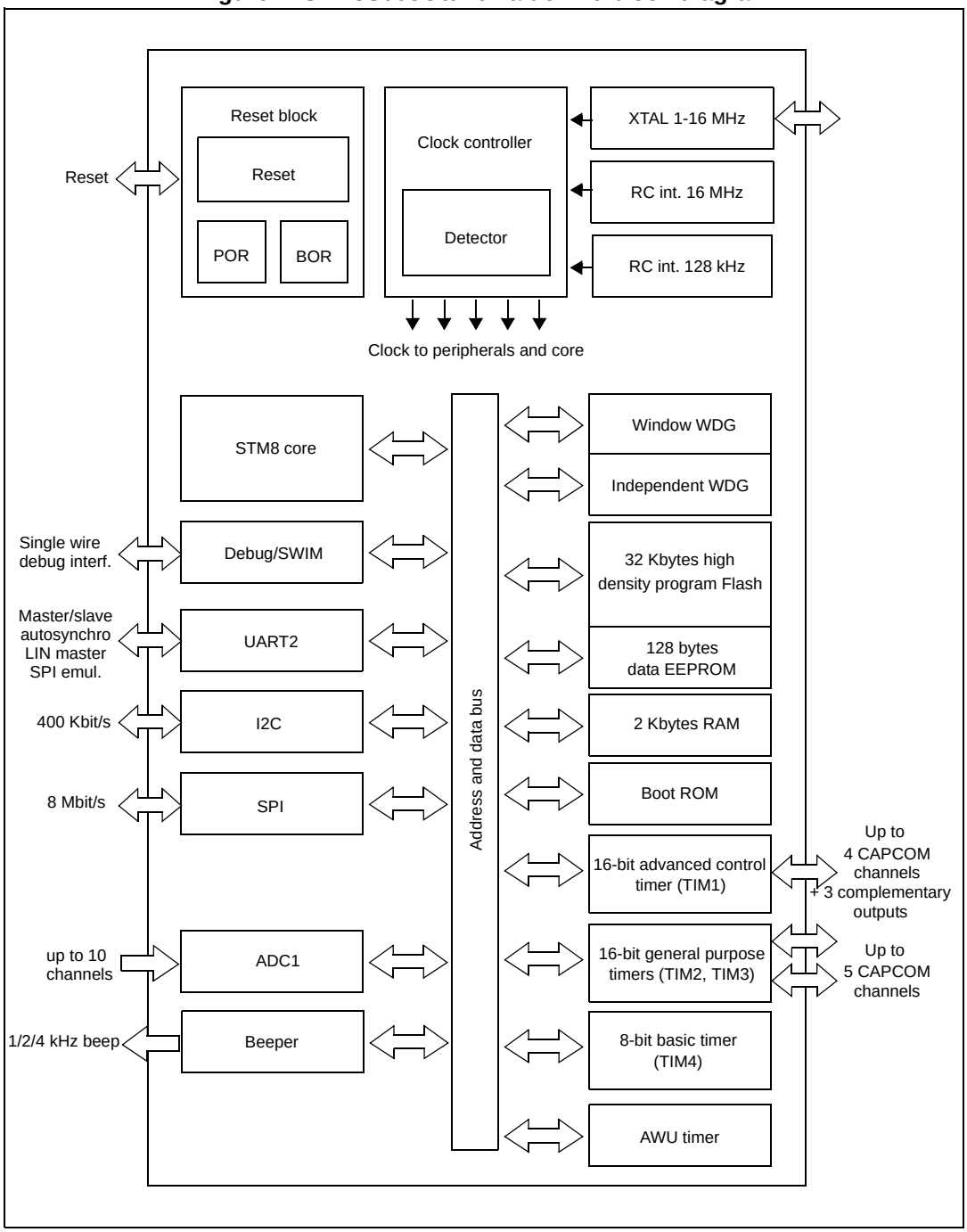
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8A
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s005k6t6ctr

List of tables

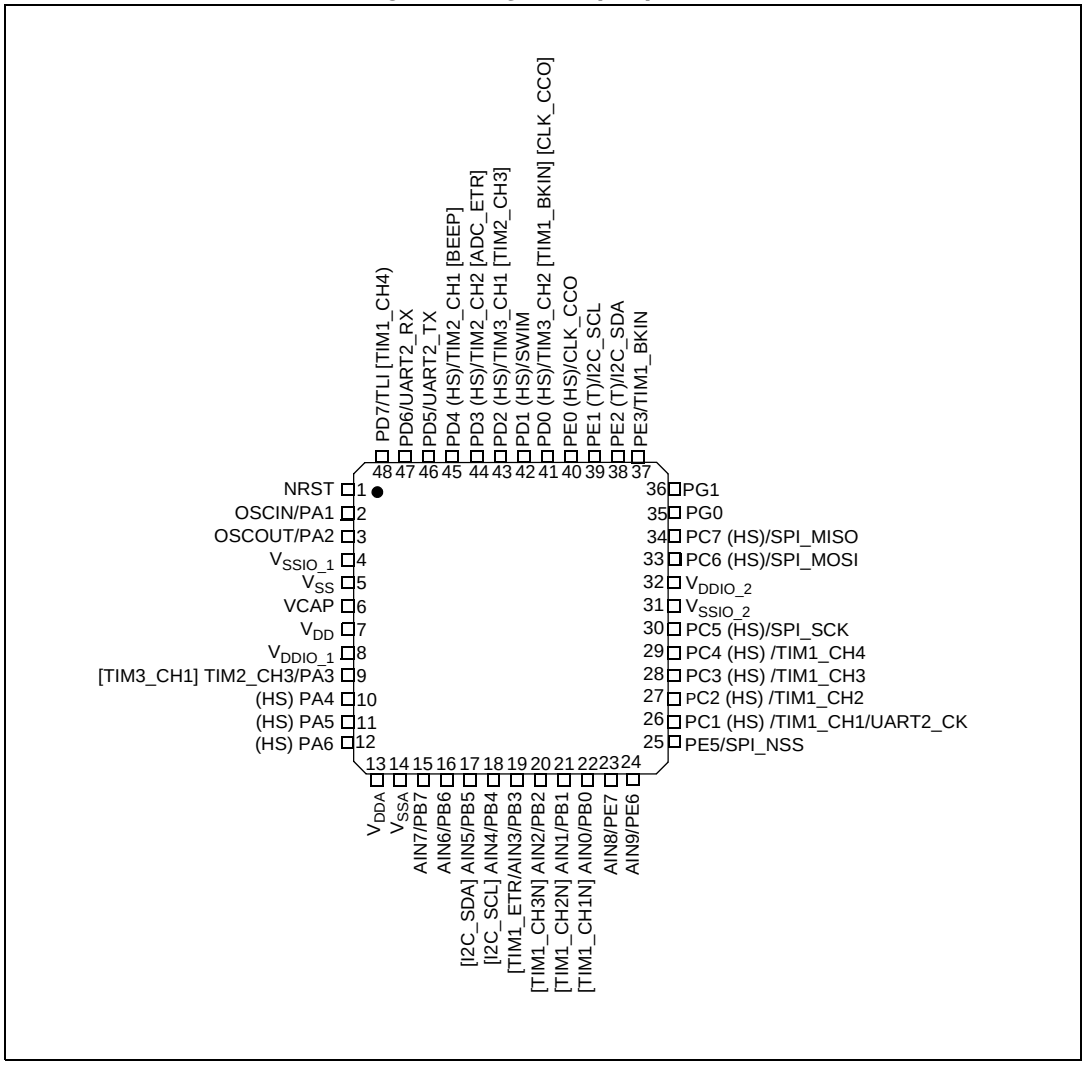
3 Block diagram

Figure 1. STM8S005C6/K6 value line block diagram



5 Pinouts and pin descriptions

Figure 3. LQFP 48-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 5. STM8S005C6 and STM8S005K6 pin descriptions

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	NRST	I/O		**X**						Reset		
2	2	PA1/OSCIN	I/O	**X**	X			O1	X	X	**Port A1**	Resonator/ crystal in	
3	3	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/ crystal out	
4	-	V_{SSIO_1}	S								I/O ground		
5	4	V_{SS}	S								Digital ground		
6	5	VCAP	S								1.8 V regulator capacitor		
7	6	V_{DD}	S								Digital power supply		
8	7	V_{DDIO_1}	S								I/O power supply		
9	-	PA3/TIM2_CH3	I/O	**X**	X	X		O1	X	X	**Port A3**	Timer 2 - channel3	TIM3_CH1 [AFR1]
10	-	PA4	I/O	**X**	X	X	HS	O3	X	X	**Port A4**		
11	-	PA5	I/O	**X**	X	X	HS	O3	X	X	**Port A5**		
12	-	PA6	I/O	**X**	X	X	HS	O3	X	X	**Port A6**		
-	8	PF4/AIN12(1)	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12 (2)	
13	9	V_{DDA}	S								Analog power supply		
14	10	V_{SSA}	S								Analog ground		
15	-	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
16	-	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
17	11	PB5/AIN5 [I^2C_SDA]	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	12	PB4/AIN4 [I^2C_SCL]	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	13	PB3/AIN3 [TIM1_ETR]	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
20	14	PB2/AIN2 [TIM1_CH3N]	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input 2	TIM1_ CH3N [AFR5]
21	15	PB1/AIN1 [TIM1_CH2N]	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_ CH2N [AFR5]

Table 5. STM8S005C6 and STM8S005K6 pin descriptions (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
41	25	PD0/TIM3_CH2 [TIM1_BKIN] [CLK_CCO]	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
43	27	PD2/TIM3_CH1 [TIM2_CH3]	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
44	28	PD3/TIM2_CH2 [ADC_ETR]	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
45	29	PD4/TIM2_CH1 [BEEP]	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	30	PD5/ UART2_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	UART2 data transmit	
47	31	PD6/ UART2_RX	I/O	**X**	X	X		O1	X	X	**Port D6**	UART2 data receive	
48	32	PD7/TLI [TIM1_CH4]	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	TIM1_CH4 [AFR4]

1. A pull-up is applied to PF4 during the reset phase. This pin is input floating after reset release.
2. AIN12 is not selectable in ADC scan mode or with analog watchdog.
3. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after the internal reset release.

5.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 8: Option bytes*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).

6 Memory and register map

6.1 Memory map

Figure 5. Memory map

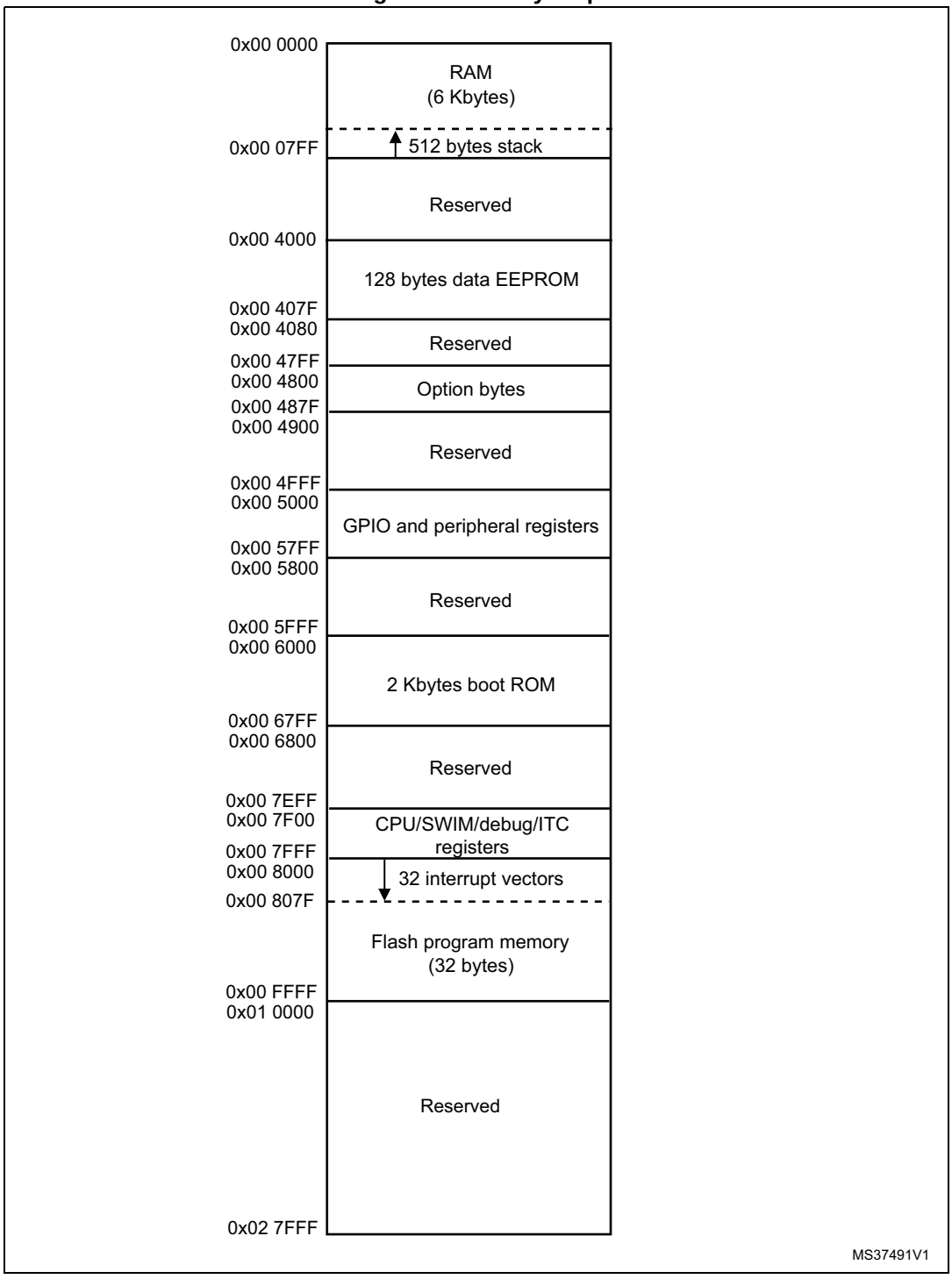


Table 13. Description of alternate function remapping bits [7:0] of OPT2

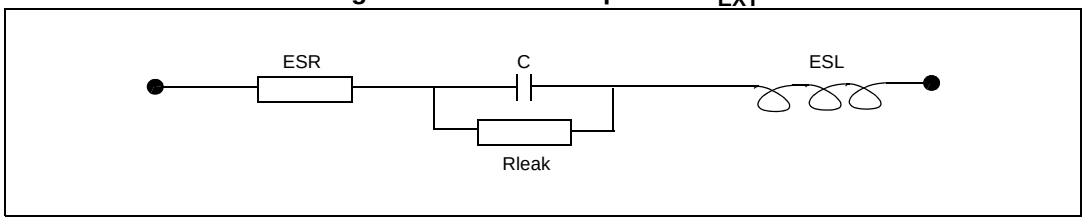
Option byte number	Description(1)
OPT2	**AFR7***Alternate function remapping option 7* 0: AFR7 remapping option inactive: default alternate function(2) 1: Port D4 alternate function = BEEP **AFR6** *Alternate function remapping option 6* 0: AFR6 remapping option inactive: default alternate function(2) 1: Port B5 alternate function = I^2C_SDA; port B4 alternate function = I^2C_SCL **AFR5** *Alternate function remapping option 5* 0: AFR5 remapping option inactive: default alternate function(2) 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_CH3N, port B1 alternate function = TIM1_CH2N, port B0 alternate function = TIM1_CH1N **AFR4** *Alternate function remapping option 4* 0: AFR4 remapping option inactive: default alternate function(2) 1: Port D alternate function = TIM1_CH4 **AFR3** *Alternate function remapping option 3* 0: AFR3 remapping option inactive: default alternate function(2) 1: Port D0 alternate function = TIM1_BKIN **AFR2** *Alternate function remapping option 2* 0: AFR2 remapping option inactive: default alternate function(2) 1: Port D0 alternate function = CLK_CCO Note: AFR2 option has priority over AFR3 if both are activated **AFR1** *Alternate function remapping option 1* 0: AFR1 remapping option inactive: default alternate function(2) 1: Port A3 alternate function = TIM3_CH1; port D2 alternate function TIM2_CH3 **AFR0** *Alternate function remapping option 0* 0: AFR0 remapping option inactive: default alternate function(2) 1: Port D3 alternate function = ADC_ETR

1. Do not use more than one remapping option in the same port.
2. Refer to the pinout description.

9.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 17*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 10. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

9.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 6 on page 42*.

Total current consumption in run mode

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled (clock stopped by Peripheral Clock Gating registers) except if explicitly mentioned.
- When the MCU is clocked at 24 MHz, $T_A \leq 85$ °C and the WAITSTATE option bit is set.

Subject to general operating conditions for V_{DD} and T_A.

Total current consumption in active halt mode

Table 23. Total current consumption in active halt mode at V_{DD} = 5 V, T_A -40 to 85° C

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source			
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal oscillator (16 MHz)	1080	-	µA
				LSI RC oscillator (128 kHz)	200	320	
			Power-down mode	HSE crystal oscillator (16 MHz)	1030	-	
				LSI RC oscillator (128 kHz)	140	270	
		Off	Operating mode	LSI RC oscillator (128 kHz)	68	120	
			Power-down mode		12	60	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Table 24. Total current consumption in active halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions			Typ	Max at 85° C (1)	Unit
		Main voltage regulator (MVR)(2)	Flash mode(3)	Clock source			
$I_{DD(AH)}$	Supply current in active halt mode	On	Operating mode	HSE crystal osc. (16 MHz)	680	-	µA
				LSI RC osc. (128 kHz)	200	320	
			Power-down mode	HSE crystal osc. (16 MHz)	630	-	
				LSI RC osc. (128 kHz)	140	270	
		Off	Operating mode	LSI RC osc. (128 kHz)	66	120	
			Power-down mode		10	60	

1. Data based on characterization results, not tested in production.
2. Configured by the REGAH bit in the CLK_ICKR register.
3. Configured by the AHALT bit in the FLASH_CR1 register.

Figure 15. Typ. $I_{DD(RUN)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz

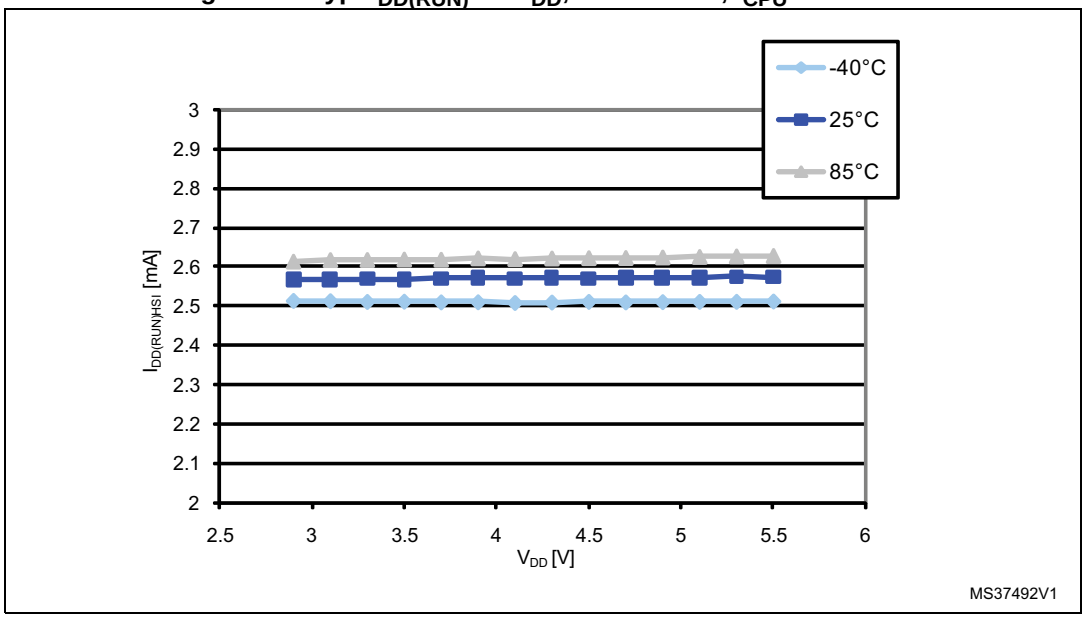
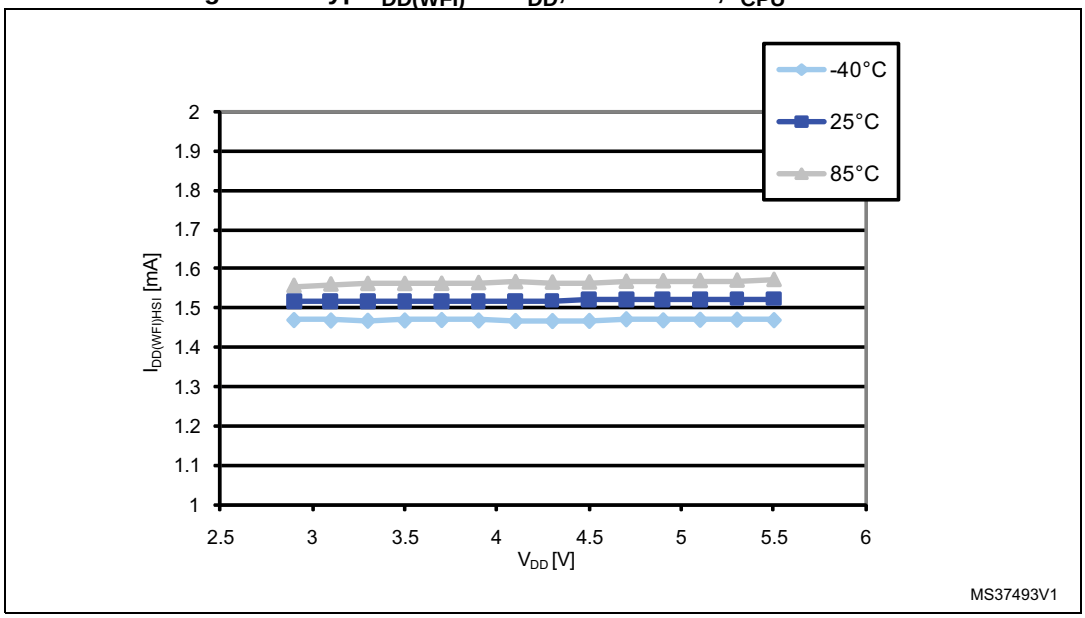


Figure 16. Typ. $I_{DD(WFI)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz



9.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A. f_{HSE}

High speed internal RC oscillator (HSI)

Table 32. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator	Trimmed by the CLK_HSITRIMR register for given V_{DD} and T_A conditions(1)	-	-	1.0(2)	%
	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 5 V, T_A = 25 °C	-	5	-	
		V_{DD} = 5 V, -40 °C ≤ T_A ≤ 85 °C	-5	-	5	
$t_{su(HSI)}$	HSI oscillator wakeup time including calibration	-	-	-	1.0(2)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	170	250(3)	µA

1. See the application note.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production

Figure 19. Typical HSI frequency variation vs V_{DD} at 3 temperatures

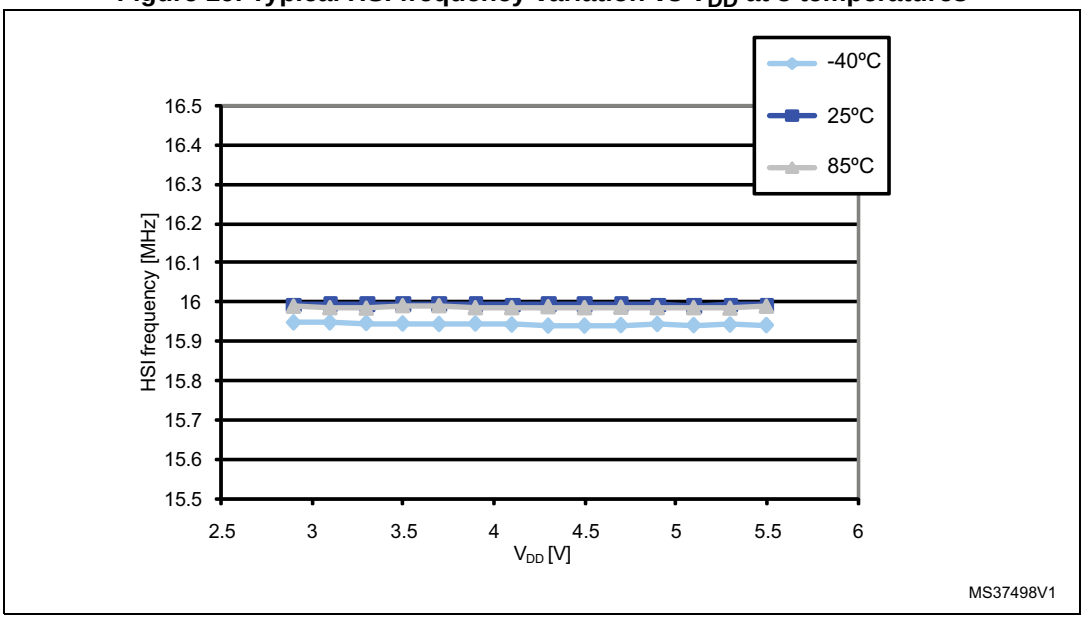


Figure 25. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

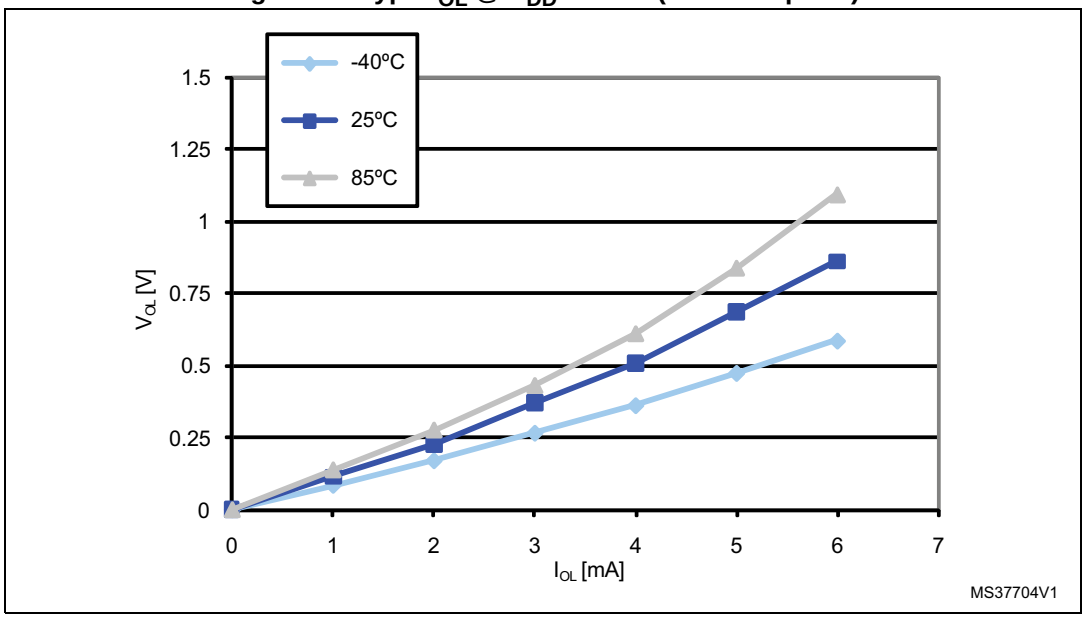


Figure 26. Typ. V_{OL} @ V_{DD} = 5 V (true open drain ports)

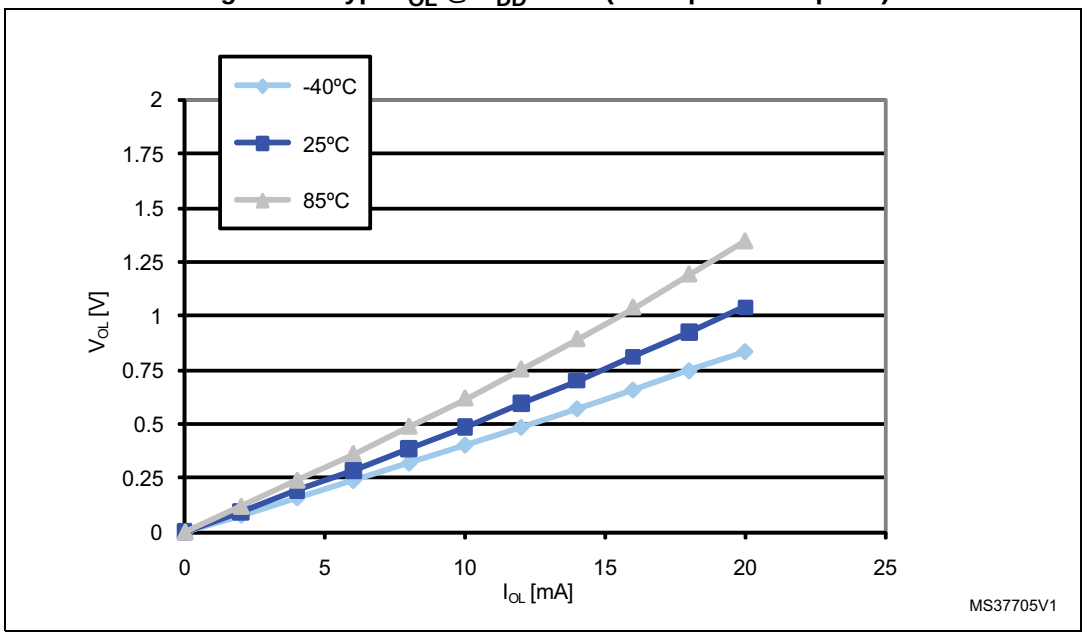


Figure 29. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

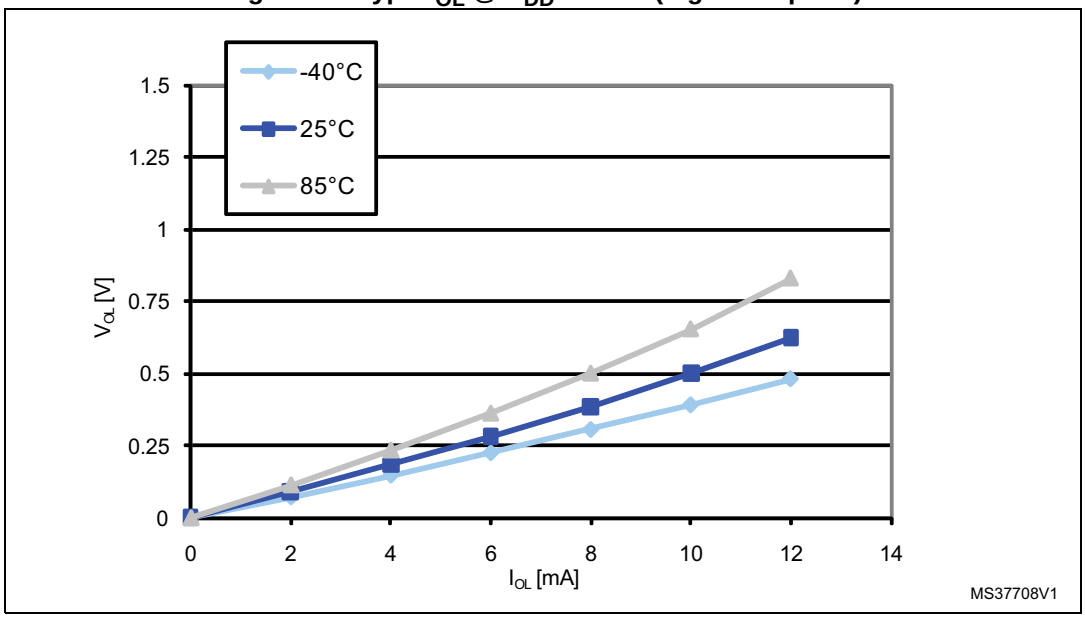


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (standard ports)

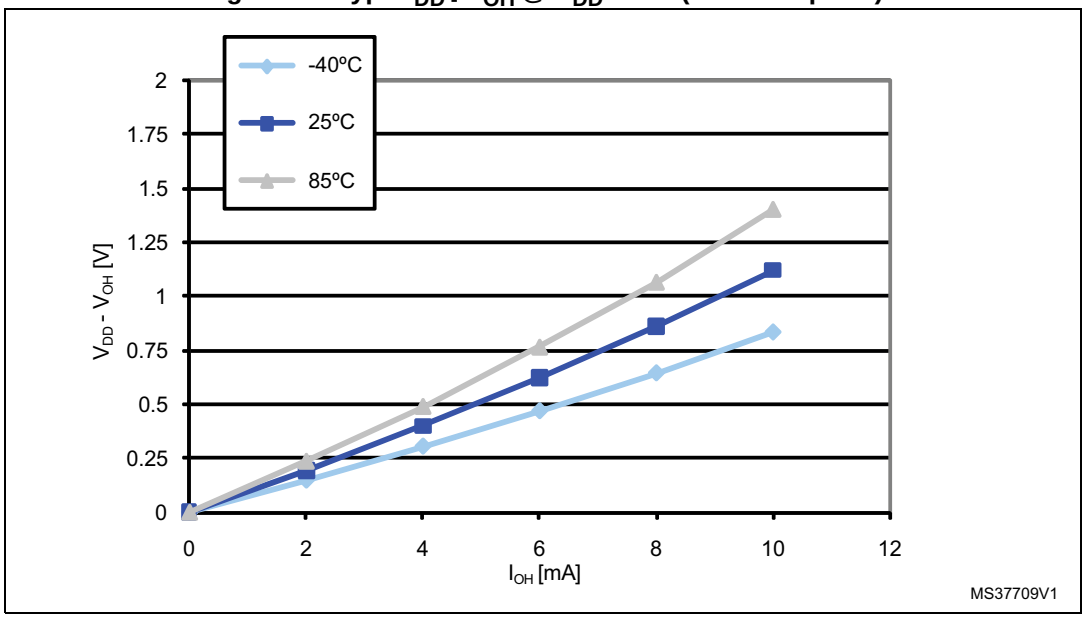
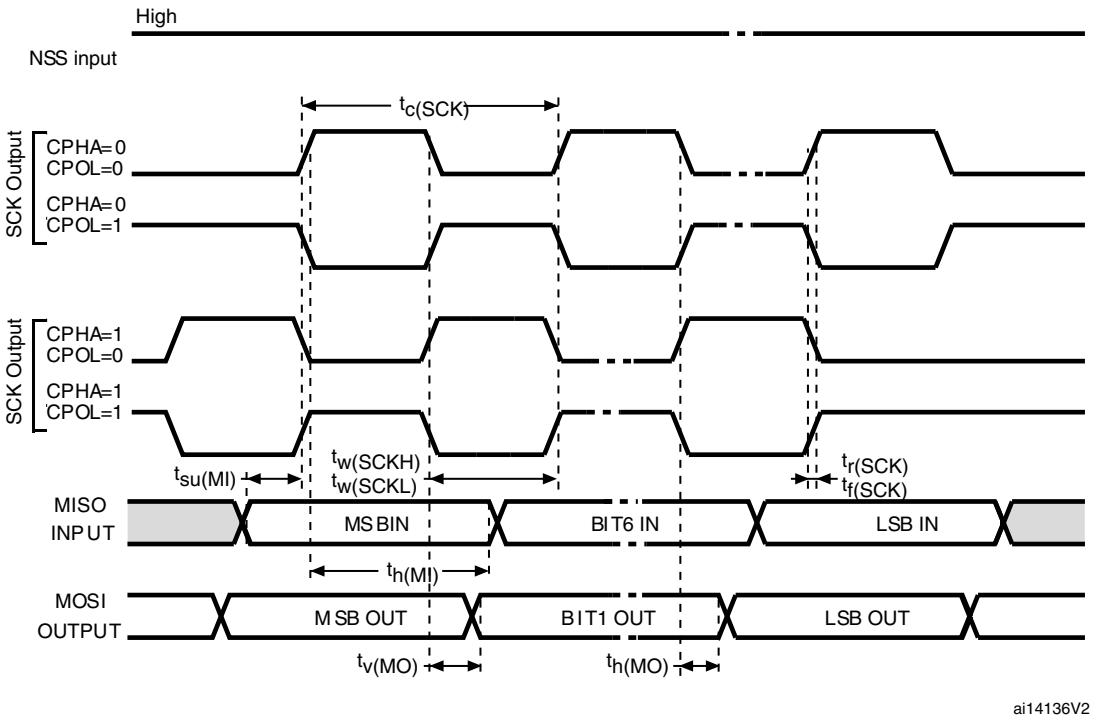


Figure 40. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 44. ADC accuracy with R_{AIN} < 10 kΩ , V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error (2)	f_{ADC} = 2 MHz	1.0	2.5	LSB
		f_{ADC} = 4 MHz	1.4	3	
		f_{ADC} = 6 MHz	1.6	3.5	
$\|E_O\|$	Offset error (2)	f_{ADC} = 2 MHz	0.6	2.0	
		f_{ADC} = 4 MHz	1.1	2.5	
		f_{ADC} = 6 MHz	1.2	2.5	
$\|E_G\|$	Gain error (2)	f_{ADC} = 2 MHz	0.2	2	
		f_{ADC} = 4 MHz	0.6	2.5	
		f_{ADC} = 6 MHz	0.8	2.5	
$\|E_D\|$	Differential linearity error (2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	0.7	1.5	
		f_{ADC} = 6 MHz	0.8	1.5	
$\|E_L\|$	Integral linearity error (2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	
		f_{ADC} = 6 MHz	0.6	1.5	

1. Data based on characterization results, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

Table 45. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DDA} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.1	2.0	LSB
		f_{ADC} = 4 MHz	1.6	2.5	
$\|E_O\|$	Offset error(2)	f_{ADC} = 2 MHz	0.7	1.5	
		f_{ADC} = 4 MHz	1.3	2.0	
$\|E_G\|$	Gain error(2)	f_{ADC} = 2 MHz	0.2	1.5	
		f_{ADC} = 4 MHz	0.5	2.0	
$\|E_D\|$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.0	
$\|E_L\|$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.6	1.5	

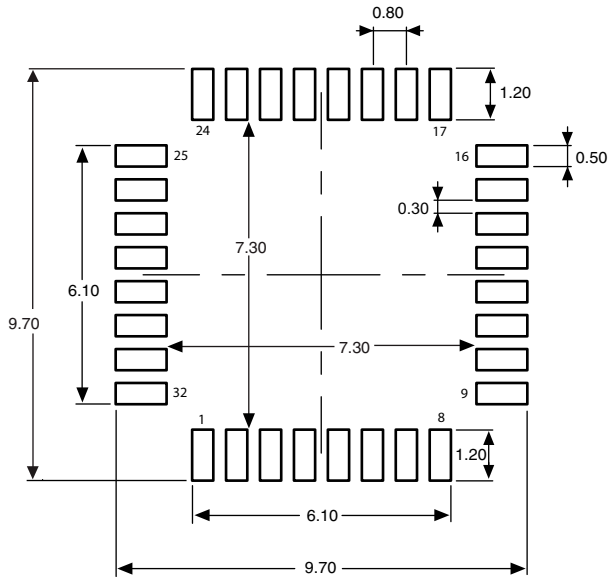
1. Data based on characterization results, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

Table 51. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

10.3.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 50: STM8S005C6/K6 value line ordering information scheme(1)*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

- Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2)
- I_{DDmax} = 15 mA, V_{DD} = 5.5 V
- Maximum eight standard I/Os used at the same time in output at low level with I_{OL} = 10 mA, V_{OL}= 2 V
- Maximum four high sink I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.5 V
- Maximum two true open drain I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 2 V

  P_{INTmax} = 15 mA x 5.5 V = 82.5 mW

  P_{IOmax} = (10 mA x 2 V x 8) + (20 mA x 2 V x 2) + (20 mA x 1.5 V x 4) = 360 mW

  This gives: P_{INTmax} = 82.5 mW and P_{IOmax} 360 mW:

  P_{Dmax} = 82.5 mW + 360 mW

  Thus: P_{Dmax} = 443 mW

Using the values obtained in *Table 52: Thermal characteristics on page 91* T_{Jmax} is calculated as follows for LQFP64 10 x 10 mm = 46 °C/W:

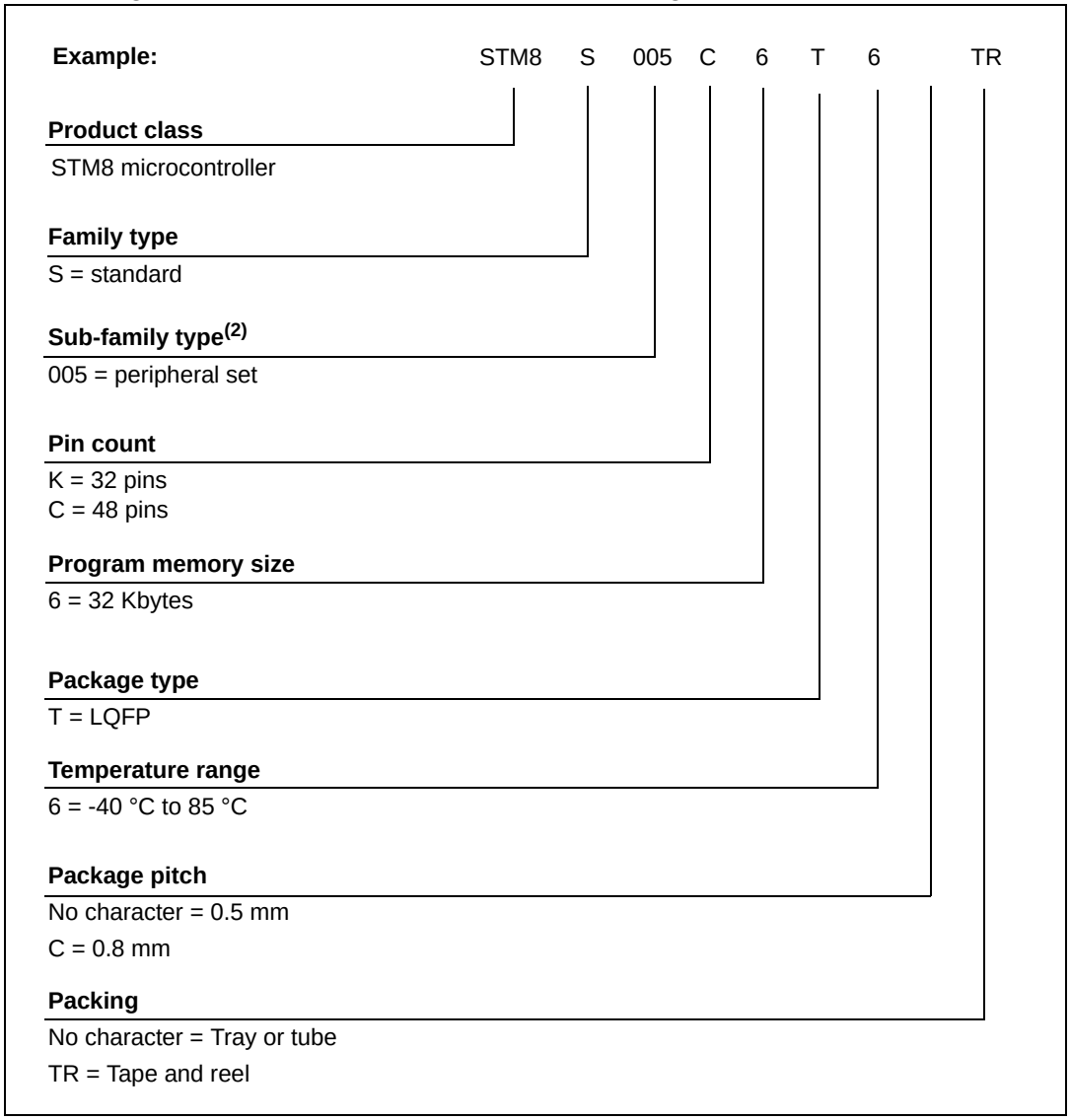
T_{Jmax} = 82 °C + (46 °C/W x 443 mW) = 82 °C + 20 °C = 102 °C

This is within the range of the suffix 6 version parts (-40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6.

11 Part numbering

Figure 50. STM8S005C6/K6 value line ordering information scheme(1)



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.
2. Refer to *Table 1: STM8S005C6/K6 value line features* for detailed description.

12 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows users to specify the components users need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.