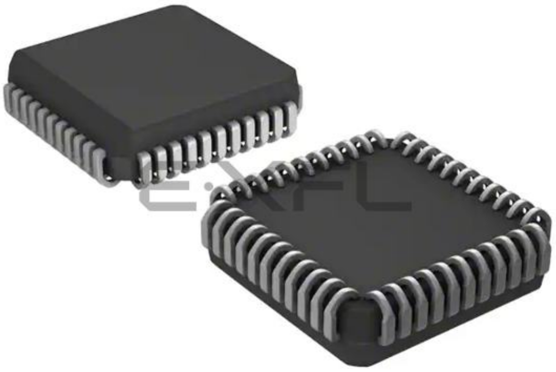


Welcome to E-XFL.COM

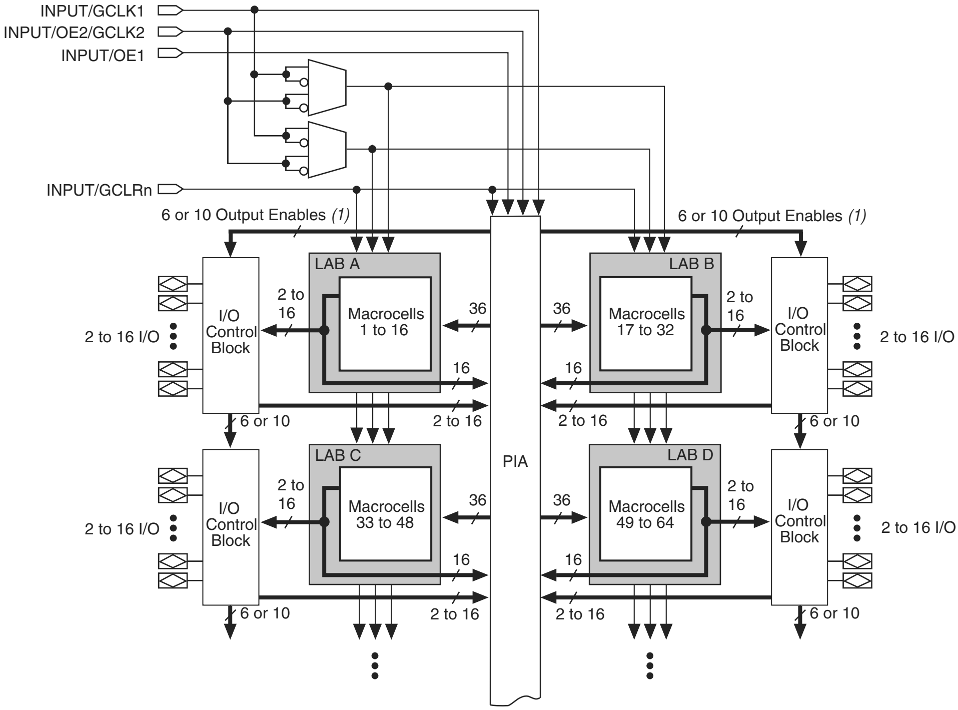
### Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 2 |
| Number of Macrocells | 32 |
| Number of Gates | 600 |
| Number of I/O | 34 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm3032alc44-10 |

*Figure 1. MAX 3000A Device Block Diagram*




*Note:*

(1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

## Logic Array Blocks

The MAX 3000A device architecture is based on the linking of high–performance LABs. LABs consist of 16–macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

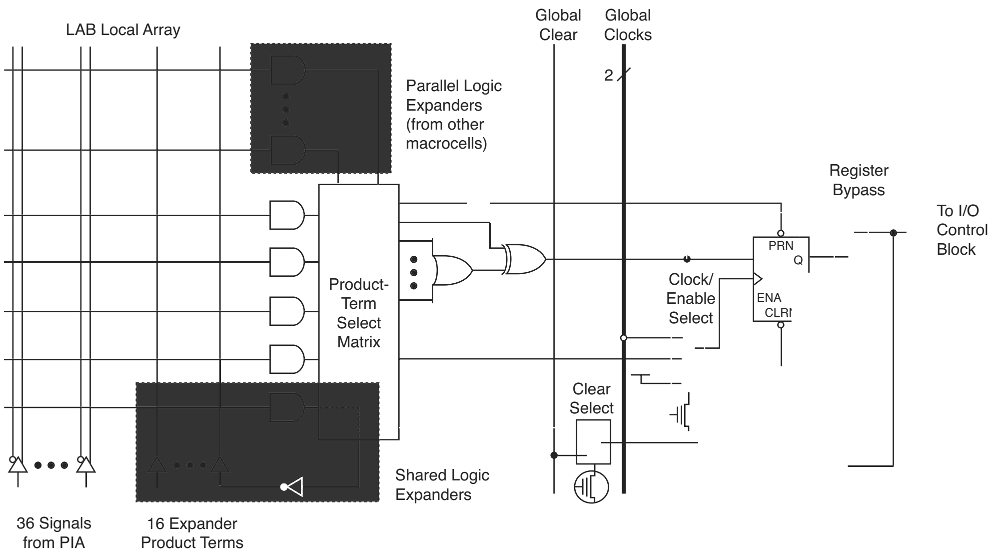
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions

## Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product–term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

*Figure 2. MAX 3000A Macrocell*




Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product–term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product–term allocation according to the logic requirements of the design.

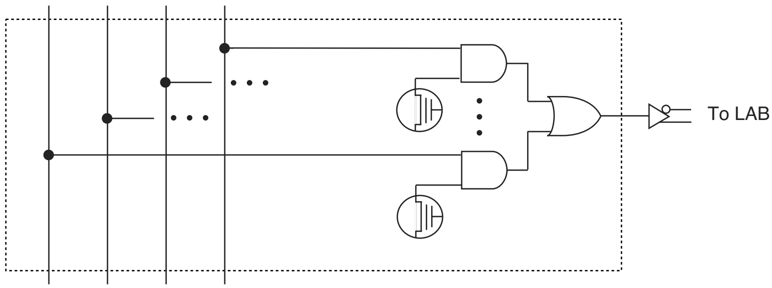
### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower–numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest–numbered macrocell can only lend parallel expanders and the highest–numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

*Figure 5. MAX 3000A PIA Routing*

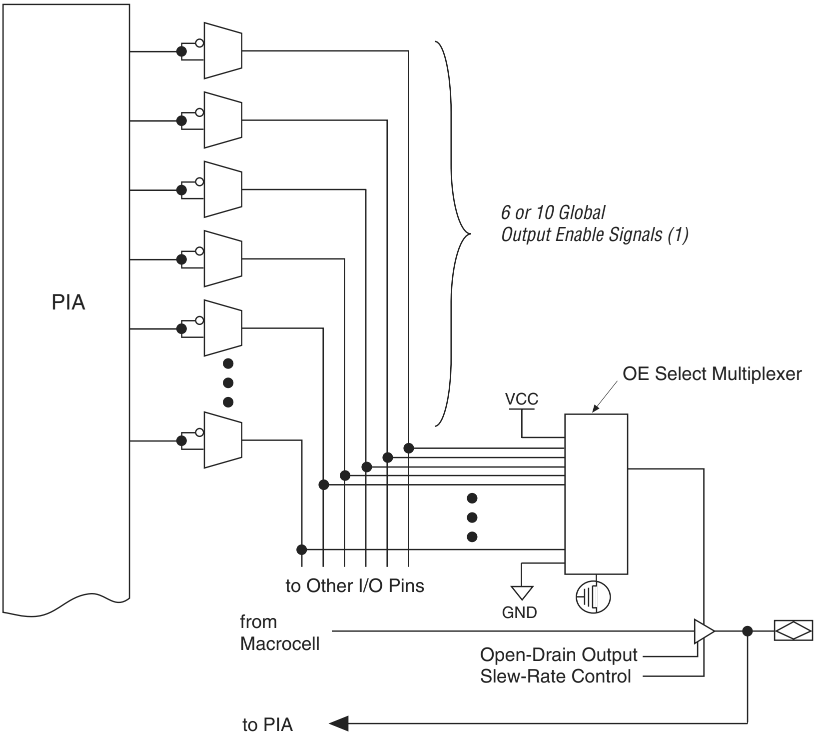



While the routing delays of channel–based routing schemes in masked or FPGAs are cumulative, variable, and path–dependent, the MAX 3000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri–state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or $V_{CC}$. Figure 6 shows the I/O control block for MAX 3000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

*Figure 6. I/O Control Block of MAX 3000A Devices*




*Note:*

(1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

When the tri–state buffer control is connected to ground, the output is tri-stated (high impedance), and the I/O pin can be used as a dedicated input. When the tri–state buffer control is connected to $V_{CC}$, the output is enabled.

The MAX 3000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### Programming a Single MAX 3000A Device

The time required to program a single MAX 3000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: $t_{PROG}$ = Programming time
$t_{PPULSE}$ = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
$f_{TCK}$ = TCK frequency

The ISP times for a stand-alone verification of a single MAX 3000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: $t_{VER}$ = Verify time
$t_{VPULSE}$ = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

## Programming with External Hardware

MAX 3000A devices can be programmed on Windows–based PCs with an Altera Logic Programmer card, MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera software can use text– or waveform–format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.

For more information, see *Programming Hardware Manufacturers*.

## IEEE Std. 1149.1 (JTAG) Boundary–Scan Support

MAX 3000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1–1990. Table 7 describes the JTAG instructions supported by MAX 3000A devices. The pin-out tables found on the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

***Table 7. MAX 3000A JTAG Instructions***

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins |
| EXTEST | Allows the external circuitry and board–level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins |
| BYPASS | Places the 1–bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation |
| IDCODE | Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO` |
| USERCODE | Selects the 32–bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO` |
| ISP Instructions | These instructions are used when programming MAX 3000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster cable, or when using a Jam STAPL file, JBC file, or SVF file via an embedded processor or test equipment |

Figure 7 shows the timing information for the JTAG signals.

***Figure 7. MAX 3000A JTAG Waveforms***

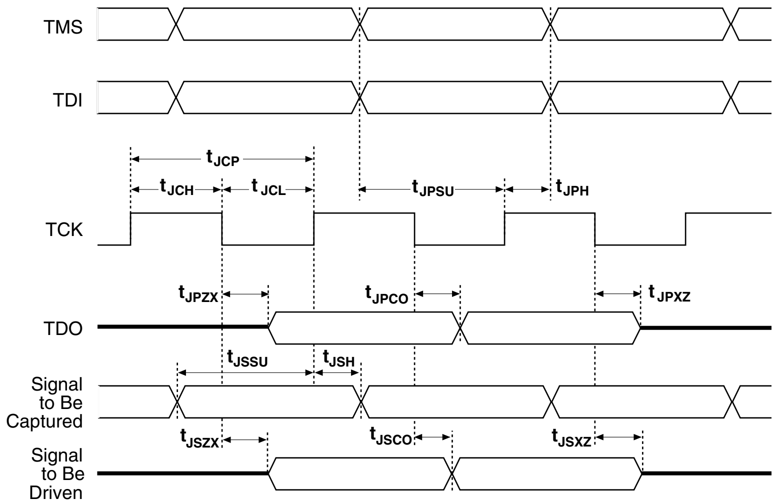



Table 10 shows the JTAG timing parameters and values for MAX 3000A devices.

***Table 10. JTAG Timing Parameters & Values for MAX 3000A Devices***

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | `TCK` clock period | 100 | | ns |
| $t_{JCH}$ | `TCK` clock high time | 50 | | ns |
| $t_{JCL}$ | `TCK` clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

### Open–Drain Output Option

MAX 3000A devices provide an optional open–drain (equivalent to open-collector) output for each I/O pin. This open–drain output enables the device to provide system–level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired–OR plane.

Open-drain output pins on MAX 3000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high $V_{IH}$. When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V, thereby meeting CMOS requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor

### Slew–Rate Control

The output buffer for each MAX 3000A I/O pin has an adjustable output slew rate that can be configured for low–noise or high–speed performance. A faster slew rate provides high–speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low–noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin–by–pin basis. The slew rate control affects both the rising and falling edges of the output signal.

## Design Security

All MAX 3000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

MAX 3000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 8. Test patterns can be used and then erased during early stages of the production flow.

**Table 13. MAX 3000A Device Recommended Operating Conditions**

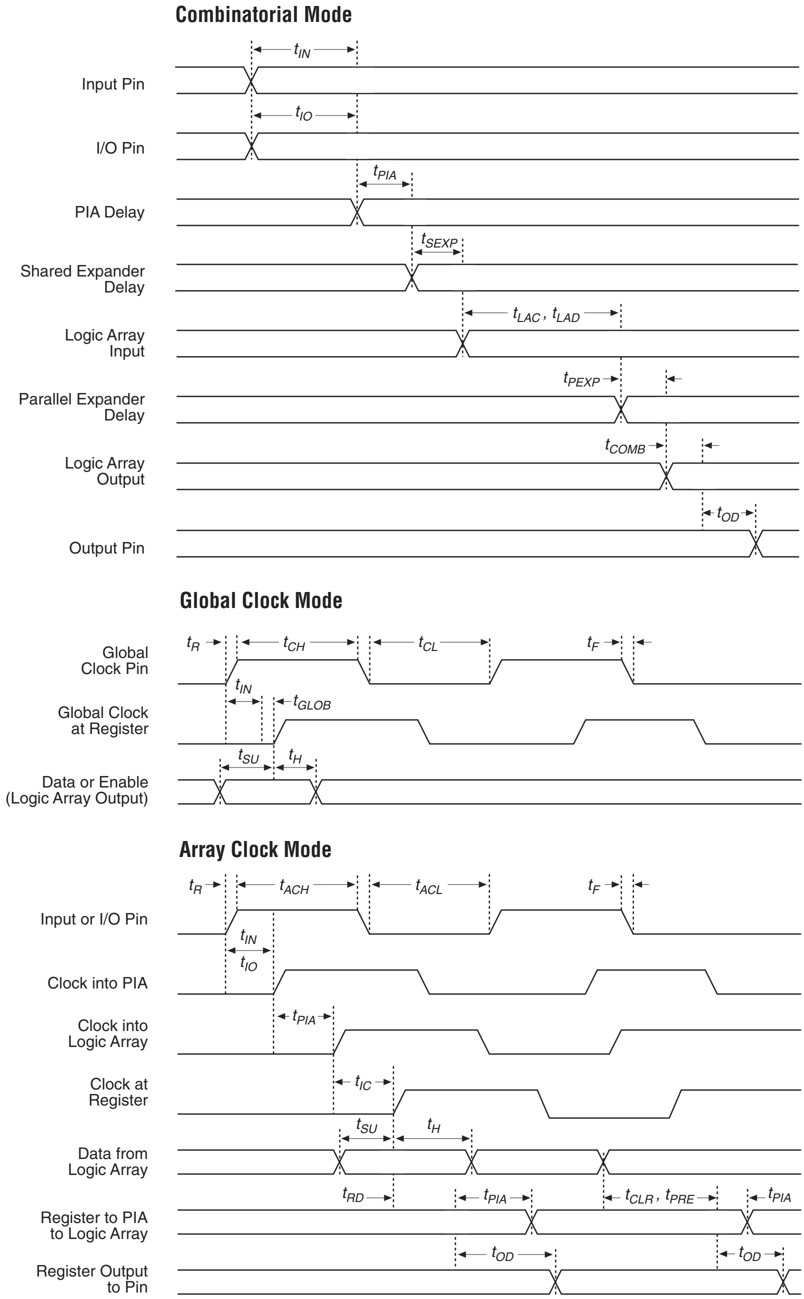
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(10)* | 3.0 | 3.6 | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 3.3–V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers, 2.5–V operation | | 2.3 | 2.7 | V |
| $V_{CCISP}$ | Supply voltage during ISP | | 3.0 | 3.6 | V |
| $V_I$ | Input voltage | *(3)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | Commercial range | 0 | 70 | ° C |
| | | Industrial range | –40 | 85 | ° C |
| $T_J$ | Junction temperature | Commercial range | 0 | 90 | ° C |
| | | Industrial range *(11)* | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

**Table 14. MAX 3000A Device DC Operating Conditions** *Note (4)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High–level input voltage | | 1.7 | 5.75 | V |
| $V_{IL}$ | Low–level input voltage | | –0.5 | 0.8 | V |
| $V_{OH}$ | 3.3–V high–level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | 2.4 | | V |
| | 3.3–V high–level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | $V_{CCIO}$ – 0.2 | | V |
| | 2.5–V high–level output voltage | $I_{OH}$ = –100 µA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 1.7 | | V |
| $V_{OL}$ | 3.3–V low–level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.4 | V |
| | 3.3–V low–level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.2 | V |
| | 2.5–V low–level output voltage | $I_{OL}$ = 100 µA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.7 | V |
| $I_I$ | Input leakage current | $V_I$ = –0.5 to 5.5 V *(7)* | –10 | 10 | µA |
| $I_{OZ}$ | Tri–state output off–state current | $V_I$ = –0.5 to 5.5 V *(7)* | –10 | 10 | µA |
| $R_{ISP}$ | Value of I/O pin pull–up resistor when programming in–system or during power–up | $V_{CCIO}$ = 2.3 to 3.6 V *(8)* | 20 | 74 | kΩ |

*Figure 11. MAX 3000A Switching Waveforms*

*$t_R$ & $t_F$ < 2 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.*



Tables 16 through 23 show EPM3032A, EPM3064A, EPM3128A, EPM3256A, and EPM3512A timing information.

| *Table 16. EPM3032A External Timing Parameters* *Note (1)* | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Speed Grade** | | | | | | **Unit** |
| | | | **–4** | | **–7** | | **–10** | | |
| | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{PD1}$ | Input to non–registered output | C1 = 35 pF *(2)* | | 4.5 | | 7.5 | | 10 | ns |
| $t_{PD2}$ | I/O input to non–registered output | C1 = 35 pF *(2)* | | 4.5 | | 7.5 | | 10 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.9 | | 4.7 | | 6.3 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 3.0 | 1.0 | 5.0 | 1.0 | 6.7 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.6 | | 2.5 | | 3.6 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.3 | | 0.5 | | 0.5 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 4.3 | 1.0 | 7.2 | 1.0 | 9.4 | ns |
| $t_{ACH}$ | Array clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 4.4 | | 7.2 | | 9.7 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(4)* | 227.3 | | 138.9 | | 103.1 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 4.4 | | 7.2 | | 9.7 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(4)* | 227.3 | | 138.9 | | 103.1 | | MHz |

**Table 17. EPM3032A Internal Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –4 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.9 | | 3.1 | | 4.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.5 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.5 | | 2.5 | | 3.3 | ns |
| $t_{LAC}$ | Logic control array delay | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.8 | | 1.3 | | 1.8 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 1.3 | | 1.8 | | 2.3 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.8 | | 6.3 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.3 | | 2.0 | | 2.8 | | ns |
| $t_{H}$ | Register hold time | | 0.6 | | 1.0 | | 1.3 | | ns |
| $t_{RD}$ | Register delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.6 | | 1.0 | | 1.3 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 2.0 | | 2.5 | ns |
| $t_{EN}$ | Register enable time | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{GLOB}$ | Global control delay | | | 0.8 | | 1.3 | | 1.9 | ns |
| $t_{PRE}$ | Register preset time | | | 1.2 | | 1.9 | | 2.6 | ns |
| $t_{CLR}$ | Register clear time | | | 1.2 | | 1.9 | | 2.6 | ns |

***Table 19. EPM3064A Internal Timing Parameters (Part 1 of 2)*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –4 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.6 | | 1.1 | | 1.4 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.6 | | 1.1 | | 1.4 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.8 | | 3.0 | | 3.9 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.7 | | 0.9 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.5 | | 2.5 | | 3.2 | ns |
| $t_{LAC}$ | Logic control array delay | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.8 | | 1.3 | | 1.8 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 1.3 | | 1.8 | | 2.3 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.8 | | 6.3 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.3 | | 2.0 | | 2.9 | | ns |
| $t_{H}$ | Register hold time | | 0.6 | | 1.0 | | 1.3 | | ns |
| $t_{RD}$ | Register delay | | | 0.7 | | 1.2 | | 1.6 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 1.9 | | 2.5 | ns |
| $t_{EN}$ | Register enable time | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.0 | | 1.5 | | 2.2 | ns |
| $t_{PRE}$ | Register preset time | | | 1.3 | | 2.1 | | 2.9 | ns |

| *Table 19. EPM3064A Internal Timing Parameters (Part 2 of 2) Note (1)* | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Speed Grade** | | | | | | **Unit** |
| | | | **–4** | | **–7** | | **–10** | | |
| | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{CLR}$ | Register clear time | | | 1.3 | | 2.1 | | 2.9 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 1.0 | | 1.7 | | 2.3 | ns |
| $t_{LPA}$ | Low–power adder | *(5)* | | 3.5 | | 4.0 | | 5.0 | ns |

| *Table 20. EPM3128A External Timing Parameters Note (1)* | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Speed Grade** | | | | | | **Unit** |
| | | | **–5** | | **–7** | | **–10** | | |
| | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{PD1}$ | Input to non–registered output | C1 = 35 pF *(2)* | | 5.0 | | 7.5 | | 10 | ns |
| $t_{PD2}$ | I/O input to non–registered output | C1 = 35 pF *(2)* | | 5.0 | | 7.5 | | 10 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 3.3 | | 4.9 | | 6.6 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 3.4 | 1.0 | 5.0 | 1.0 | 6.6 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.8 | | 2.8 | | 3.8 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.3 | | 0.4 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 4.9 | 1.0 | 7.1 | 1.0 | 9.4 | ns |
| $t_{ACH}$ | Array clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 5.2 | | 7.7 | | 10.2 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2), (4)* | 192.3 | | 129.9 | | 98.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 5.2 | | 7.7 | | 10.2 | ns |

**Table 22. EPM3256A External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 7.9 | | 10.5 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2), (4)* | 126.6 | | 95.2 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 7.9 | | 10.5 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2), (4)* | 126.6 | | 95.2 | | MHz |

**Table 23. EPM3256A Internal Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.9 | | 1.2 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.9 | | 1.2 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 2.8 | | 3.7 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.5 | | 0.6 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.2 | | 2.8 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.0 | | 1.3 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.2 | | 1.6 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 1.7 | | 2.1 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.2 | | 6.6 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 4.5 | | 5.5 | ns |

### *Figure 13. $I_{CC}$ vs. Frequency for MAX 3000A Devices*

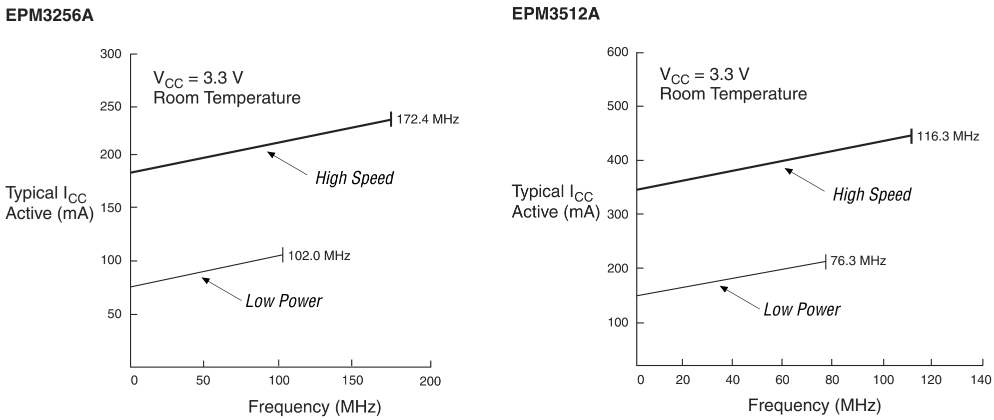


***Figure 15. 100–Pin TQFP Package Pin–Out Diagram***

*Package outline not drawn to scale.*

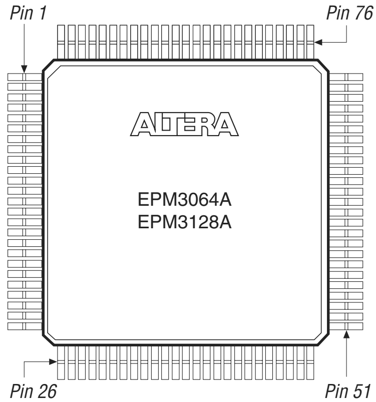



***Figure 16. 144–Pin TQFP Package Pin–Out Diagram***

*Package outline not drawn to scale.*

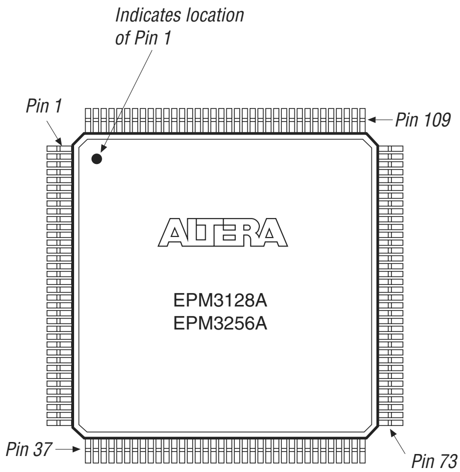
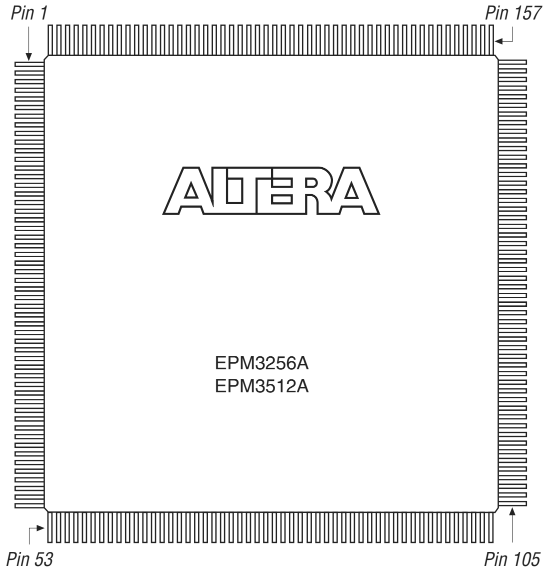


***Figure 17. 208–Pin PQFP Package Pin–Out Diagram***

*Package outline not drawn to scale.*



## Version 3.3

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.3:

- Updated Tables 3, 13, and 26.
- Added Tables 4 through 6.
- Updated Figures 12 and 13.
- Added "Programming Sequence" on page 14 and "Programming Times" on page 14

## Version 3.2

The following change were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.2:

- Updated the EPM3512 $I_{CC}$ versus frequency graph in Figure 13.

## Version 3.1

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.1:

- Updated timing information in Table 1 for the EPM3256A device.
- Updated *Note (10)* of Table 15.

## Version 3.0

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.0:

- Added EPM3512A device.
- Updated Tables 2 and 3.

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