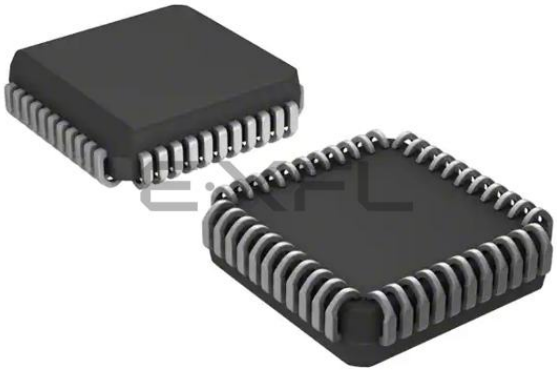


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

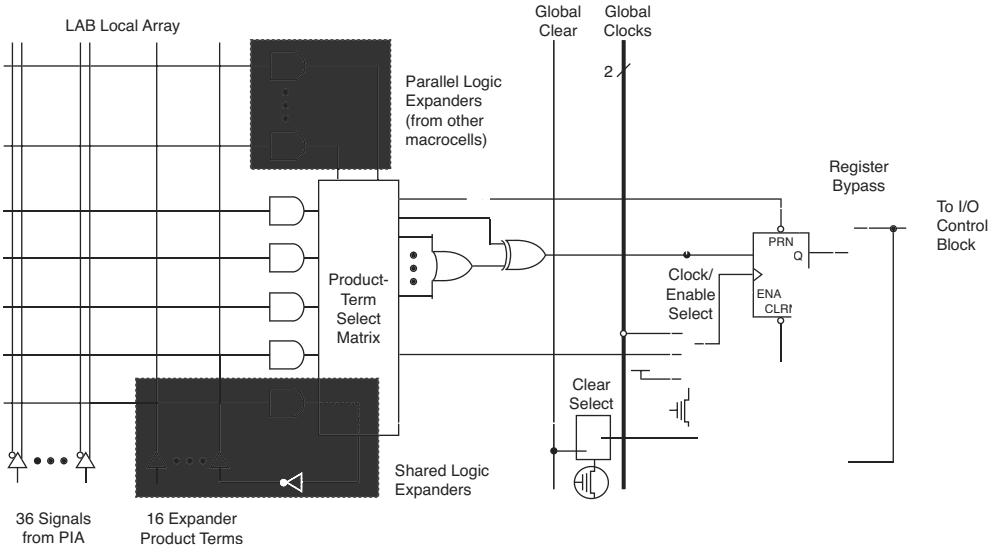
Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	600
Number of I/O	34
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm3032alc44-7

Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product–term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

Figure 2. MAX 3000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product–term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product–term allocation according to the logic requirements of the design.

Parallel Expanders

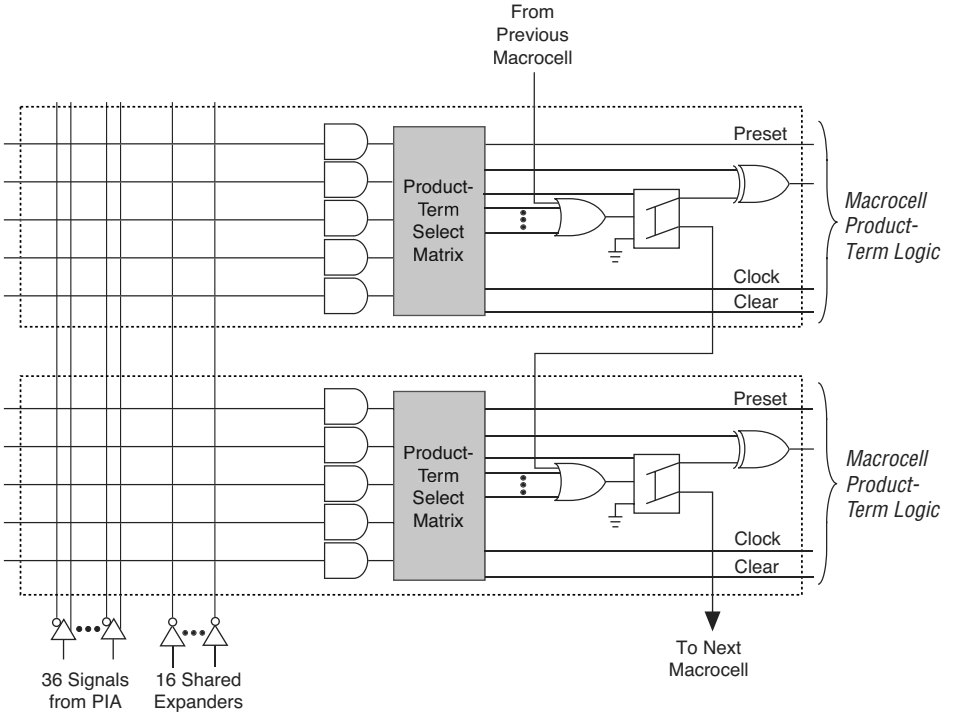
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower–numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest–numbered macrocell can only lend parallel expanders and the highest–numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 3000A Parallel Expanders

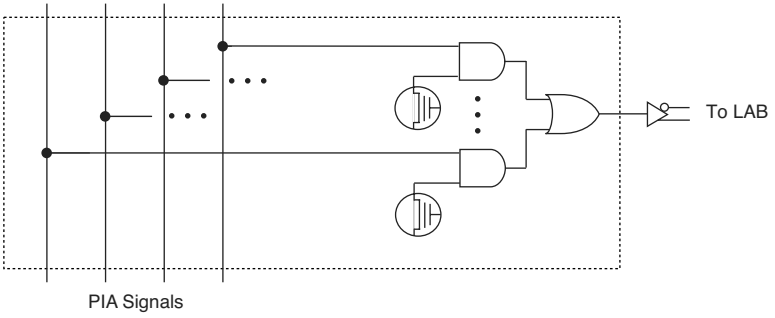
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 3000A PIA Routing



While the routing delays of channel–based routing schemes in masked or FPGAs are cumulative, variable, and path–dependent, the MAX 3000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri–state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 3000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

In–System Programmability

MAX 3000A devices can be programmed in–system via an industry–standard four–pin IEEE Std. 1149.1-1990 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The MAX 3000A architecture internally generates the high programming voltages required to program its EEPROM cells, allowing in–system programming with only a single 3.3–V power supply. During in–system programming, the I/O pins are tri–stated and weakly pulled–up to eliminate board conflicts. The pull–up value is nominally 50 kΩ

MAX 3000A devices have an enhanced ISP algorithm for faster programming. These devices also offer an `ISP_Done` bit that ensures safe operation when in–system programming is interrupted. This `ISP_Done` bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board (PCB) with standard pick–and–place equipment before they are programmed. MAX 3000A devices can be programmed by downloading the information via in–circuit testers, embedded processors, the MasterBlaster communications cable, the ByteBlasterMV parallel port download cable, and the BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high–pin–count packages (e.g., QFP packages) due to device handling. MAX 3000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

The Jam STAPL programming and test language can be used to program MAX 3000A devices with in–circuit testers, PCs, or embedded processors.

For more information on using the Jam STAPL programming and test language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)*, *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)* and *AN 111 (Embedded Programming Using the 8051 and Jam Byte-Code)*.

The ISP circuitry in MAX 3000A devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary–scan register length and device IDCODE information for MAX 3000A devices.

Table 8. MAX 3000A Boundary–Scan Register Length

Device	Boundary–Scan Register Length
EPM3032A	96
EPM3064A	192
EPM3128A	288
EPM3256A	480
EPM3512A	624

Table 9. 32–Bit MAX 3000A Device IDCODE Value *Note (1)*

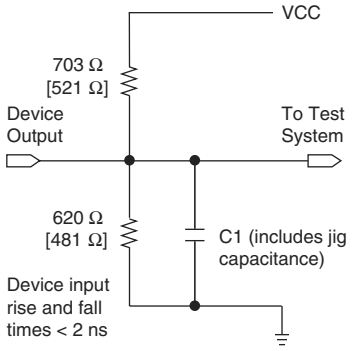
Device	IDCODE (32 bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM3032A	0001	0111 0000 0011 0010	00001101110	1
EPM3064A	0001	0111 0000 0110 0100	00001101110	1
EPM3128A	0001	0111 0001 0010 1000	00001101110	1
EPM3256A	0001	0111 0010 0101 0110	00001101110	1
EPM3512A	0001	0111 0101 0001 0010	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary–Scan Testing in Altera Devices)* for more information on JTAG BST.

Figure 8. MAX 3000A AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large–amplitude, fast–ground–current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5–V outputs. Numbers without brackets are for 3.3–V devices or outputs.



Operating Conditions

Tables 12 through 15 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for MAX 3000A devices.

Table 12. MAX 3000A Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_A	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP and TQFP packages, under bias		135	° C

Table 13. MAX 3000A Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(10)*	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3–V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5–V operation		2.3	2.7	V
V_{CCISP}	Supply voltage during ISP		3.0	3.6	V
V_I	Input voltage	*(3)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	Commercial range	0	70	° C
		Industrial range	–40	85	° C
T_J	Junction temperature	Commercial range	0	90	° C
		Industrial range *(11)*	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 14. MAX 3000A Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High–level input voltage		1.7	5.75	V
V_{IL}	Low–level input voltage		–0.5	0.8	V
V_{OH}	3.3–V high–level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(5)*	2.4		V
	3.3–V high–level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(5)*	V_{CCIO} – 0.2		V
	2.5–V high–level output voltage	I_{OH} = –100 µA DC, V_{CCIO} = 2.30 V *(5)*	2.1		V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(5)*	2.0		V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(5)*	1.7		V
V_{OL}	3.3–V low–level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V *(6)*		0.4	V
	3.3–V low–level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(6)*		0.2	V
	2.5–V low–level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V *(6)*		0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(6)*		0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(6)*		0.7	V
I_I	Input leakage current	V_I = –0.5 to 5.5 V *(7)*	–10	10	µA
I_{OZ}	Tri–state output off–state current	V_I = –0.5 to 5.5 V *(7)*	–10	10	µA
R_{ISP}	Value of I/O pin pull–up resistor when programming in–system or during power–up	V_{CCIO} = 2.3 to 3.6 V *(8)*	20	74	kΩ

Table 15. MAX 3000A Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

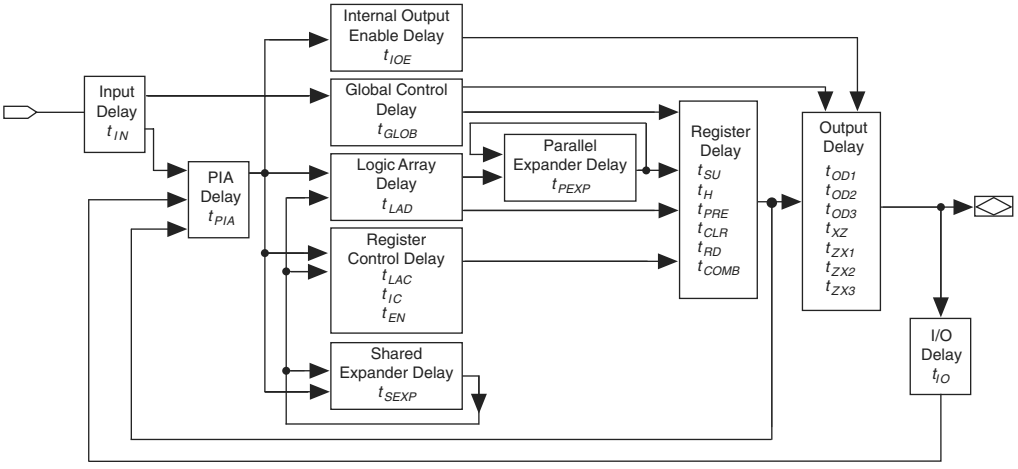
(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(4) These values are specified under the recommended operating conditions, as shown in Table 13 on page 23.
(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high–level TTL or CMOS output current.
(6) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low–level TTL, PCI, or CMOS output current.
(7) This value is specified during normal device operation. During power-up, the maximum leakage current is ±300 µA.
(8) This pull–up exists while devices are programmed in–system and in unprogrammed devices during power–up.
(9) Capacitance is measured at 25° C and is sample–tested only. The `OE1` pin (high–voltage pin during programming) has a maximum capacitance of 20 pF.
(10) The POR time for all MAX 3000A devices does not exceed 100 µs. The sufficient V_{CCINT} voltage level for POR is 3.0 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
(11) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

Figure 9 shows the typical output drive characteristics of MAX 3000A devices.

Timing Model

MAX 3000A device timing can be analyzed with the Altera software, with a variety of popular industry–standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 3000A devices have predictable internal delays that enable the designer to determine the worst–case timing of any design. The software provides timing simulation, point–to–point delay prediction, and detailed timing analysis for device–wide performance evaluation.

Figure 10. MAX 3000A Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin–to–pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the timing relationship between internal and external delay parameters.

Figure 11. MAX 3000A Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

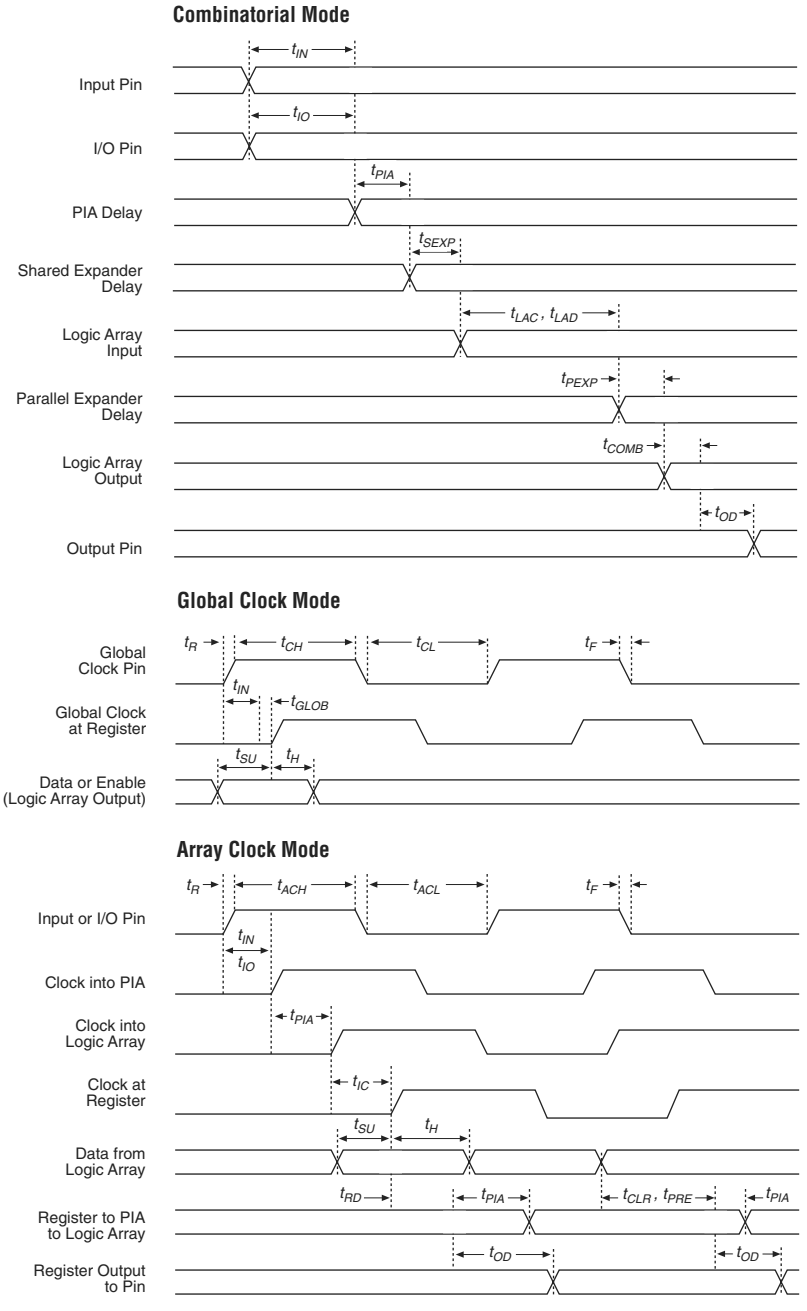


Table 17. EPM3032A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–4		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.2		1.5	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.2		1.5	ns
t_{SEXP}	Shared expander delay			1.9		3.1		4.0	ns
t_{PEXP}	Parallel expander delay			0.5		0.8		1.0	ns
t_{LAD}	Logic array delay			1.5		2.5		3.3	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.8		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{RD}	Register delay			0.7		1.2		1.5	ns
t_{COMB}	Combinatorial delay			0.6		1.0		1.3	ns
t_{IC}	Array clock delay			1.2		2.0		2.5	ns
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			0.8		1.3		1.9	ns
t_{PRE}	Register preset time			1.2		1.9		2.6	ns
t_{CLR}	Register clear time			1.2		1.9		2.6	ns

Table 19. EPM3064A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–4		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t_{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.5		2.5		3.2	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.9		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{RD}	Register delay			0.7		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.9		2.5	ns
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			1.0		1.5		2.2	ns
t_{PRE}	Register preset time			1.3		2.1		2.9	ns

Table 19. EPM3064A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–4		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{CLR}	Register clear time			1.3		2.1		2.9	ns
t_{PIA}	PIA delay	*(2)*		1.0		1.7		2.3	ns
t_{LPA}	Low–power adder	*(5)*		3.5		4.0		5.0	ns

Table 20. EPM3128A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–5		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non–registered output	C1 = 35 pF *(2)*		5.0		7.5		10	ns
t_{PD2}	I/O input to non–registered output	C1 = 35 pF *(2)*		5.0		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	3.3		4.9		6.6		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.4	1.0	5.0	1.0	6.6	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.8		2.8		3.8		ns
t_{AH}	Array clock hold time	*(2)*	0.2		0.3		0.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.9	1.0	7.1	1.0	9.4	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		5.2		7.7		10.2	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	192.3		129.9		98.0		MHz
t_{ACNT}	Minimum array clock period	*(2)*		5.2		7.7		10.2	ns

Table 20. EPM3128A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–5		–7		–10		
			Min	Max	Min	Max	Min	Max	
f_{ACNT}	Maximum internal array clock frequency	*(2), (4)*	192.3		129.9		98.0		MHz

Table 21. EPM3128A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–5		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.0		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.0		1.4	ns
t_{SEXP}	Shared expander delay			2.0		2.9		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.6		2.4		3.1	ns
t_{LAC}	Logic control array delay			0.7		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.3		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns

Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.0		6.5	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0	ns
t_{SU}	Register setup time		2.1		3.0		ns
t_{H}	Register hold time		0.6		0.8		ns
t_{FSU}	Register setup time of fast input		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		ns
t_{RD}	Register delay			1.3		1.7	ns
t_{COMB}	Combinatorial delay			0.6		0.8	ns
t_{IC}	Array clock delay			1.8		2.3	ns
t_{EN}	Register enable time			1.0		1.3	ns
t_{GLOB}	Global control delay			1.7		2.2	ns
t_{PRE}	Register preset time			1.0		1.4	ns
t_{CLR}	Register clear time			1.0		1.4	ns
t_{PIA}	PIA delay	*(2)*		3.0		4.0	ns
t_{LPA}	Low-power adder	*(5)*		4.5		5.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.

(2) These values are specified for a PIA fan–out of one LAB (16 macrocells). For each additional LAB fan–out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(4) These parameters are measured with a 16–bit loadable, enabled, up/down counter programmed into each LAB.

(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in low–power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 3000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in the I_{CCINT} equation are:

MC_{TON}	=	Number of macrocells with the Turbo Bit™ option turned on, as reported in the Quartus II or MAX+PLUS II Report File (**.rpt**)
MC_{DEV}	=	Number of macrocells in the device
MC_{USED}	=	Total number of macrocells in the design, as reported in the RPT File
$\mathbf{f_{MAX}}$	=	Highest clock frequency to the device
$\mathbf{tog_{LC}}$	=	Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C	=	Constants (shown in Table 26)

Table 26. MAX 3000A I_{CC} Equation Constants

Device	A	B	C
EPM3032A	0.71	0.30	0.014
EPM3064A	0.71	0.30	0.014
EPM3128A	0.71	0.30	0.014
EPM3256A	0.71	0.30	0.014
EPM3512A	0.71	0.30	0.014

The I_{CCINT} calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16–bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figures 12 and 13 show the typical supply current versus frequency for MAX 3000A devices.

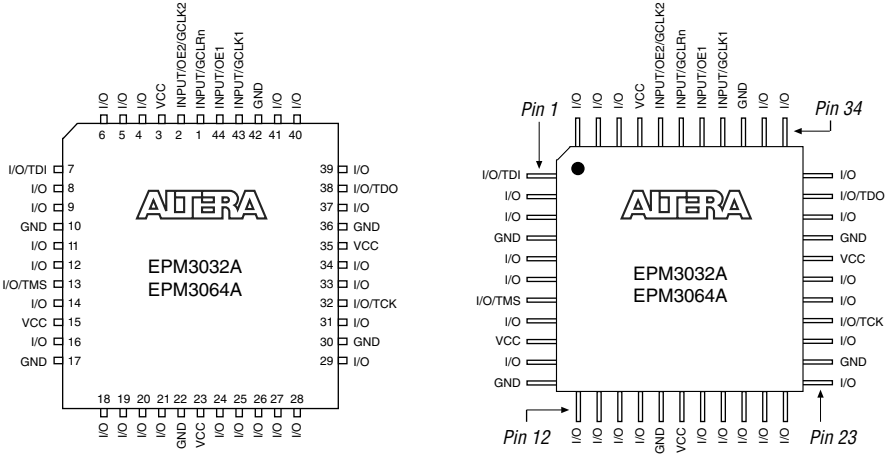
Device Pin–Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin–out information.

Figures 14 through 18 show the package pin–out diagrams for MAX 3000A devices.

Figure 14. 44–Pin PLCC/TQFP Package Pin–Out Diagram

Package outlines not drawn to scale.



44-Pin PLCC

44-Pin TQFP

Figure 15. 100–Pin TQFP Package Pin–Out Diagram

Package outline not drawn to scale.

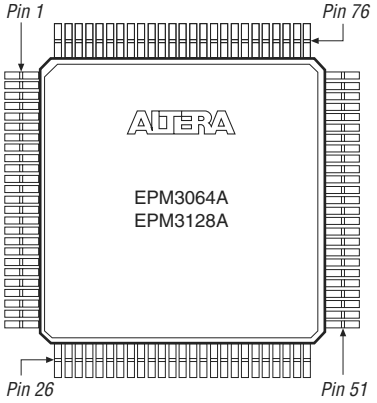


Figure 16. 144–Pin TQFP Package Pin–Out Diagram

Package outline not drawn to scale.

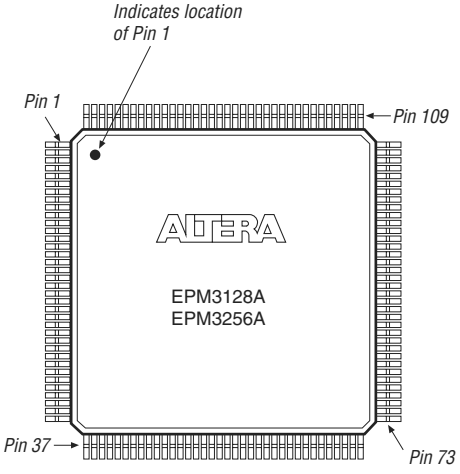


Figure 18. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

Revision History

The information contained in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5 supersedes information published in previous versions. The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5:

Version 3.5

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5:

- New paragraph added before "Expander Product Terms".

Version 3.4

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.4:

- Updated Table 1.