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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	34
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm3064alc44-4n">https://www.e-xfl.com/product-detail/intel/epm3064alc44-4n</a>

## ...and More Features

- PCI compatible
- Bus-friendly architecture including programmable slew-rate control
- Open-drain output option
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a power reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- Enhanced architectural features, including:
  - 6 or 10 pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from third-party manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with the Altera master programming unit (MPU), MasterBlaster™ communications cable, ByteBlasterMV™ parallel port download cable, BitBlaster™ serial download cable as well as programming hardware from third-party manufacturers and any in-circuit tester that supports Jam™ Standard Test and Programming Language (STAPL) Files (.jam), Jam STAPL Byte-Code Files (.jbc), or Serial Vector Format Files (.svf)

## General Description

MAX 3000A devices are low-cost, high-performance devices based on the Altera MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 3000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 3000A devices in the -4, -5, -6, -7, and -10 speed grades are compatible with the timing requirements of the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See Table 2.

**Table 2. MAX 3000A Speed Grades**

Device	Speed Grade				
	-4	-5	-6	-7	-10
EPM3032A	✓			✓	✓
EPM3064A	✓			✓	✓
EPM3128A		✓		✓	✓
EPM3256A				✓	✓
EPM3512A				✓	✓

The MAX 3000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density small-scale integration (SSI), medium-scale integration (MSI), and large-scale integration (LSI) logic functions. The MAX 3000A architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 3000A devices are available in a wide range of packages, including PLCC, PQFP, and TQFP packages. See Table 3.

**Table 3. MAX 3000A Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA
EPM3032A	34	34				
EPM3064A	34	34	66			
EPM3128A			80	96		98
EPM3256A				116	158	161
EPM3512A					172	208

**Note:**

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

MAX 3000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 3000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debugging cycles, and can be programmed and erased up to 100 times.

MAX 3000A devices contain 32 to 512 macrocells, combined into groups of 16 macrocells called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with shareable expander and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 3000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 3000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 3000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 3000A devices to be used in mixed-voltage systems.

MAX 3000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The MAX 3000A architecture includes the following elements:

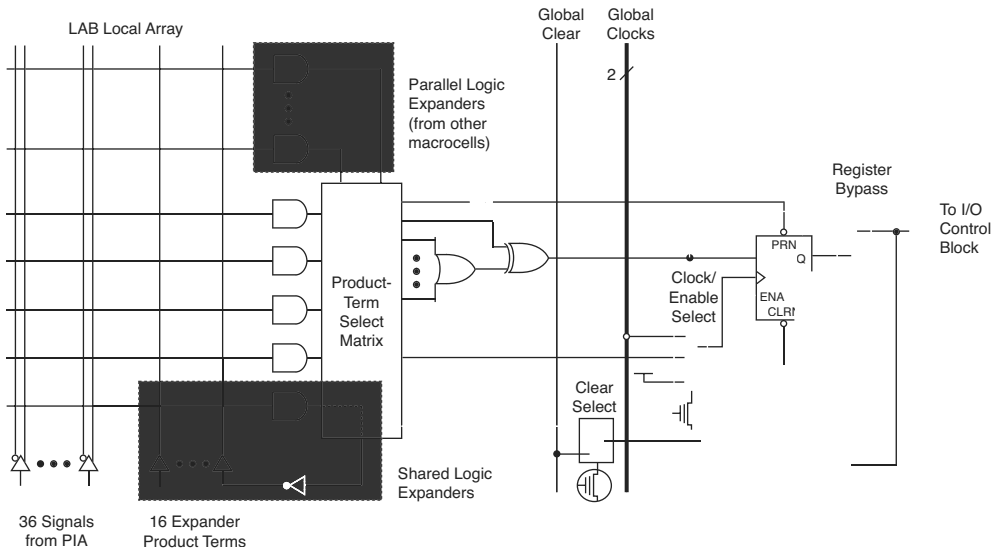
- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array (PIA)
- I/O control blocks

The MAX 3000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 3000A devices.

## Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product-term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

**Figure 2. MAX 3000A Macrocell**



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development system software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal mode, which achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 3000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the two global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn).

All registers are cleared upon power-up. By default, all registered outputs drive low when the device is powered up. You can set the registered outputs to drive high upon power-up through the Quartus® II software. Quartus II software uses the NOT Gate Push-Back method, which uses an additional macrocell to set the output high. To set this in the Quartus II software, go to the Assignment Editor and set the **Power-Up Level** assignment for the register to **High**.

## Expander Product Terms

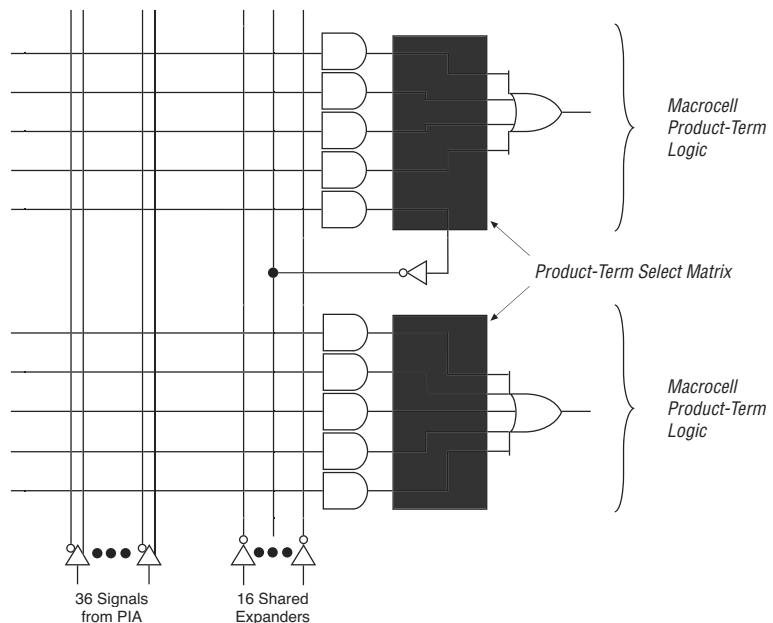
Although most logic functions can be implemented with the five product terms available in each macrocell, highly complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 3000A architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shareable expanders incur a small delay ( $t_{SEXP}$ ). Figure 3 shows how shareable expanders can feed multiple macrocells.

**Figure 3. MAX 3000A Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in an LAB.*



### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.



By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 3000A Device*

The time required to program a single MAX 3000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:  $t_{PROG}$  = Programming time  
 $t_{PPULSE}$  = Sum of the fixed times to erase, program, and verify the EEPROM cells  
 $Cycle_{PTCK}$  = Number of TCK cycles to program a device  
 $f_{TCK}$  = TCK frequency

The ISP times for a stand-alone verification of a single MAX 3000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:  $t_{VER}$  = Verify time  
 $t_{VPULSE}$  = Sum of the fixed times to verify the EEPROM cells  
 $Cycle_{VTCK}$  = Number of TCK cycles to verify a device

## Programming with External Hardware

MAX 3000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.



For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see *Programming Hardware Manufacturers*.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 3000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1–1990. Table 7 describes the JTAG instructions supported by MAX 3000A devices. The pin-out tables found on the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

**Table 7. MAX 3000A JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO
ISP Instructions	These instructions are used when programming MAX 3000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster cable, or when using a Jam STAPL file, JBC file, or SVF file via an embedded processor or test equipment

The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary-scan register length and device IDCODE information for MAX 3000A devices.

**Table 8. MAX 3000A Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPM3032A	96
EPM3064A	192
EPM3128A	288
EPM3256A	480
EPM3512A	624

**Table 9. 32-Bit MAX 3000A Device IDCODE Value** Note (1)

Device	IDCODE (32 bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM3032A	0001	0111 0000 0011 0010	00001101110	1
EPM3064A	0001	0111 0000 0110 0100	00001101110	1
EPM3128A	0001	0111 0001 0010 1000	00001101110	1
EPM3256A	0001	0111 0010 0101 0110	00001101110	1
EPM3512A	0001	0111 0101 0001 0010	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

Figure 7 shows the timing information for the JTAG signals.

**Figure 7. MAX 3000A JTAG Waveforms**

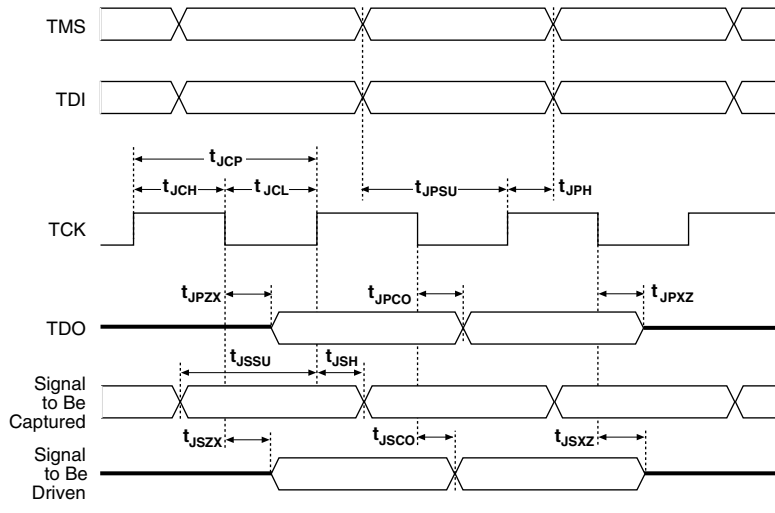


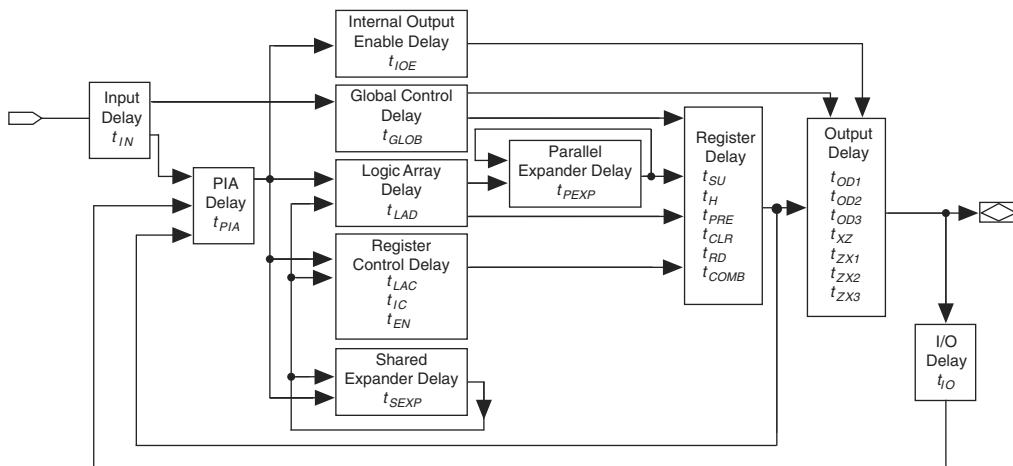
Table 10 shows the JTAG timing parameters and values for MAX 3000A devices.

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns

## Timing Model

MAX 3000A device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 3000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

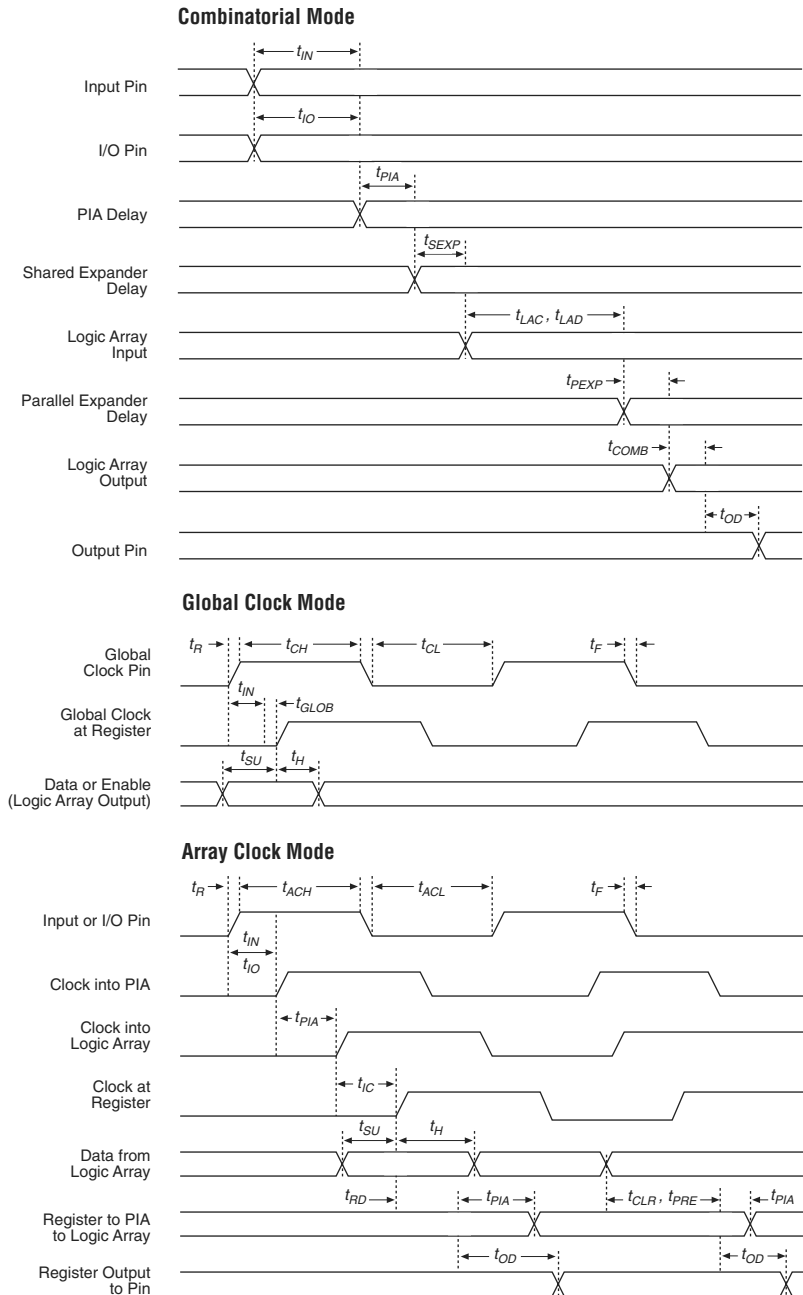
**Figure 10. MAX 3000A Timing Model**



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the timing relationship between internal and external delay parameters.

**Figure 11. MAX 3000A Switching Waveforms**

$t_R$  &  $t_F < 2$  ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



**Table 17. EPM3032A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
$t_{PIA}$	PIA delay	(2)		0.9		1.5		2.1	ns
$t_{LPA}$	Low-power adder	(5)		2.5		4.0		5.0	ns

**Table 18. EPM3064A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.8		4.7		6.2		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.1	1.0	5.1	1.0	7.0	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.6		2.6		3.6		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.3		0.4		0.6		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.6	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		4.5		7.4		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	222.2		135.1		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		4.5		7.4		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	222.2		135.1		100.0		MHz

**Table 20. EPM3128A External Timing Parameters** Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			−5		−7		−10		
			Min	Max	Min	Max	Min	Max	
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	192.3		129.9		98.0		MHz

**Table 21. EPM3128A Internal Timing Parameters (Part 1 of 2)** Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		1.0		1.4	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		1.0		1.4	ns
$t_{SEXP}$	Shared expander delay			2.0		2.9		3.8	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.7		0.9	ns
$t_{LAD}$	Logic array delay			1.6		2.4		3.1	ns
$t_{LAC}$	Logic control array delay			0.7		1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.2		1.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.3		1.7		2.1	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns



**Table 21. EPM3128A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−5		−7		−10		
			Min	Max	Min	Max	Min	Max	
$t_{SU}$	Register setup time		1.4		2.1		2.9		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{RD}$	Register delay			0.8		1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.5		0.9		1.3	ns
$t_{IC}$	Array clock delay			1.2		1.7		2.2	ns
$t_{EN}$	Register enable time			0.7		1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.1		1.6		2.0	ns
$t_{PRE}$	Register preset time			1.4		2.0		2.7	ns
$t_{CLR}$	Register clear time			1.4		2.0		2.7	ns
$t_{PIA}$	PIA delay	(2)		1.4		2.0		2.6	ns
$t_{LPA}$	Low-power adder	(5)		4.0		4.0		5.0	ns

**Table 22. EPM3256A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		7.5		10	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		7.5		10	ns
t <sub>SU</sub>	Global clock setup time	(2)	5.2		6.9		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	4.8	1.0	6.4	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	2.7		3.6		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.3		0.5		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	7.3	1.0	9.7	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	3.0		4.0		ns

**Table 24. EPM3512A External Timing Parameters** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.3		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	7.8	1.0	10.4	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		8.6		11.5	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	116.3		87.0		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		8.6		11.5	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	116.3		87.0		MHz

**Table 25. EPM3512A Internal Timing Parameters (Part 1 of 2)** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		0.9	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		0.9	ns
$t_{FIN}$	Fast input delay			3.1		3.6	ns
$t_{SEXP}$	Shared expander delay			2.7		3.5	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.5	ns
$t_{LAD}$	Logic array delay			2.2		2.8	ns
$t_{LAC}$	Logic control array delay			1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	C1 = 35 pF		1.0		1.5	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	C1 = 35 pF		1.5		2.0	ns

**Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

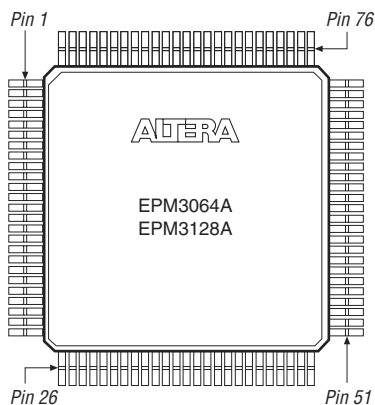
Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.5	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0	ns
$t_{SU}$	Register setup time		2.1		3.0		ns
$t_H$	Register hold time		0.6		0.8		ns
$t_{FSU}$	Register setup time of fast input		1.6		1.6		ns
$t_{FH}$	Register hold time of fast input		1.4		1.4		ns
$t_{RD}$	Register delay			1.3		1.7	ns
$t_{COMB}$	Combinatorial delay			0.6		0.8	ns
$t_{IC}$	Array clock delay			1.8		2.3	ns
$t_{EN}$	Register enable time			1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.7		2.2	ns
$t_{PRE}$	Register preset time			1.0		1.4	ns
$t_{CLR}$	Register clear time			1.0		1.4	ns
$t_{PIA}$	PIA delay	(2)		3.0		4.0	ns
$t_{LPA}$	Low-power adder	(5)		4.5		5.0	ns

**Notes to tables:**

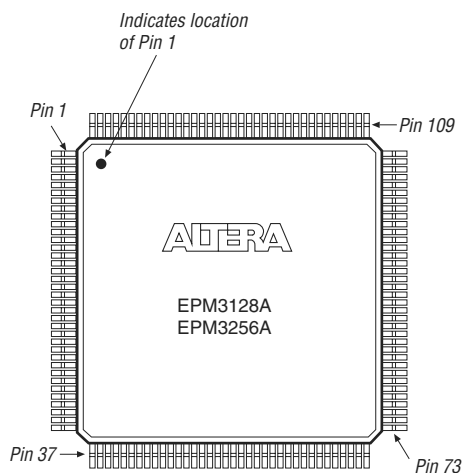
- These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.
- These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in low-power mode.

**Figure 15. 100-Pin TQFP Package Pin-Out Diagram**

Package outline not drawn to scale.

**Figure 16. 144-Pin TQFP Package Pin-Out Diagram**

Package outline not drawn to scale.



**Figure 17. 208-Pin PQFP Package Pin-Out Diagram**

*Package outline not drawn to scale.*

