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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	34
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm3064ali44-10

Table 2. MAX 3000A Speed Grades

Device	Speed Grade				
	-4	-5	-6	-7	-10
EPM3032A	✓			✓	✓
EPM3064A	✓			✓	✓
EPM3128A		✓		✓	✓
EPM3256A				✓	✓
EPM3512A				✓	✓

The MAX 3000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density small-scale integration (SSI), medium-scale integration (MSI), and large-scale integration (LSI) logic functions. The MAX 3000A architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 3000A devices are available in a wide range of packages, including PLCC, PQFP, and TQFP packages. See Table 3.

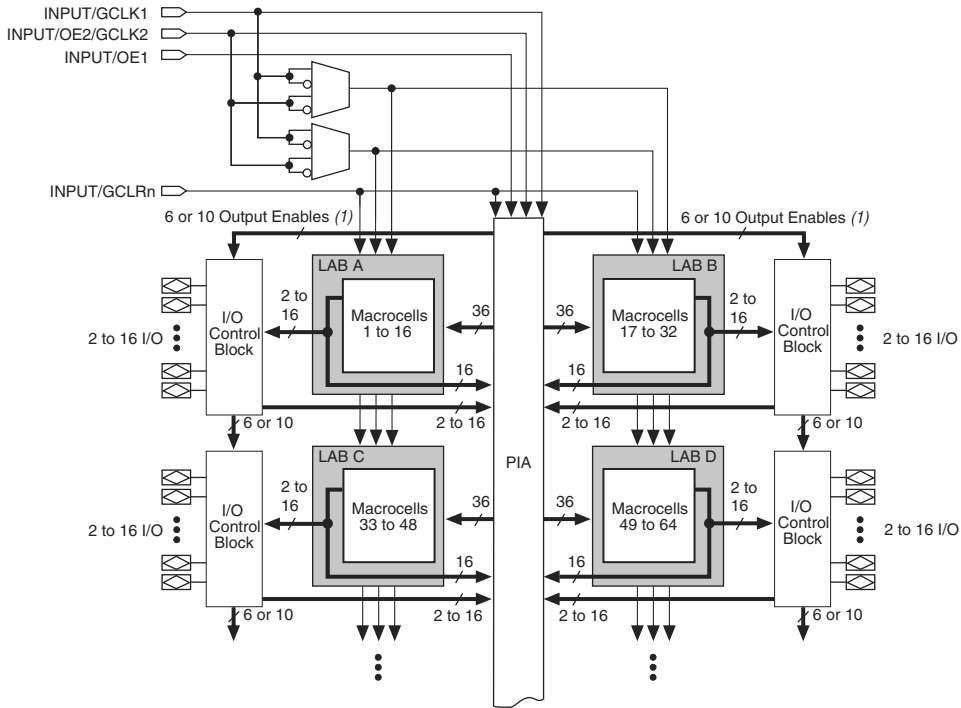
Table 3. MAX 3000A Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA
EPM3032A	34	34				
EPM3064A	34	34	66			
EPM3128A			80	96		98
EPM3256A				116	158	161
EPM3512A					172	208

Note:

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

MAX 3000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 3000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debugging cycles, and can be programmed and erased up to 100 times.

Figure 1. MAX 3000A Device Block Diagram**Note:**

- (1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

Logic Array Blocks

The MAX 3000A device architecture is based on the linking of high-performance LABs. LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

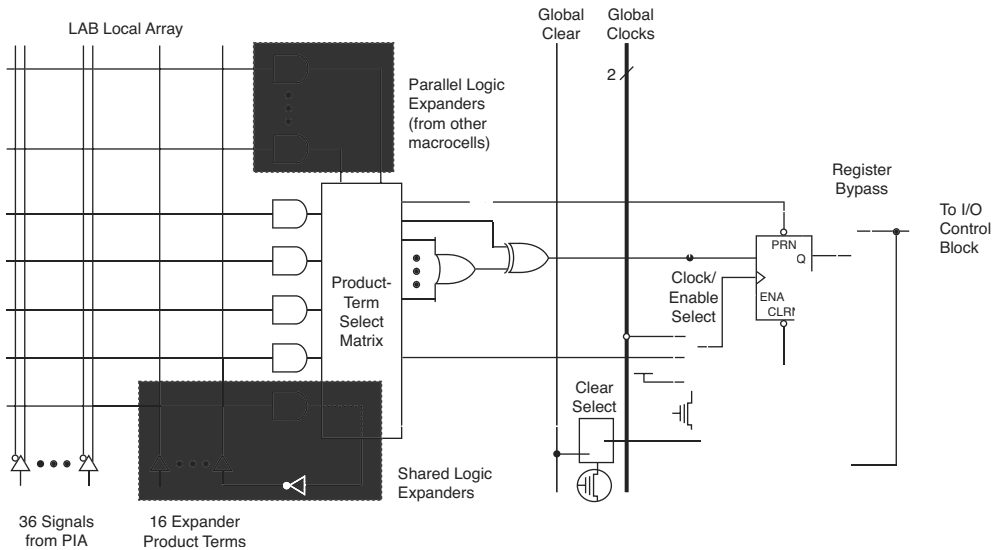
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions

Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product-term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

Figure 2. MAX 3000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development system software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal mode, which achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 3000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the two global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn).

All registers are cleared upon power-up. By default, all registered outputs drive low when the device is powered up. You can set the registered outputs to drive high upon power-up through the Quartus® II software. Quartus II software uses the NOT Gate Push-Back method, which uses an additional macrocell to set the output high. To set this in the Quartus II software, go to the Assignment Editor and set the **Power-Up Level** assignment for the register to **High**.

Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, highly complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 3000A architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shareable expanders incur a small delay (t_{SEXP}). Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 3000A Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.

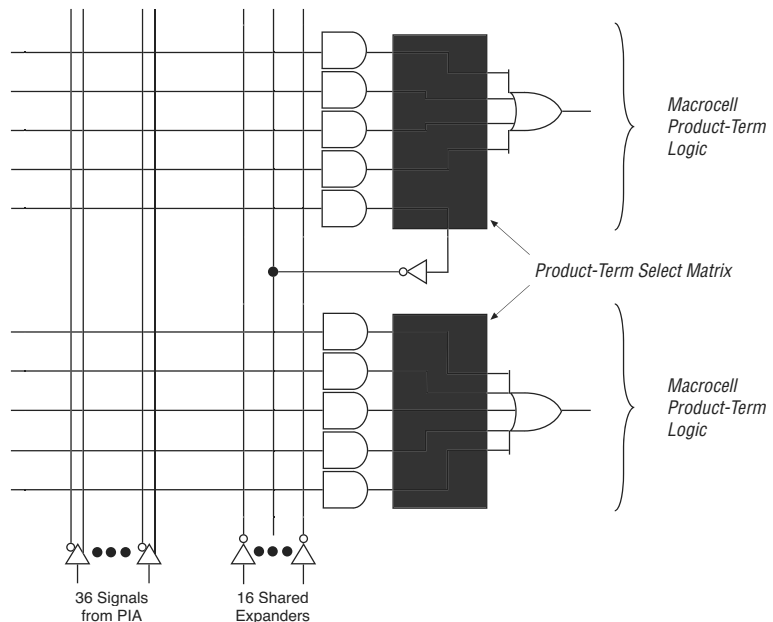
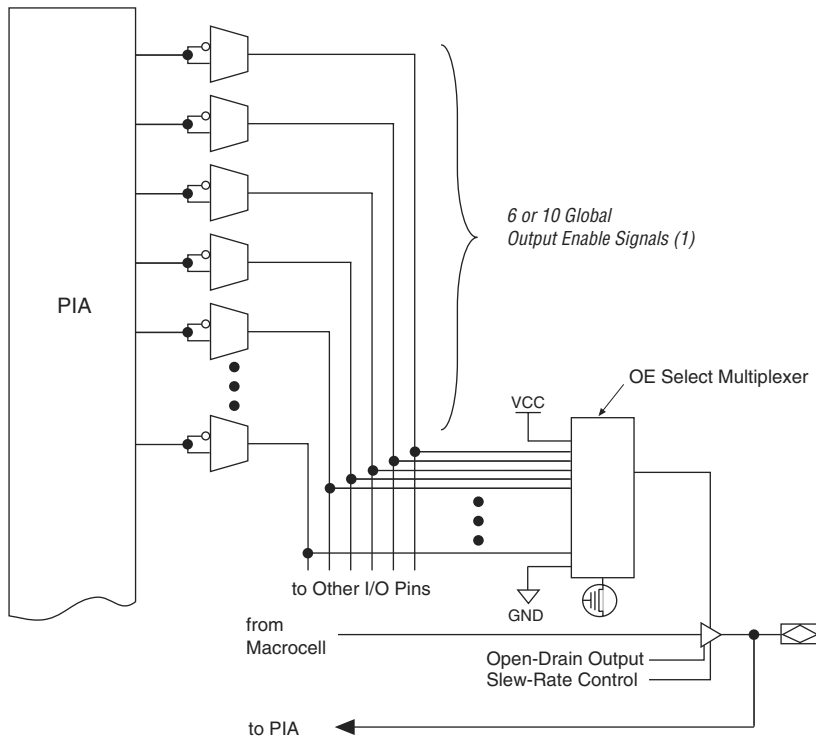


Figure 6. I/O Control Block of MAX 3000A Devices

**Note:**

- (1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance), and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC} , the output is enabled.

The MAX 3000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability

MAX 3000A devices can be programmed in-system via an industry-standard four-pin IEEE Std. 1149.1-1990 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The MAX 3000A architecture internally generates the high programming voltages required to program its EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

MAX 3000A devices have an enhanced ISP algorithm for faster programming. These devices also offer an `ISP_Done` bit that ensures safe operation when in-system programming is interrupted. This `ISP_Done` bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board (PCB) with standard pick-and-place equipment before they are programmed. MAX 3000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the MasterBlaster communications cable, the ByteBlasterMV parallel port download cable, and the BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 3000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

The Jam STAPL programming and test language can be used to program MAX 3000A devices with in-circuit testers, PCs, or embedded processors.



For more information on using the Jam STAPL programming and test language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)*, *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)* and *AN 111 (Embedded Programming Using the 8051 and Jam Byte-Code)*.

The ISP circuitry in MAX 3000A devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 3000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 3000A Device

The time required to program a single MAX 3000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 3000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Programming with External Hardware

MAX 3000A devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.



For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera software can use text- or waveform-format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

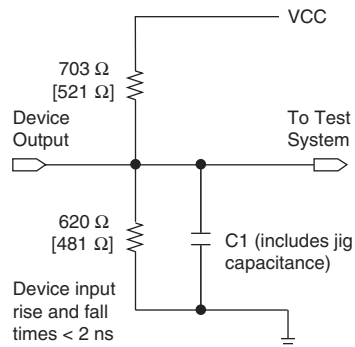
MAX 3000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1–1990. Table 7 describes the JTAG instructions supported by MAX 3000A devices. The pin-out tables found on the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 7. MAX 3000A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO
ISP Instructions	These instructions are used when programming MAX 3000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster cable, or when using a Jam STAPL file, JBC file, or SVF file via an embedded processor or test equipment

Figure 8. MAX 3000A AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V devices or outputs.



Operating Conditions

Tables 12 through 15 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for MAX 3000A devices.

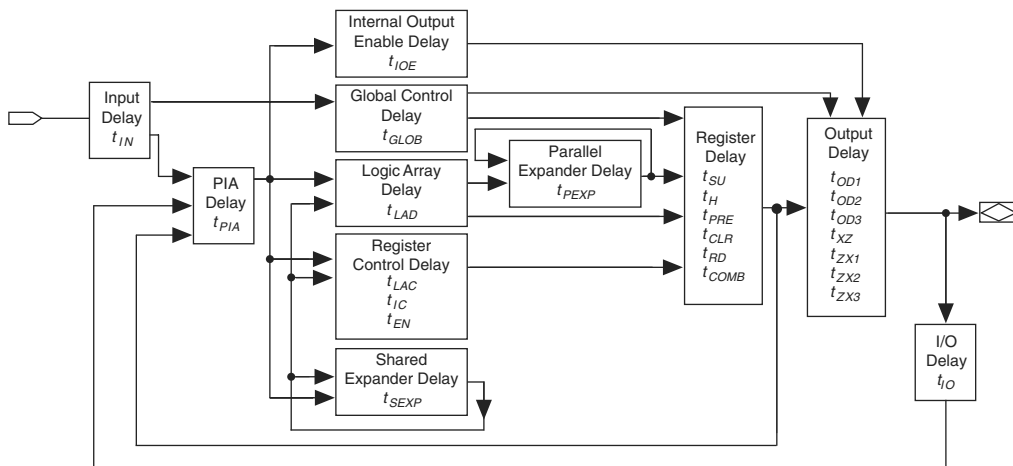
Table 12. MAX 3000A Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	-0.5	4.6	V
V_I	DC input voltage		-2.0	5.75	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	°C
T_A	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	PQFP and TQFP packages, under bias		135	°C

Timing Model

MAX 3000A device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 3000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 10. MAX 3000A Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the timing relationship between internal and external delay parameters.

Tables 16 through 23 show EPM3032A, EPM3064A, EPM3128A, EPM3256A, and EPM3512A timing information.

Table 16. EPM3032A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non–registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{PD2}	I/O input to non–registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t _{SU}	Global clock setup time	(2)	2.9		4.7		6.3		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.6		2.5		3.6		ns
t _{AH}	Array clock hold time	(2)	0.3		0.5		0.5		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t _{ACNT}	Minimum array clock period	(2)		4.4		7.2		9.7	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

Table 17. EPM3032A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
t_{PIA}	PIA delay	(2)		0.9		1.5		2.1	ns
t_{LPA}	Low-power adder	(5)		2.5		4.0		5.0	ns

Table 18. EPM3064A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10.0	ns
t _{SU}	Global clock setup time	(2)	2.8		4.7		6.2		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.1	1.0	5.1	1.0	7.0	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.6		2.6		3.6		ns
t _{AH}	Array clock hold time	(2)	0.3		0.4		0.6		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.6	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		4.5		7.4		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	222.2		135.1		100.0		MHz
t _{ACNT}	Minimum array clock period	(2)		4.5		7.4		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	222.2		135.1		100.0		MHz

Table 19. EPM3064A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t_{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.5		2.5		3.2	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.9		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{RD}	Register delay			0.7		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.9		2.5	ns
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			1.0		1.5		2.2	ns
t_{PRE}	Register preset time			1.3		2.1		2.9	ns

Table 22. EPM3256A External Timing Parameters Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
t _{CNT}	Minimum global clock period	(2)		7.9		10.5	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	126.6		95.2		MHz
t _{ACNT}	Minimum array clock period	(2)		7.9		10.5	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	126.6		95.2		MHz

Table 23. EPM3256A Internal Timing Parameters (Part 1 of 2) Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.9		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.9		1.2	ns
t_{SEXP}	Shared expander delay			2.8		3.7	ns
t_{PEXP}	Parallel expander delay			0.5		0.6	ns
t_{LAD}	Logic array delay			2.2		2.8	ns
t_{LAC}	Logic control array delay			1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		5.5	ns

Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t_{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$		6.0		6.5	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0	ns
t_{SU}	Register setup time		2.1		3.0		ns
t_H	Register hold time		0.6		0.8		ns
t_{FSU}	Register setup time of fast input		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		ns
t_{RD}	Register delay			1.3		1.7	ns
t_{COMB}	Combinatorial delay			0.6		0.8	ns
t_{IC}	Array clock delay			1.8		2.3	ns
t_{EN}	Register enable time			1.0		1.3	ns
t_{GLOB}	Global control delay			1.7		2.2	ns
t_{PRE}	Register preset time			1.0		1.4	ns
t_{CLR}	Register clear time			1.0		1.4	ns
t_{PIA}	PIA delay	(2)		3.0		4.0	ns
t_{LPA}	Low-power adder	(5)		4.5		5.0	ns

Notes to tables:

- These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.
- These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX} , in MHz) for MAX 3000A devices is calculated with the following equation:

$$P = P_{\text{INT}} + P_{\text{IO}} = I_{\text{CCINT}} \times V_{\text{CC}} + P_{\text{IO}}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{\text{CCINT}} =$$

$$(A \times \text{MC}_{\text{TON}}) + [B \times (\text{MC}_{\text{DEV}} - \text{MC}_{\text{TON}})] + (C \times \text{MC}_{\text{USED}} \times f_{\text{MAX}} \times \text{tog}_{\text{LC}})$$

The parameters in the I_{CCINT} equation are:

- MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the Quartus II or MAX+PLUS II Report File (.rpt)
- MC_{DEV} = Number of macrocells in the device
- MC_{USED} = Total number of macrocells in the design, as reported in the RPT File
- f_{MAX} = Highest clock frequency to the device
- tog_{LC} = Average percentage of logic cells toggling at each clock (typically 12.5%)
- A, B, C = Constants (shown in Table 26)

Table 26. MAX 3000A I_{CC} Equation Constants

Device	A	B	C
EPM3032A	0.71	0.30	0.014
EPM3064A	0.71	0.30	0.014
EPM3128A	0.71	0.30	0.014
EPM3256A	0.71	0.30	0.014
EPM3512A	0.71	0.30	0.014

The I_{CCINT} calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figures 12 and 13 show the typical supply current versus frequency for MAX 3000A devices.

Figure 17. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.

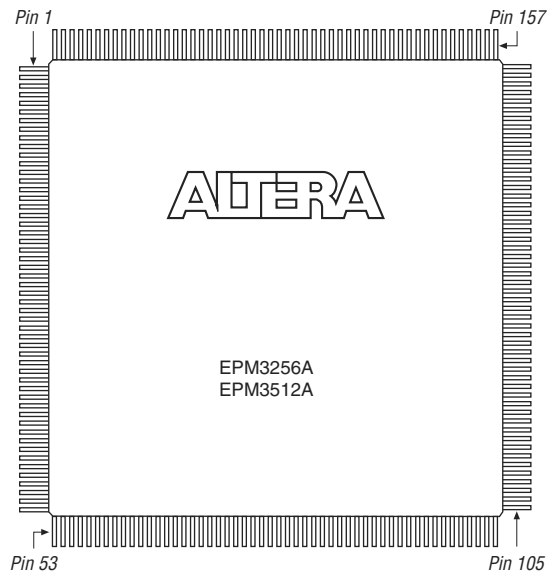
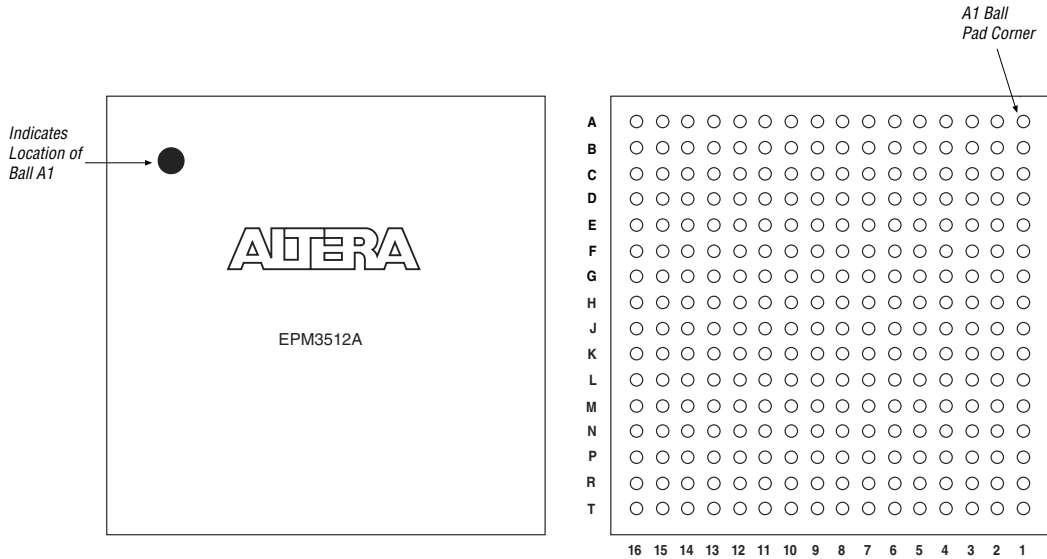


Figure 18. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5 supersedes information published in previous versions. The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5:

Version 3.5

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5:

- New paragraph added before “Expander Product Terms”.

Version 3.4

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.4:

- Updated Table 1.