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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	66
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm3064atc100-7">https://www.e-xfl.com/product-detail/intel/epm3064atc100-7</a>

**Table 2. MAX 3000A Speed Grades**

Device	Speed Grade				
	-4	-5	-6	-7	-10
EPM3032A	✓			✓	✓
EPM3064A	✓			✓	✓
EPM3128A		✓		✓	✓
EPM3256A				✓	✓
EPM3512A				✓	✓

The MAX 3000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density small-scale integration (SSI), medium-scale integration (MSI), and large-scale integration (LSI) logic functions. The MAX 3000A architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 3000A devices are available in a wide range of packages, including PLCC, PQFP, and TQFP packages. See Table 3.

**Table 3. MAX 3000A Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA
EPM3032A	34	34				
EPM3064A	34	34	66			
EPM3128A			80	96		98
EPM3256A				116	158	161
EPM3512A					172	208

**Note:**

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

MAX 3000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 3000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debugging cycles, and can be programmed and erased up to 100 times.

MAX 3000A devices contain 32 to 512 macrocells, combined into groups of 16 macrocells called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with shareable expander and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 3000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 3000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 3000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5-V, 3.3-V, and 5.0-V tolerant, allowing MAX 3000A devices to be used in mixed-voltage systems.

MAX 3000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The MAX 3000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array (PIA)
- I/O control blocks

The MAX 3000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 3000A devices.

### *Parallel Expanders*

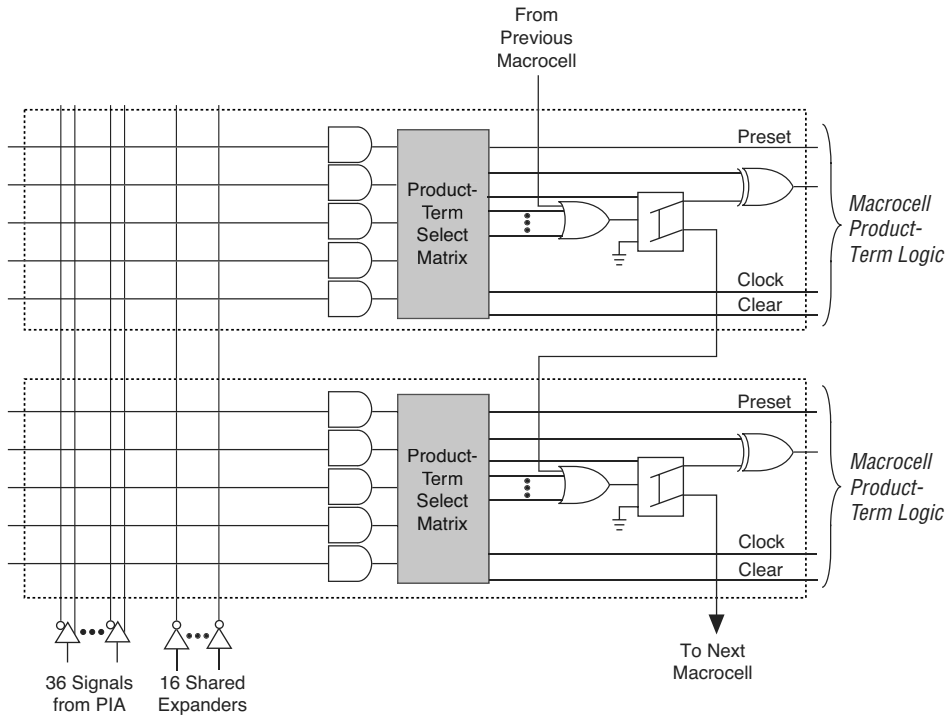
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

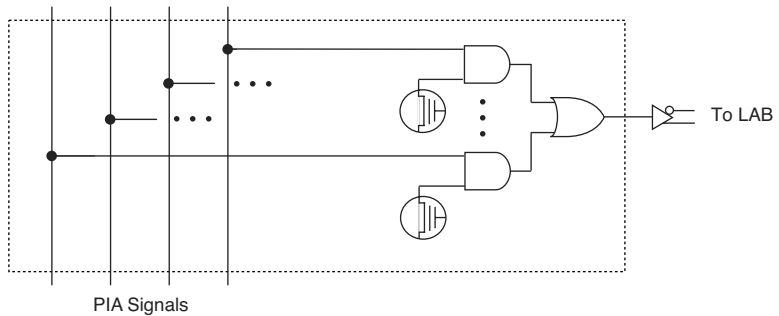
**Figure 4. MAX 3000A Parallel Expanders**

*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



## Programmable Interconnect Array

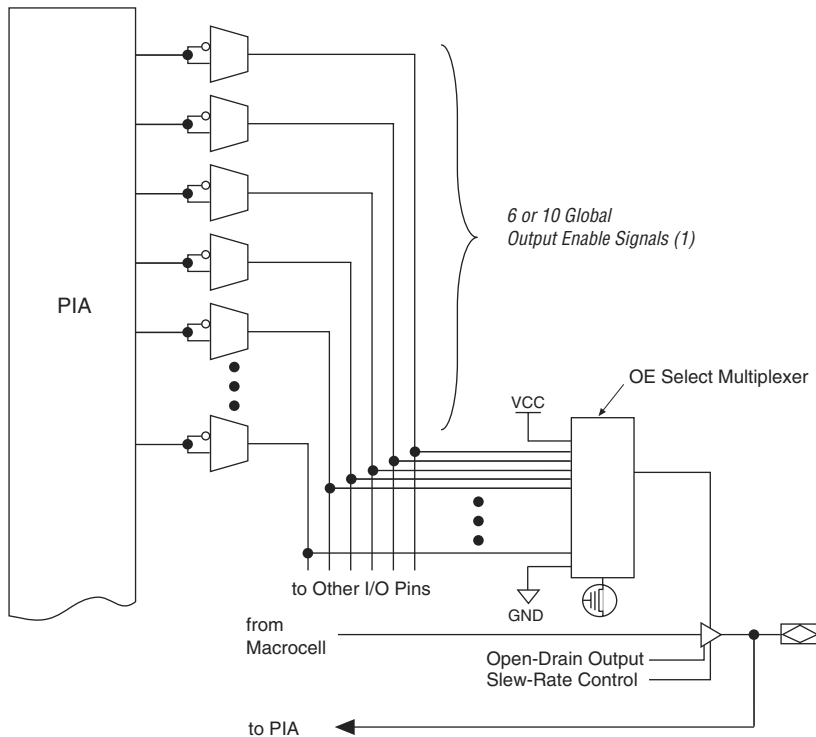
Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

**Figure 5. MAX 3000A PIA Routing**

While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 3000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

### I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or  $V_{CC}$ . Figure 6 shows the I/O control block for MAX 3000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

**Figure 6. I/O Control Block of MAX 3000A Devices****Note:**

- (1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance), and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

The MAX 3000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Figure 7 shows the timing information for the JTAG signals.

**Figure 7. MAX 3000A JTAG Waveforms**

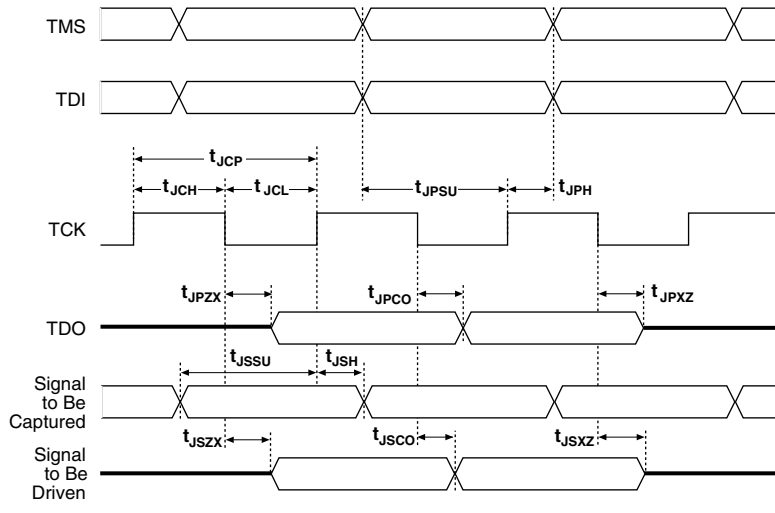


Table 10 shows the JTAG timing parameters and values for MAX 3000A devices.

<b>Table 10. JTAG Timing Parameters &amp; Values for MAX 3000A Devices</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns



## Open-Drain Output Option

MAX 3000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Open-drain output pins on MAX 3000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high  $V_{IH}$ . When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V, thereby meeting CMOS requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

## Slew-Rate Control

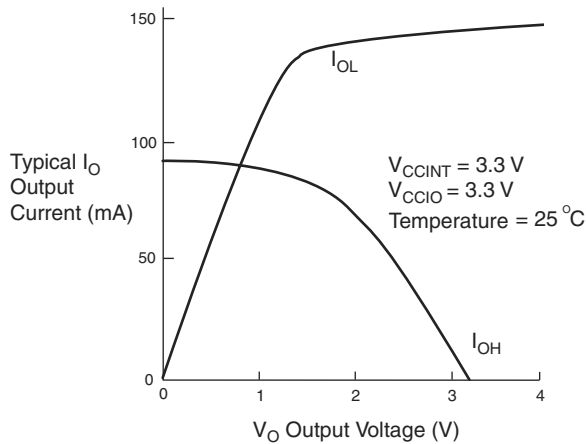
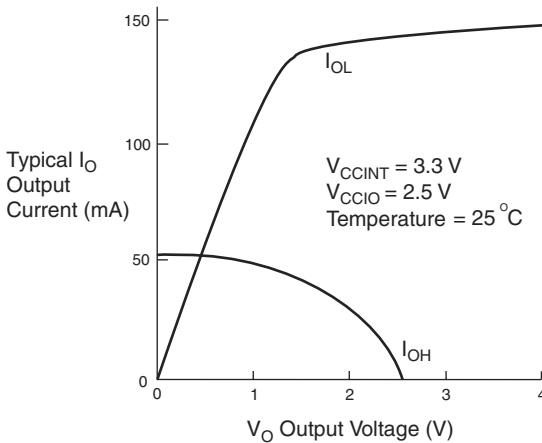
The output buffer for each MAX 3000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

## Design Security

All MAX 3000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

MAX 3000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 8. Test patterns can be used and then erased during early stages of the production flow.

**Figure 9. Output Drive Characteristics of MAX 3000A Devices****3.3 V****2.5 V**

## Power Sequencing & Hot-Socketing

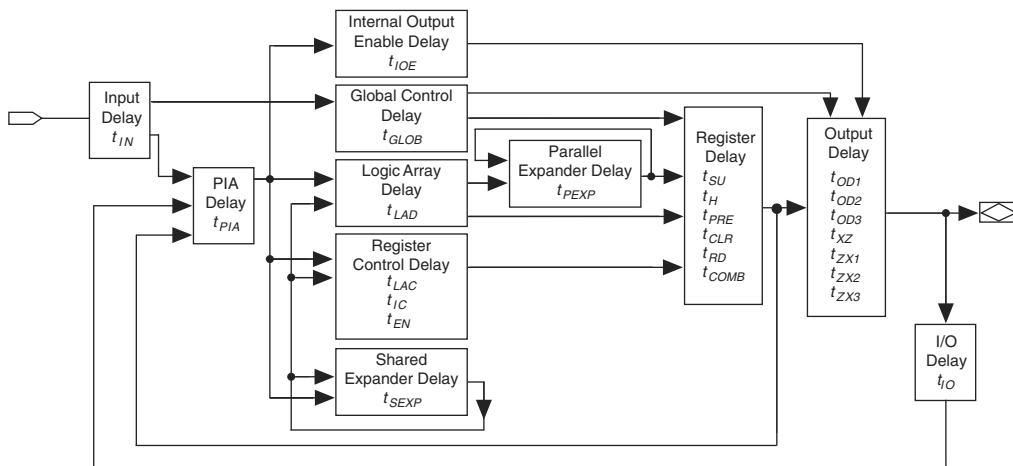
Because MAX 3000A devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into MAX 3000A devices before and during power-up without damaging the device. In addition, MAX 3000A devices do not drive out during power-up. Once operating conditions are reached, MAX 3000A devices operate as specified by the user.

## Timing Model

MAX 3000A device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 3000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

**Figure 10. MAX 3000A Timing Model**



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the timing relationship between internal and external delay parameters.

Tables 16 through 23 show EPM3032A, EPM3064A, EPM3128A, EPM3256A, and EPM3512A timing information.

**Table 16. EPM3032A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non–registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t <sub>PD2</sub>	I/O input to non–registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.9		4.7		6.3		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.6		2.5		3.6		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.3		0.5		0.5		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		4.4		7.2		9.7	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

**Table 17. EPM3032A Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		1.2		1.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		1.2		1.5	ns
$t_{SEXP}$	Shared expander delay			1.9		3.1		4.0	ns
$t_{PEXP}$	Parallel expander delay			0.5		0.8		1.0	ns
$t_{LAD}$	Logic array delay			1.5		2.5		3.3	ns
$t_{LAC}$	Logic control array delay			0.6		1.0		1.2	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.3		1.8		2.3	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.3		2.0		2.8		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{RD}$	Register delay			0.7		1.2		1.5	ns
$t_{COMB}$	Combinatorial delay			0.6		1.0		1.3	ns
$t_{IC}$	Array clock delay			1.2		2.0		2.5	ns
$t_{EN}$	Register enable time			0.6		1.0		1.2	ns
$t_{GLOB}$	Global control delay			0.8		1.3		1.9	ns
$t_{PRE}$	Register preset time			1.2		1.9		2.6	ns
$t_{CLR}$	Register clear time			1.2		1.9		2.6	ns

**Table 20. EPM3128A External Timing Parameters** Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			−5		−7		−10		
			Min	Max	Min	Max	Min	Max	
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	192.3		129.9		98.0		MHz

**Table 21. EPM3128A Internal Timing Parameters (Part 1 of 2)** Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		1.0		1.4	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		1.0		1.4	ns
$t_{SEXP}$	Shared expander delay			2.0		2.9		3.8	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.7		0.9	ns
$t_{LAD}$	Logic array delay			1.6		2.4		3.1	ns
$t_{LAC}$	Logic control array delay			0.7		1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.2		1.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.3		1.7		2.1	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns

**Table 21. EPM3128A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−5		−7		−10		
			Min	Max	Min	Max	Min	Max	
$t_{SU}$	Register setup time		1.4		2.1		2.9		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{RD}$	Register delay			0.8		1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.5		0.9		1.3	ns
$t_{IC}$	Array clock delay			1.2		1.7		2.2	ns
$t_{EN}$	Register enable time			0.7		1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.1		1.6		2.0	ns
$t_{PRE}$	Register preset time			1.4		2.0		2.7	ns
$t_{CLR}$	Register clear time			1.4		2.0		2.7	ns
$t_{PIA}$	PIA delay	(2)		1.4		2.0		2.6	ns
$t_{LPA}$	Low-power adder	(5)		4.0		4.0		5.0	ns

**Table 22. EPM3256A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		7.5		10	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		7.5		10	ns
t <sub>SU</sub>	Global clock setup time	(2)	5.2		6.9		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	4.8	1.0	6.4	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	2.7		3.6		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.3		0.5		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	7.3	1.0	9.7	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	3.0		4.0		ns

**Table 23. EPM3256A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0	ns
$t_{SU}$	Register setup time		2.1		2.9		ns
$t_H$	Register hold time		0.9		1.2		ns
$t_{RD}$	Register delay			1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.8		1.2	ns
$t_{IC}$	Array clock delay			1.6		2.1	ns
$t_{EN}$	Register enable time			1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.5		2.0	ns
$t_{PRE}$	Register preset time			2.3		3.0	ns
$t_{CLR}$	Register clear time			2.3		3.0	ns
$t_{PIA}$	PIA delay	(2)		2.4		3.2	ns
$t_{LPA}$	Low-power adder	(5)		4.0		5.0	ns

**Table 24. EPM3512A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	5.6		7.6		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	2.5		3.5		ns



**Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.5	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0	ns
$t_{SU}$	Register setup time		2.1		3.0		ns
$t_H$	Register hold time		0.6		0.8		ns
$t_{FSU}$	Register setup time of fast input		1.6		1.6		ns
$t_{FH}$	Register hold time of fast input		1.4		1.4		ns
$t_{RD}$	Register delay			1.3		1.7	ns
$t_{COMB}$	Combinatorial delay			0.6		0.8	ns
$t_{IC}$	Array clock delay			1.8		2.3	ns
$t_{EN}$	Register enable time			1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.7		2.2	ns
$t_{PRE}$	Register preset time			1.0		1.4	ns
$t_{CLR}$	Register clear time			1.0		1.4	ns
$t_{PIA}$	PIA delay	(2)		3.0		4.0	ns
$t_{LPA}$	Low-power adder	(5)		4.5		5.0	ns

**Notes to tables:**

- These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.
- These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{\text{MAX}}$ , in MHz) for MAX 3000A devices is calculated with the following equation:

$$P = P_{\text{INT}} + P_{\text{IO}} = I_{\text{CCINT}} \times V_{\text{CC}} + P_{\text{IO}}$$

The  $P_{\text{IO}}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The  $I_{\text{CCINT}}$  value depends on the switching frequency and the application logic. The  $I_{\text{CCINT}}$  value is calculated with the following equation:

$$I_{\text{CCINT}} =$$

$$(A \times \text{MC}_{\text{TON}}) + [B \times (\text{MC}_{\text{DEV}} - \text{MC}_{\text{TON}})] + (C \times \text{MC}_{\text{USED}} \times f_{\text{MAX}} \times \text{tog}_{\text{LC}})$$

The parameters in the  $I_{\text{CCINT}}$  equation are:

- $\text{MC}_{\text{TON}}$  = Number of macrocells with the Turbo Bit™ option turned on, as reported in the Quartus II or MAX+PLUS II Report File (.rpt)
- $\text{MC}_{\text{DEV}}$  = Number of macrocells in the device
- $\text{MC}_{\text{USED}}$  = Total number of macrocells in the design, as reported in the RPT File
- $f_{\text{MAX}}$  = Highest clock frequency to the device
- $\text{tog}_{\text{LC}}$  = Average percentage of logic cells toggling at each clock (typically 12.5%)
- A, B, C = Constants (shown in Table 26)

**Table 26. MAX 3000A  $I_{\text{CC}}$  Equation Constants**

Device	A	B	C
EPM3032A	0.71	0.30	0.014
EPM3064A	0.71	0.30	0.014
EPM3128A	0.71	0.30	0.014
EPM3256A	0.71	0.30	0.014
EPM3512A	0.71	0.30	0.014

The  $I_{\text{CCINT}}$  calculation provides an  $I_{\text{CC}}$  estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual  $I_{\text{CC}}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figures 12 and 13 show the typical supply current versus frequency for MAX 3000A devices.

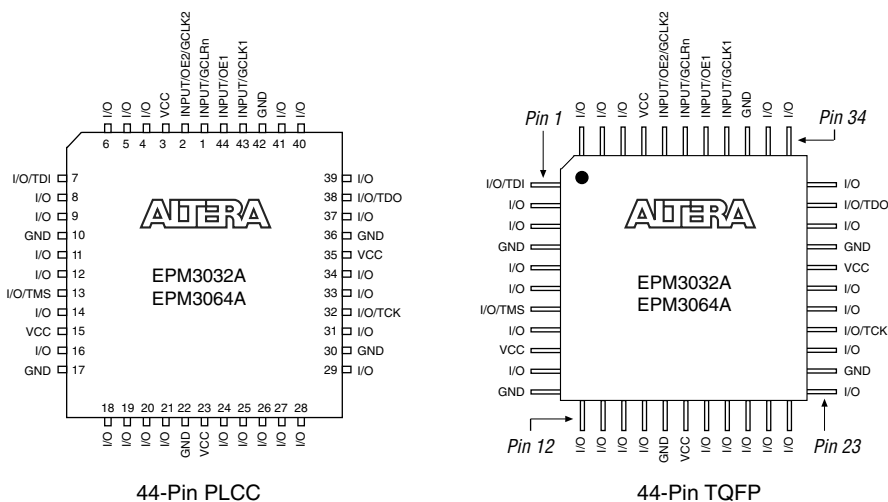
## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 14 through 18 show the package pin-out diagrams for MAX 3000A devices.

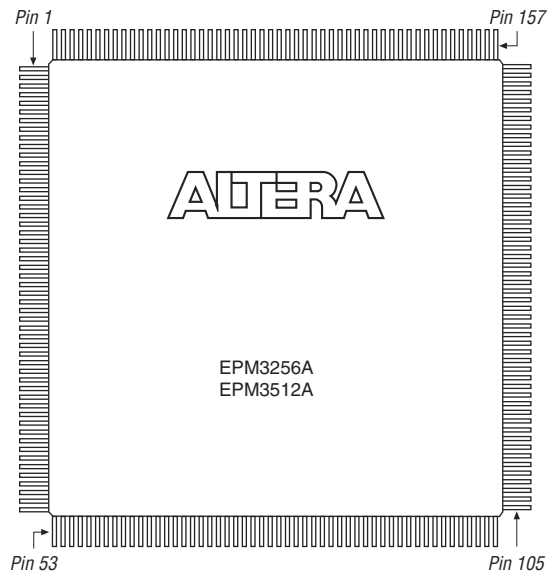
**Figure 14. 44-Pin PLCC/TQFP Package Pin-Out Diagram**

*Package outlines not drawn to scale.*



**Figure 17. 208-Pin PQFP Package Pin-Out Diagram**

*Package outline not drawn to scale.*



### Version 3.3

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.3:

- Updated Tables 3, 13, and 26.
- Added Tables 4 through 6.
- Updated Figures 12 and 13.
- Added “Programming Sequence” on page 14 and “Programming Times” on page 14

### Version 3.2

The following change were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.2:

- Updated the EPM3512 I<sub>CC</sub> versus frequency graph in Figure 13.

### Version 3.1

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.1:

- Updated timing information in Table 1 for the EPM3256A device.
- Updated *Note (10)* of Table 15.

### Version 3.0

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.0:

- Added EPM3512A device.
- Updated Tables 2 and 3.

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