Intel - EPM3064ATC44-10 Datasheet





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Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	34
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm3064atc44-10

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Figure 1. MAX 3000A Device Block Diagram

Note:

(1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

Logic Array Blocks

The MAX 3000A device architecture is based on the linking of high–performance LABs. LABs consist of 16–macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions

Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, highly complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 3000A architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shareable expanders incur a small delay (t_{SEXP}). Figure 3 shows how shareable expanders can feed multiple macrocells.





Shareable expanders can be shared by any or all macrocells in an LAB.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower–numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest–numbered macrocell can only lend parallel expanders and the highest–numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 3000A Parallel Expanders



Unused product terms in a macrocell can be allocated to a neighboring macrocell.

Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

In–System Programmability

MAX 3000A devices can be programmed in–system via an industry– standard four–pin IEEE Std. 1149.1-1990 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The MAX 3000A architecture internally generates the high programming voltages required to program its EEPROM cells, allowing in–system programming with only a single 3.3–V power supply. During in–system programming, the I/O pins are tri–stated and weakly pulled–up to eliminate board conflicts. The pull–up value is nominally 50 kΩ

MAX 3000A devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that ensures safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board (PCB) with standard pick–and–place equipment before they are programmed. MAX 3000A devices can be programmed by downloading the information via in–circuit testers, embedded processors, the MasterBlaster communications cable, the ByteBlasterMV parallel port download cable, and the BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high–pin–count packages (e.g., QFP packages) due to device handling. MAX 3000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

The Jam STAPL programming and test language can be used to program MAX 3000A devices with in–circuit testers, PCs, or embedded processors.



For more information on using the Jam STAPL programming and test language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor), Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)* and *AN 111 (Embedded Programming Using the 8051 and Jam Byte-Code).*

The ISP circuitry in MAX 3000A devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 3000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

- 1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
- 2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
- 3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
- 4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
- 5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
- 6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary–scan register length and device IDCODE information for MAX 3000A devices.

Table 8. MAX 3000A Boundary–Scan Register Length							
Device	Boundary–Scan Register Length						
EPM3032A	96						
EPM3064A	192						
EPM3128A	288						
EPM3256A	480						
EPM3512A	624						

Table 9. 32-Bit MAX 3000A Device IDCODE Value Note (1)									
Device		IDCODE (32 bits)							
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)					
EPM3032A	0001	0111 0000 0011 0010	00001101110	1					
EPM3064A	0001	0111 0000 0110 0100	00001101110	1					
EPM3128A	0001	0111 0001 0010 1000	00001101110	1					
EPM3256A	0001	0111 0010 0101 0110	00001101110	1					
EPM3512A	0001	0111 0101 0001 0010	00001101110	1					

Notes:

(1) The most significant bit (MSB) is on the left.

(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See *Application Note* 39 (IEEE 1149.1 (JTAG) Boundary–Scan Testing in Altera Devices) for more information on JTAG BST.

Figure 8. MAX 3000A AC Test Conditions



Operating Conditions

Tables 12 through 15 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for MAX 3000A devices.

Table 1	Table 12. MAX 3000A Device Absolute Maximum RatingsNote (1)							
Symbol	Parameter	Conditions	Min	Max	Unit			
V _{CC}	Supply voltage	With respect to ground (2)	-0.5	4.6	V			
VI	DC input voltage		-2.0	5.75	V			
I _{OUT}	DC output current, per pin		-25	25	mA			
T _{STG}	Storage temperature	No bias	-65	150	°C			
T _A	Ambient temperature	Under bias	-65	135	°C			
TJ	Junction temperature	PQFP and TQFP packages, under bias		135	°C			

Timing Model

MAX 3000A device timing can be analyzed with the Altera software, with a variety of popular industry–standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 3000A devices have predictable internal delays that enable the designer to determine the worst–case timing of any design. The software provides timing simulation, point–to–point delay prediction, and detailed timing analysis for device–wide performance evaluation.



Figure 10. MAX 3000A Timing Model

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin–to–pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the timing relationship between internal and external delay parameters.

Figure 11. MAX 3000A Switching Waveforms



Symbol	Parameter	Conditions			Speed	Grade			Unit
			-	-4	-	-7	_	10	
			Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.7		1.2		1.5	ns
t _{IO}	I/O input pad and buffer delay			0.7		1.2		1.5	ns
t _{SEXP}	Shared expander delay			1.9		3.1		4.0	ns
t _{PEXP}	Parallel expander delay			0.5		0.8		1.0	ns
t _{LAD}	Logic array delay			1.5		2.5		3.3	ns
t _{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t _{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		0.8		1.3		1.8	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF		1.3		1.8		2.3	ns
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.8		6.3		6.8	ns
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0	ns
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF		4.5		4.5		5.5	ns
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		9.0		9.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t _{SU}	Register setup time		1.3		2.0		2.8		ns
t _H	Register hold time		0.6		1.0		1.3		ns
t _{RD}	Register delay			0.7		1.2		1.5	ns
t _{COMB}	Combinatorial delay			0.6		1.0		1.3	ns
t _{IC}	Array clock delay			1.2		2.0		2.5	ns
t _{EN}	Register enable time			0.6		1.0		1.2	ns
t _{GLOB}	Global control delay			0.8		1.3		1.9	ns
t _{PRE}	Register preset time			1.2		1.9		2.6	ns
t _{CLR}	Register clear time			1.2		1.9		2.6	ns

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Table 17. EPM3032A Internal Timing Parameters (Part 2 of 2) Note (1)									
Symbol	Parameter	Conditions		Speed Grade					Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{PIA}	PIA delay	(2)		0.9		1.5		2.1	ns
t _{LPA}	Low-power adder	(5)		2.5		4.0		5.0	ns

Table 18. EPM3064A External Timing Parameters Note (1)

Symbol	Parameter	Conditions			Speed	Grade			Unit
			_	4	-	7		10	
			Min	Мах	Min	Max	Min	Max	
t _{PD1}	Input to non–registered output	C1 = 35 pF <i>(2)</i>		4.5		7.5		10.0	ns
t _{PD2}	I/O input to non–registered output	C1 = 35 pF <i>(2)</i>		4.5		7.5		10.0	ns
t _{SU}	Global clock setup time	(2)	2.8		4.7		6.2		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.1	1.0	5.1	1.0	7.0	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.6		2.6		3.6		ns
t _{AH}	Array clock hold time	(2)	0.3		0.4		0.6		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF <i>(2)</i>	1.0	4.3	1.0	7.2	1.0	9.6	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		4.5		7.4		10.0	ns
f _{сnт}	Maximum internal global clock frequency	(2), (4)	222.2		135.1		100.0		MHz
t _{ACNT}	Minimum array clock period	(2)		4.5		7.4		10.0	ns
facnt	Maximum internal array clock frequency	(2), (4)	222.2		135.1		100.0		MHz

Symbol	Parameter	Conditions			Snood	Grado			Unit
Symbol	Falailletei	Conuntions			oheen	uraue			Unit
				-4	-	-7	-	10	
			Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t _{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t _{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t _{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t _{LAD}	Logic array delay			1.5		2.5		3.2	ns
t _{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t _{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off V _{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF		1.3		1.8		2.3	ns
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5 V \text{ or } 3.3 V$	C1 = 35 pF		5.8		6.3		6.8	ns
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		4.0		5.0	ns
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF		4.5		4.5		5.5	ns
t _{ZX3}	Output buffer enable delay, slow slew rate = on V _{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t _{SU}	Register setup time		1.3		2.0		2.9		ns
t _H	Register hold time		0.6		1.0		1.3		ns
t _{RD}	Register delay			0.7		1.2		1.6	ns
t _{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t _{IC}	Array clock delay			1.2		1.9		2.5	ns
t _{EN}	Register enable time			0.6		1.0		1.2	ns
t _{GLOB}	Global control delay			1.0		1.5		2.2	ns
t _{PRE}	Register preset time			1.3		2.1		2.9	ns

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Table 19. EPM3064A Internal Timing Parameters (Part 2 of 2) Note (1)									
Symbol	Parameter	Conditions		Speed Grade					
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t _{CLR}	Register clear time			1.3		2.1		2.9	ns
t _{PIA}	PIA delay	(2)		1.0		1.7		2.3	ns
t _{LPA}	Low-power adder	(5)		3.5		4.0		5.0	ns

 Table 20. EPM3128A External Timing Parameters
 Note (1)

Symbol	Parameter	Conditions			Speed	Grade			Unit
			_	5	-	7		10	
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non– registered output	C1 = 35 pF <i>(2)</i>		5.0		7.5		10	ns
t _{PD2}	I/O input to non– registered output	C1 = 35 pF <i>(2)</i>		5.0		7.5		10	ns
t _{SU}	Global clock setup time	(2)	3.3		4.9		6.6		ns
t _H	Global clock hold time	(2)	0.0		0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.4	1.0	5.0	1.0	6.6	ns
t _{CH}	Global clock high time		2.0		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		3.0		4.0		ns
t _{ASU}	Array clock setup time	(2)	1.8		2.8		3.8		ns
t _{AH}	Array clock hold time	(2)	0.2		0.3		0.4		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF <i>(2)</i>	1.0	4.9	1.0	7.1	1.0	9.4	ns
t _{ACH}	Array clock high time		2.0		3.0		4.0		ns
t _{ACL}	Array clock low time		2.0		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		5.2		7.7		10.2	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	192.3		129.9		98.0		MHz
t _{ACNT}	Minimum array clock period	(2)		5.2		7.7		10.2	ns

Table 24. EPM3512A External Timing Parameters Note (1)							
Symbol	Parameter	Conditions		Speed	Grade		Unit
			-	-7		10	
			Min	Max	Min	Max	
t _{AH}	Array clock hold time	(2)	0.2		0.3		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF <i>(2)</i>	1.0	7.8	1.0	10.4	ns
t _{ACH}	Array clock high time		3.0		4.0		ns
t _{ACL}	Array clock low time		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		4.0		ns
t _{CNT}	Minimum global clock period	(2)		8.6		11.5	ns
f _{CNT}	Maximum internal global clock frequency	(2), (4)	116.3		87.0		MHz
t _{ACNT}	Minimum array clock period	(2)		8.6		11.5	ns
f _{ACNT}	Maximum internal array clock frequency	(2), (4)	116.3		87.0		MHz

Table 25. EPM3512A Internal Timing Parameters (Part 1 of 2)	Note (1)	

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.7		0.9	ns
t _{IO}	I/O input pad and buffer delay			0.7		0.9	ns
t _{FIN}	Fast input delay			3.1		3.6	ns
t _{SEXP}	Shared expander delay			2.7		3.5	ns
t _{PEXP}	Parallel expander delay			0.4		0.5	ns
t _{LAD}	Logic array delay			2.2		2.8	ns
t _{LAC}	Logic control array delay			1.0		1.3	ns
t _{IOE}	Internal output enable delay			0.0		0.0	ns
t _{OD1}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		1.0		1.5	ns
t _{OD2}	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF		1.5		2.0	ns

Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2) Note (1)											
Symbol	Parameter	Conditions	Speed Grade				Unit				
			-7		-10		-				
			Min	Max	Min	Max					
t _{OD3}	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5$ V or 3.3 V	C1 = 35 pF		6.0		6.5	ns				
t _{ZX1}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF		4.0		5.0	ns				
t _{ZX2}	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5 V$	C1 = 35 pF		4.5		5.5	ns				
t _{ZX3}	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3 V$	C1 = 35 pF		9.0		10.0	ns				
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0	ns				
t _{SU}	Register setup time		2.1		3.0		ns				
t _H	Register hold time		0.6		0.8		ns				
t _{FSU}	Register setup time of fast input		1.6		1.6		ns				
t _{FH}	Register hold time of fast input		1.4		1.4		ns				
t _{RD}	Register delay			1.3		1.7	ns				
t _{COMB}	Combinatorial delay			0.6		0.8	ns				
t _{IC}	Array clock delay			1.8		2.3	ns				
t _{EN}	Register enable time			1.0		1.3	ns				
t _{GLOB}	Global control delay			1.7		2.2	ns				
t _{PRE}	Register preset time			1.0		1.4	ns				
t _{CLR}	Register clear time			1.0		1.4	ns				
t _{PIA}	PIA delay	(2)		3.0		4.0	ns				
t _{LPA}	Low-power adder	(5)		4.5		5.0	ns				

Notes to tables:

- These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.
- (2) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in low–power mode.

Figure 12. I_{CC} vs. Frequency for MAX 3000A Devices

100

80 60

40

20

0

50

Typical I_{CC} Active (mA)



High Speed

200

250

- 108.7 MHz

Low Power

Frequency (MHz)

150

100

Device Pin–Outs

See the Altera web site (http://www.altera.com) or the *Altera Digital Library* for pin–out information.

Figures 14 through 18 show the package pin–out diagrams for MAX 3000A devices.



Package outlines not drawn to scale.



Figure 18. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5 supersedes information published in previous versions. The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5:

Version 3.5

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5:

■ New paragraph added before "Expander Product Terms".

Version 3.4

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.4:

Updated Table 1.

Version 3.3

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.3:

- Updated Tables 3, 13, and 26.
- Added Tables 4 through 6.
- Updated Figures 12 and 13.
- Added "Programming Sequence" on page 14 and "Programming Times" on page 14

Version 3.2

The following change were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.2:

■ Updated the EPM3512 I_{CC} versus frequency graph in Figure 13.

Version 3.1

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.1:

- Updated timing information in Table 1 for the EPM3256A device.
- Updated *Note (10)* of Table 15.

Version 3.0

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.0:

- Added EPM3512A device.
- Updated Tables 2 and 3.

101 Innovation Drive San Jose, CA 95134 (408) 544-7000 http://www.altera.com Applications Hotline: (800) 800-EPLD Customer Marketing: (408) 544-7104 Literature Services: lit_reg@altera.com

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