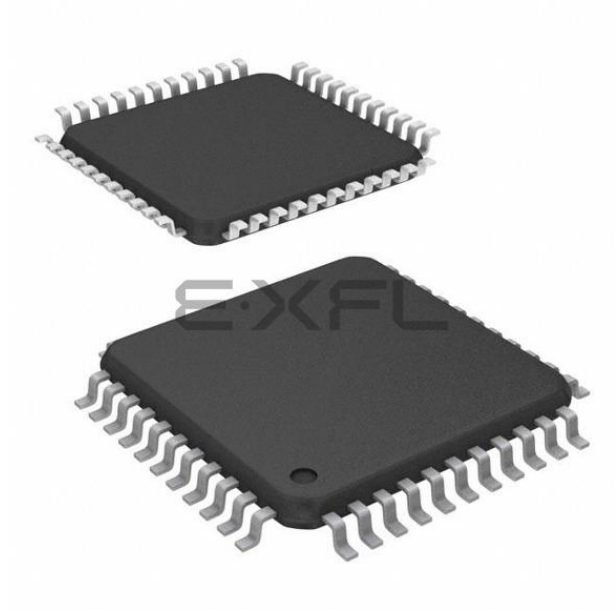

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 4 |
| Number of Macrocells | 64 |
| Number of Gates | 1250 |
| Number of I/O | 34 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm3064atc44-7n |

## …and More Features

- PCI compatible
- Bus–friendly architecture including programmable slew–rate control
- Open–drain output option
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power–saving mode for a power reduction of over 50% in each macrocell
- Configurable expander product–term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- Enhanced architectural features, including:
  - 6 or 10 pin– or logic–driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Programmable output slew–rate control
- Software design support and automatic place–and–route provided by Altera's development systems for Windows–based PCs and Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from third–party manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with the Altera master programming unit (MPU), MasterBlaster™ communications cable, ByteBlasterMV™ parallel port download cable, BitBlaster™ serial download cable as well as programming hardware from third–party manufacturers and any in–circuit tester that supports Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**), Jam STAPL Byte-Code Files (**.jbc**), or Serial Vector Format Files (**.svf**)

## General Description

MAX 3000A devices are low–cost, high–performance devices based on the Altera MAX architecture. Fabricated with advanced CMOS technology, the EEPROM–based MAX 3000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 3000A devices in the –4, –5, –6, –7, and –10 speed grades are compatible with the timing requirements of the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 2.

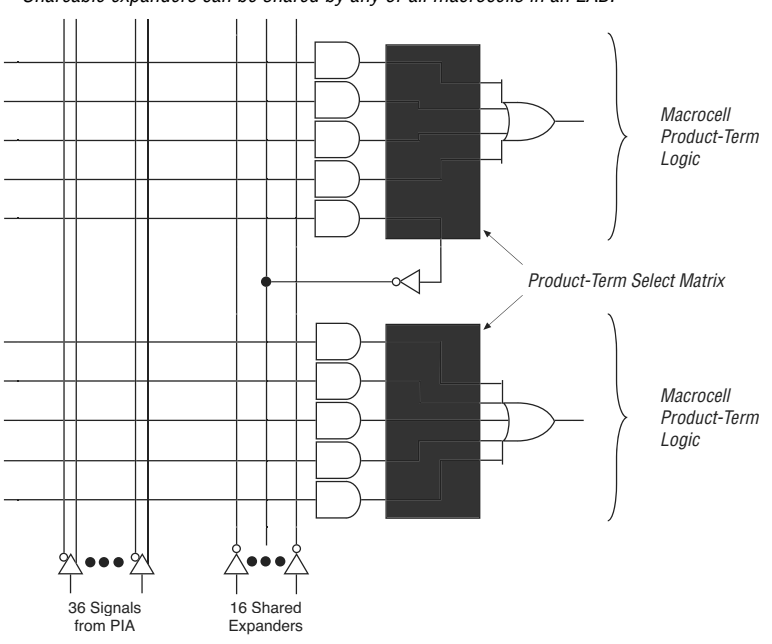
## Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, highly complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 3000A architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

### *Shareable Expanders*

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shareable expanders incur a small delay ($t_{SEXP}$). Figure 3 shows how shareable expanders can feed multiple macrocells.

***Figure 3. MAX 3000A Shareable Expanders***



### *Parallel Expanders*

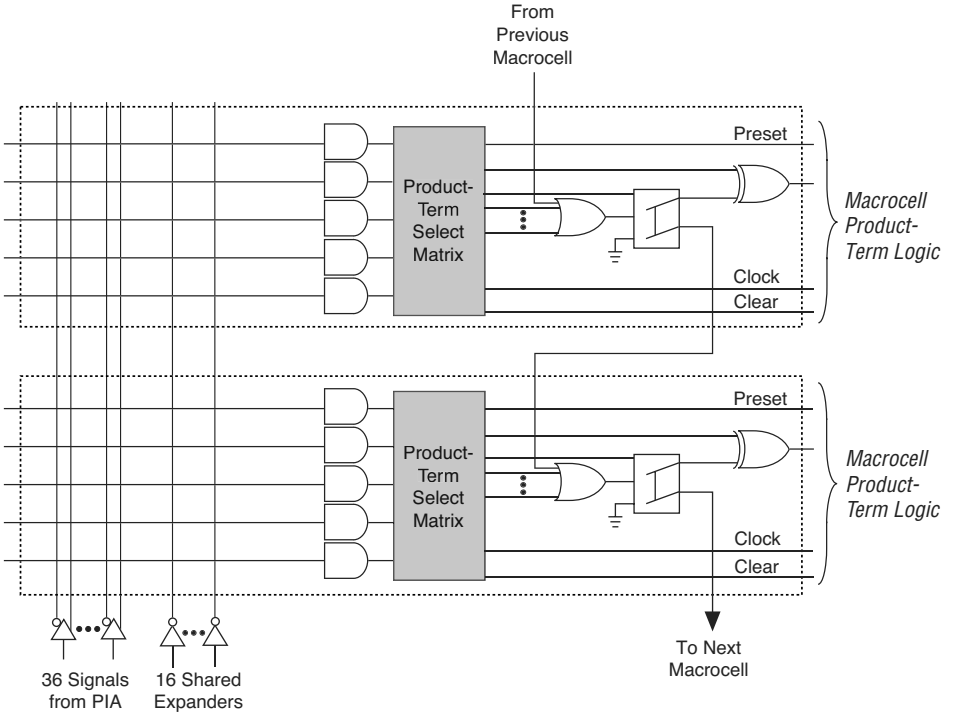
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower–numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest–numbered macrocell can only lend parallel expanders and the highest–numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

*Figure 4. MAX 3000A Parallel Expanders*

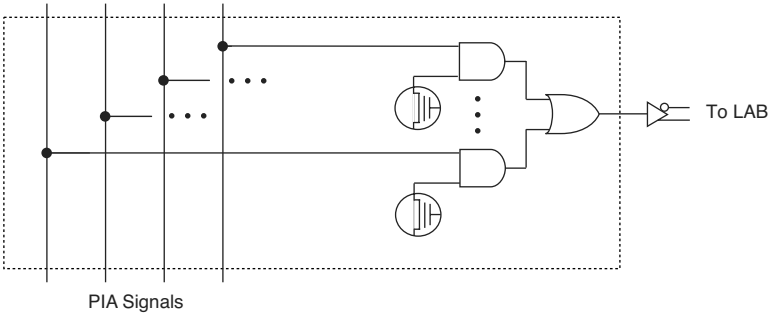
*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*




## Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

*Figure 5. MAX 3000A PIA Routing*

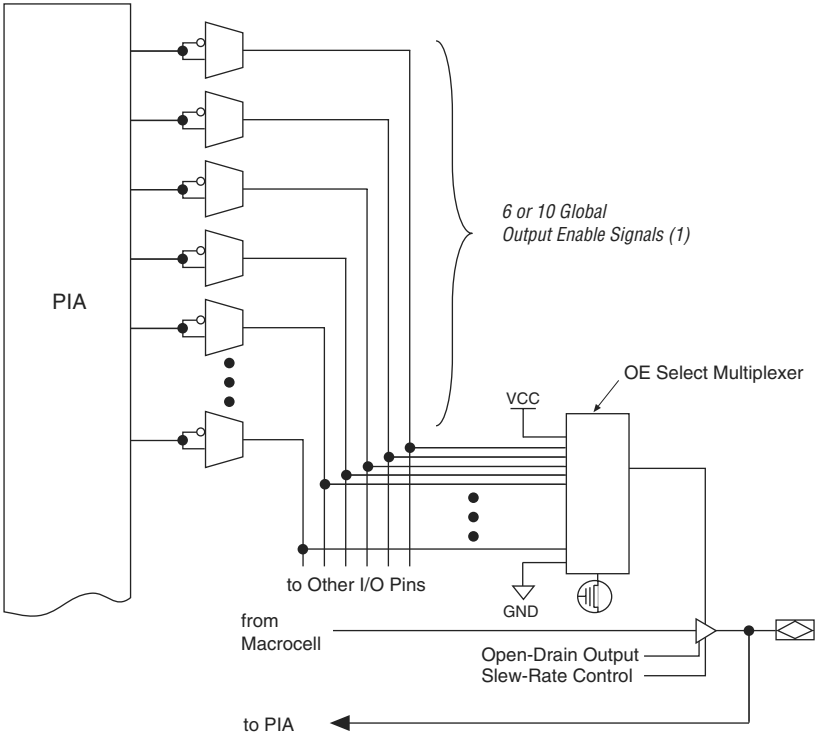



While the routing delays of channel–based routing schemes in masked or FPGAs are cumulative, variable, and path–dependent, the MAX 3000A PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri–state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or $V_{CC}$. Figure 6 shows the I/O control block for MAX 3000A devices. The I/O control block has 6 or 10 global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

*Figure 6. I/O Control Block of MAX 3000A Devices*




*Note:*
(1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

When the tri–state buffer control is connected to ground, the output is tri-stated (high impedance), and the I/O pin can be used as a dedicated input. When the tri–state buffer control is connected to $V_{CC}$, the output is enabled.

The MAX 3000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## In–System Programmability

MAX 3000A devices can be programmed in–system via an industry–standard four–pin IEEE Std. 1149.1-1990 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The MAX 3000A architecture internally generates the high programming voltages required to program its EEPROM cells, allowing in–system programming with only a single 3.3–V power supply. During in–system programming, the I/O pins are tri–stated and weakly pulled–up to eliminate board conflicts. The pull–up value is nominally 50 kΩ

MAX 3000A devices have an enhanced ISP algorithm for faster programming. These devices also offer an `ISP_Done` bit that ensures safe operation when in–system programming is interrupted. This `ISP_Done` bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board (PCB) with standard pick–and–place equipment before they are programmed. MAX 3000A devices can be programmed by downloading the information via in–circuit testers, embedded processors, the MasterBlaster communications cable, the ByteBlasterMV parallel port download cable, and the BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high–pin–count packages (e.g., QFP packages) due to device handling. MAX 3000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

The Jam STAPL programming and test language can be used to program MAX 3000A devices with in–circuit testers, PCs, or embedded processors.

For more information on using the Jam STAPL programming and test language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)*, *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)* and *AN 111 (Embedded Programming Using the 8051 and Jam Byte-Code)*.

The ISP circuitry in MAX 3000A devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

The programming times described in Tables 4 through 6 are associated with the worst-case method using the enhanced ISP algorithm.

*Table 4. MAX 3000A $t_{PULSE}$ & $Cycle_{TCK}$ Values*

| Device | Programming | | Stand-Alone Verification | |
|---|---|---|---|---|
| | $t_{PPULSE}$ (s) | $Cycle_{PTCK}$ | $t_{VPULSE}$ (s) | $Cycle_{VTCK}$ |
| EPM3032A | 2.00 | 55,000 | 0.002 | 18,000 |
| EPM3064A | 2.00 | 105,000 | 0.002 | 35,000 |
| EPM3128A | 2.00 | 205,000 | 0.002 | 68,000 |
| EPM3256A | 2.00 | 447,000 | 0.002 | 149,000 |
| EPM3512A | 2.00 | 890,000 | 0.002 | 297,000 |

Tables 5 and 6 show the in-system programming and stand alone verification times for several common test clock frequencies.

*Table 5. MAX 3000A In-System Programming Times for Different Test Clock Frequencies*

| Device | $f_{TCK}$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM3032A | 2.01 | 2.01 | 2.03 | 2.06 | 2.11 | 2.28 | 2.55 | 3.10 | s |
| EPM3064A | 2.01 | 2.02 | 2.05 | 2.11 | 2.21 | 2.53 | 3.05 | 4.10 | s |
| EPM3128A | 2.02 | 2.04 | 2.10 | 2.21 | 2.41 | 3.03 | 4.05 | 6.10 | s |
| EPM3256A | 2.05 | 2.09 | 2.23 | 2.45 | 2.90 | 4.24 | 6.47 | 10.94 | s |
| EPM3512A | 2.09 | 2.18 | 2.45 | 2.89 | 3.78 | 6.45 | 10.90 | 19.80 | s |

*Table 6. MAX 3000A Stand-Alone Verification Times for Different Test Clock Frequencies*

| Device | $f_{TCK}$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM3032A | 0.00 | 0.01 | 0.01 | 0.02 | 0.04 | 0.09 | 0.18 | 0.36 | s |
| EPM3064A | 0.01 | 0.01 | 0.02 | 0.04 | 0.07 | 0.18 | 0.35 | 0.70 | s |
| EPM3128A | 0.01 | 0.02 | 0.04 | 0.07 | 0.14 | 0.34 | 0.68 | 1.36 | s |
| EPM3256A | 0.02 | 0.03 | 0.08 | 0.15 | 0.30 | 0.75 | 1.49 | 2.98 | s |
| EPM3512A | 0.03 | 0.06 | 0.15 | 0.30 | 0.60 | 1.49 | 2.97 | 5.94 | s |

The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary–scan register length and device IDCODE information for MAX 3000A devices.

*Table 8. MAX 3000A Boundary–Scan Register Length*

| Device | Boundary–Scan Register Length |
|---|---|
| EPM3032A | 96 |
| EPM3064A | 192 |
| EPM3128A | 288 |
| EPM3256A | 480 |
| EPM3512A | 624 |

*Table 9. 32–Bit MAX 3000A Device IDCODE Value* *Note (1)*

| Device | IDCODE (32 bits) | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer's Identity (11 Bits) | 1 (1 Bit) *(2)* |
| EPM3032A | 0001 | 0111 0000 0011 0010 | 00001101110 | 1 |
| EPM3064A | 0001 | 0111 0000 0110 0100 | 00001101110 | 1 |
| EPM3128A | 0001 | 0111 0001 0010 1000 | 00001101110 | 1 |
| EPM3256A | 0001 | 0111 0010 0101 0110 | 00001101110 | 1 |
| EPM3512A | 0001 | 0111 0101 0001 0010 | 00001101110 | 1 |

*Notes:*
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary–Scan Testing in Altera Devices)* for more information on JTAG BST.

Figure 7 shows the timing information for the JTAG signals.

*Figure 7. MAX 3000A JTAG Waveforms*

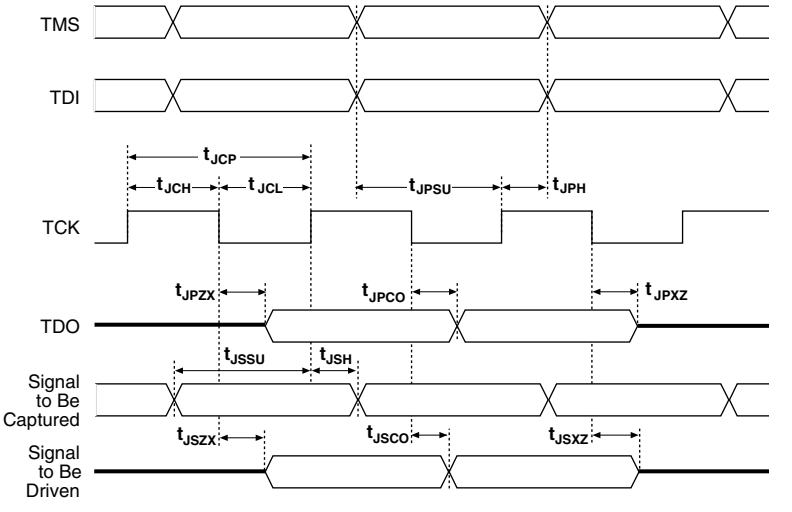



Table 10 shows the JTAG timing parameters and values for MAX 3000A devices.

*Table 10. JTAG Timing Parameters & Values for MAX 3000A Devices*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

*Table 13. MAX 3000A Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(10)* | 3.0 | 3.6 | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 3.3–V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers, 2.5–V operation | | 2.3 | 2.7 | V |
| $V_{CCISP}$ | Supply voltage during ISP | | 3.0 | 3.6 | V |
| $V_I$ | Input voltage | *(3)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | Commercial range | 0 | 70 | ° C |
| | | Industrial range | –40 | 85 | ° C |
| $T_J$ | Junction temperature | Commercial range | 0 | 90 | ° C |
| | | Industrial range *(11)* | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 14. MAX 3000A Device DC Operating Conditions* *Note (4)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High–level input voltage | | 1.7 | 5.75 | V |
| $V_{IL}$ | Low–level input voltage | | –0.5 | 0.8 | V |
| $V_{OH}$ | 3.3–V high–level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | 2.4 | | V |
| | 3.3–V high–level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | $V_{CCIO}$ – 0.2 | | V |
| | 2.5–V high–level output voltage | $I_{OH}$ = –100 µA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 1.7 | | V |
| $V_{OL}$ | 3.3–V low–level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.4 | V |
| | 3.3–V low–level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.2 | V |
| | 2.5–V low–level output voltage | $I_{OL}$ = 100 µA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.7 | V |
| $I_I$ | Input leakage current | $V_I$ = –0.5 to 5.5 V *(7)* | –10 | 10 | µA |
| $I_{OZ}$ | Tri–state output off–state current | $V_I$ = –0.5 to 5.5 V *(7)* | –10 | 10 | µA |
| $R_{ISP}$ | Value of I/O pin pull–up resistor when programming in–system or during power–up | $V_{CCIO}$ = 2.3 to 3.6 V *(8)* | 20 | 74 | kΩ |

*Table 17. EPM3032A Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –4 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.9 | | 3.1 | | 4.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.5 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.5 | | 2.5 | | 3.3 | ns |
| $t_{LAC}$ | Logic control array delay | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.8 | | 1.3 | | 1.8 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 1.3 | | 1.8 | | 2.3 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.8 | | 6.3 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.3 | | 2.0 | | 2.8 | | ns |
| $t_{H}$ | Register hold time | | 0.6 | | 1.0 | | 1.3 | | ns |
| $t_{RD}$ | Register delay | | | 0.7 | | 1.2 | | 1.5 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.6 | | 1.0 | | 1.3 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 2.0 | | 2.5 | ns |
| $t_{EN}$ | Register enable time | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{GLOB}$ | Global control delay | | | 0.8 | | 1.3 | | 1.9 | ns |
| $t_{PRE}$ | Register preset time | | | 1.2 | | 1.9 | | 2.6 | ns |
| $t_{CLR}$ | Register clear time | | | 1.2 | | 1.9 | | 2.6 | ns |

*Table 17. EPM3032A Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –4 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PIA}$ | PIA delay | *(2)* | | 0.9 | | 1.5 | | 2.1 | ns |
| $t_{LPA}$ | Low–power adder | *(5)* | | 2.5 | | 4.0 | | 5.0 | ns |

*Table 18. EPM3064A External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –4 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non–registered output | C1 = 35 pF *(2)* | | 4.5 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non–registered output | C1 = 35 pF *(2)* | | 4.5 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 2.8 | | 4.7 | | 6.2 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 3.1 | 1.0 | 5.1 | 1.0 | 7.0 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.6 | | 2.6 | | 3.6 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.3 | | 0.4 | | 0.6 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 4.3 | 1.0 | 7.2 | 1.0 | 9.6 | ns |
| $t_{ACH}$ | Array clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 4.5 | | 7.4 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(4)* | 222.2 | | 135.1 | | 100.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 4.5 | | 7.4 | | 10.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(4)* | 222.2 | | 135.1 | | 100.0 | | MHz |

*Table 19. EPM3064A Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –4 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.6 | | 1.1 | | 1.4 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.6 | | 1.1 | | 1.4 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 1.8 | | 3.0 | | 3.9 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.7 | | 0.9 | ns |
| $t_{LAD}$ | Logic array delay | | | 1.5 | | 2.5 | | 3.2 | ns |
| $t_{LAC}$ | Logic control array delay | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 0.8 | | 1.3 | | 1.8 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 1.3 | | 1.8 | | 2.3 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 5.8 | | 6.3 | | 6.8 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.3 | | 2.0 | | 2.9 | | ns |
| $t_{H}$ | Register hold time | | 0.6 | | 1.0 | | 1.3 | | ns |
| $t_{RD}$ | Register delay | | | 0.7 | | 1.2 | | 1.6 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 1.9 | | 2.5 | ns |
| $t_{EN}$ | Register enable time | | | 0.6 | | 1.0 | | 1.2 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.0 | | 1.5 | | 2.2 | ns |
| $t_{PRE}$ | Register preset time | | | 1.3 | | 2.1 | | 2.9 | ns |

*Table 23. EPM3256A Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 2.1 | | 2.9 | | ns |
| $t_{H}$ | Register hold time | | 0.9 | | 1.2 | | ns |
| $t_{RD}$ | Register delay | | | 1.2 | | 1.6 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.8 | | 1.2 | ns |
| $t_{IC}$ | Array clock delay | | | 1.6 | | 2.1 | ns |
| $t_{EN}$ | Register enable time | | | 1.0 | | 1.3 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.5 | | 2.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.3 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.3 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 2.4 | | 3.2 | ns |
| $t_{LPA}$ | Low–power adder | *(5)* | | 4.0 | | 5.0 | ns |

*Table 24. EPM3512A External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF *(2)* | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF *(2)* | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 5.6 | | 7.6 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 4.7 | 1.0 | 6.3 | ns |
| $t_{CH}$ | Global clock high time | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 2.5 | | 3.5 | | ns |

*Table 24. EPM3512A External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.3 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 7.8 | 1.0 | 10.4 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 8.6 | | 11.5 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(4)* | 116.3 | | 87.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 8.6 | | 11.5 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(4)* | 116.3 | | 87.0 | | MHz |

*Table 25. EPM3512A Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.7 | | 0.9 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.7 | | 0.9 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.1 | | 3.6 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 2.7 | | 3.5 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.5 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.2 | | 2.8 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.0 | | 1.3 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.0 | | 1.5 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 1.5 | | 2.0 | ns |

## Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 3000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The $I_{CCINT}$ value depends on the switching frequency and the application logic. The $I_{CCINT}$ value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in the $I_{CCINT}$ equation are:

| | | |
|---|---|---|
| $MC_{TON}$ | = | Number of macrocells with the Turbo Bit™ option turned on, as reported in the Quartus II or MAX+PLUS II Report File (**.rpt**) |
| $MC_{DEV}$ | = | Number of macrocells in the device |
| $MC_{USED}$ | = | Total number of macrocells in the design, as reported in the RPT File |
| $\mathbf{f_{MAX}}$ | = | Highest clock frequency to the device |
| $\mathbf{tog_{LC}}$ | = | Average percentage of logic cells toggling at each clock (typically 12.5%) |
| A, B, C | = | Constants (shown in Table 26) |

*Table 26. MAX 3000A $I_{CC}$ Equation Constants*

| Device | A | B | C |
|---|---|---|---|
| EPM3032A | 0.71 | 0.30 | 0.014 |
| EPM3064A | 0.71 | 0.30 | 0.014 |
| EPM3128A | 0.71 | 0.30 | 0.014 |
| EPM3256A | 0.71 | 0.30 | 0.014 |
| EPM3512A | 0.71 | 0.30 | 0.014 |

The $I_{CCINT}$ calculation provides an $I_{CC}$ estimate based on typical conditions using a pattern of a 16–bit, loadable, enabled, up/down counter in each LAB with no output load. Actual $I_{CC}$ should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figures 12 and 13 show the typical supply current versus frequency for MAX 3000A devices.

*Figure 12. $I_{CC}$ vs. Frequency for MAX 3000A Devices*

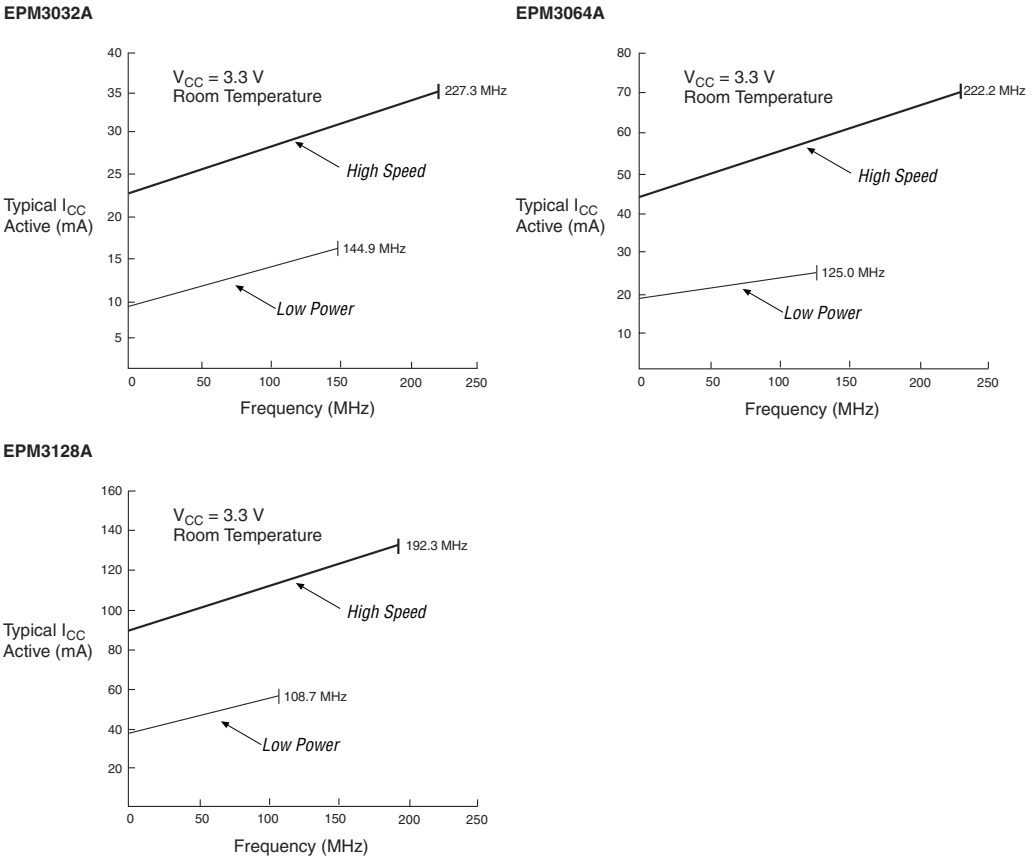


*Figure 13. $I_{CC}$ vs. Frequency for MAX 3000A Devices*

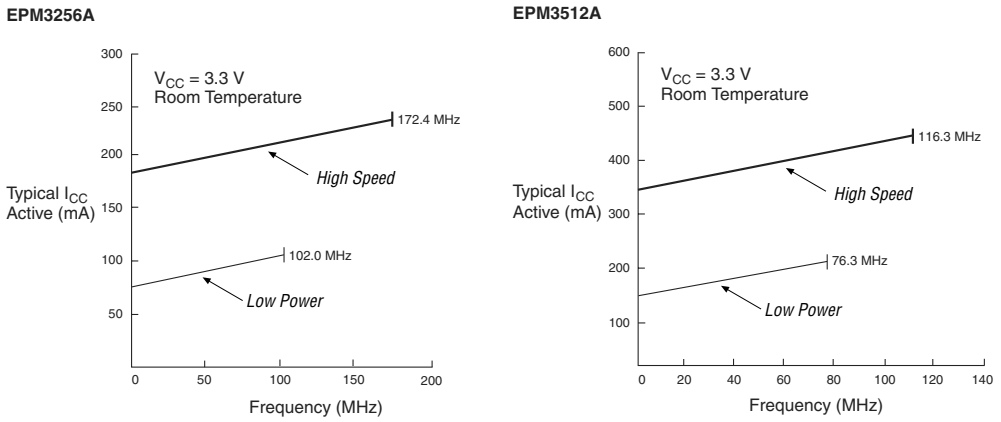


*Figure 15. 100–Pin TQFP Package Pin–Out Diagram*

*Package outline not drawn to scale.*

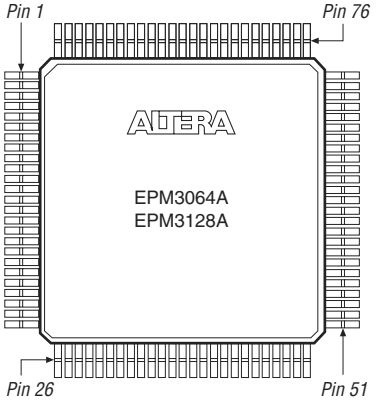



*Figure 16. 144–Pin TQFP Package Pin–Out Diagram*

*Package outline not drawn to scale.*