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### Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	80
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm3128atc100-5">https://www.e-xfl.com/product-detail/intel/epm3128atc100-5</a>

**Table 2. MAX 3000A Speed Grades**

Device	Speed Grade				
	-4	-5	-6	-7	-10
EPM3032A	✓			✓	✓
EPM3064A	✓			✓	✓
EPM3128A		✓		✓	✓
EPM3256A				✓	✓
EPM3512A				✓	✓

The MAX 3000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high-density small-scale integration (SSI), medium-scale integration (MSI), and large-scale integration (LSI) logic functions. The MAX 3000A architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 3000A devices are available in a wide range of packages, including PLCC, PQFP, and TQFP packages. See Table 3.

**Table 3. MAX 3000A Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin TQFP	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA
EPM3032A	34	34				
EPM3064A	34	34	66			
EPM3128A			80	96		98
EPM3256A				116	158	161
EPM3512A					172	208

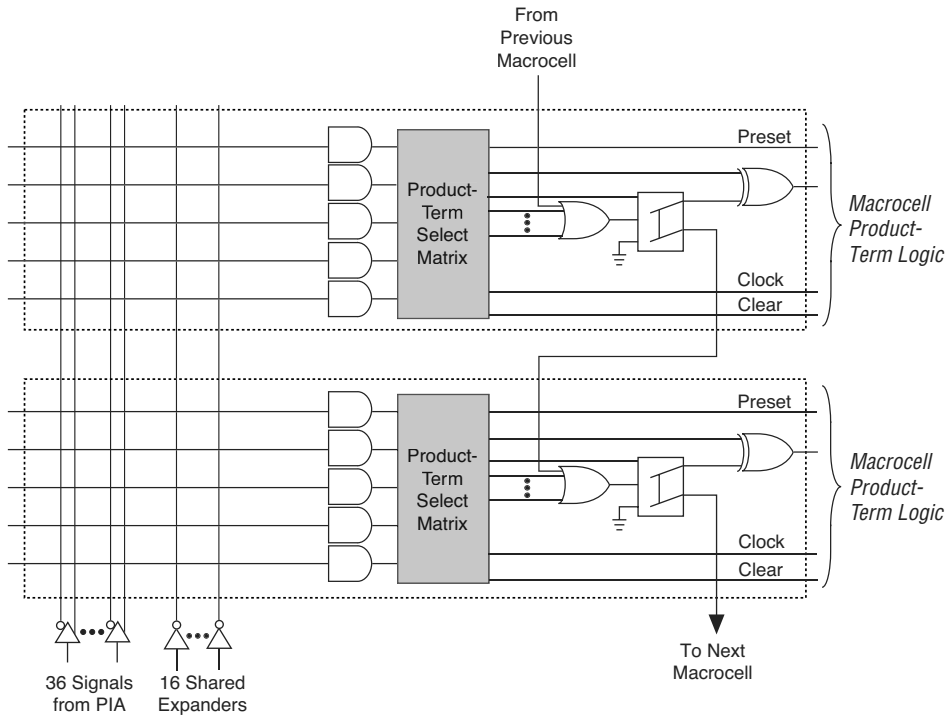
**Note:**

- (1) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

MAX 3000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 3000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debugging cycles, and can be programmed and erased up to 100 times.

**Figure 4. MAX 3000A Parallel Expanders**

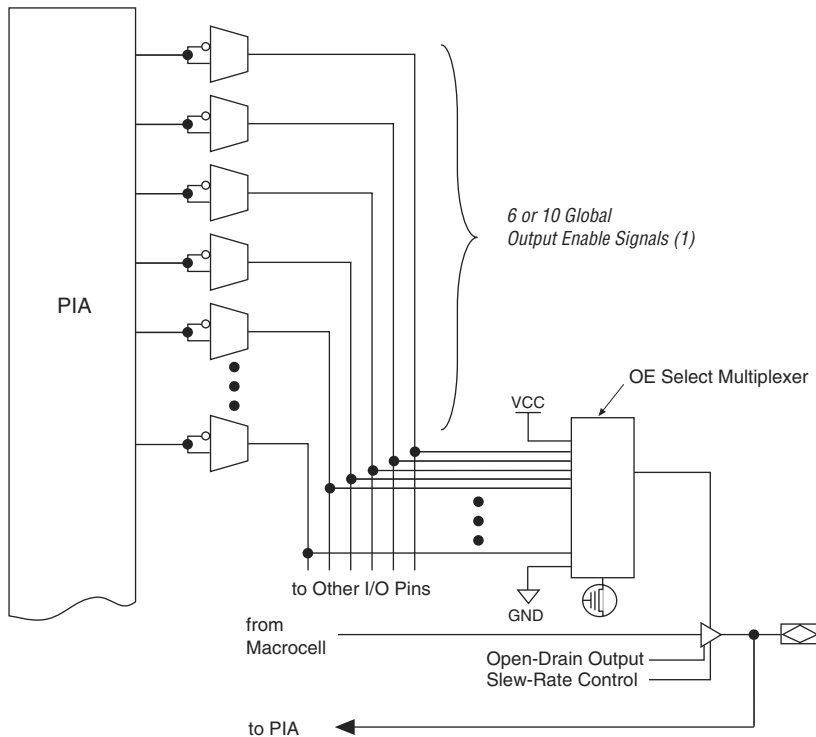
*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



## Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 6. I/O Control Block of MAX 3000A Devices

**Note:**

- (1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance), and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

The MAX 3000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## In-System Programmability

MAX 3000A devices can be programmed in-system via an industry-standard four-pin IEEE Std. 1149.1-1990 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The MAX 3000A architecture internally generates the high programming voltages required to program its EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k $\Omega$ .

MAX 3000A devices have an enhanced ISP algorithm for faster programming. These devices also offer an `ISP_Done` bit that ensures safe operation when in-system programming is interrupted. This `ISP_Done` bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board (PCB) with standard pick-and-place equipment before they are programmed. MAX 3000A devices can be programmed by downloading the information via in-circuit testers, embedded processors, the MasterBlaster communications cable, the ByteBlasterMV parallel port download cable, and the BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 3000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

The Jam STAPL programming and test language can be used to program MAX 3000A devices with in-circuit testers, PCs, or embedded processors.



For more information on using the Jam STAPL programming and test language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)*, *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)* and *AN 111 (Embedded Programming Using the 8051 and Jam Byte-Code)*.

The ISP circuitry in MAX 3000A devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary-scan register length and device IDCODE information for MAX 3000A devices.

**Table 8. MAX 3000A Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPM3032A	96
EPM3064A	192
EPM3128A	288
EPM3256A	480
EPM3512A	624

**Table 9. 32-Bit MAX 3000A Device IDCODE Value** Note (1)

Device	IDCODE (32 bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM3032A	0001	0111 0000 0011 0010	00001101110	1
EPM3064A	0001	0111 0000 0110 0100	00001101110	1
EPM3128A	0001	0111 0001 0010 1000	00001101110	1
EPM3256A	0001	0111 0010 0101 0110	00001101110	1
EPM3512A	0001	0111 0101 0001 0010	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

## Programmable Speed/Power Control

MAX 3000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 3000A device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{EN}$ ,  $t_{CPPW}$  and  $t_{SEXP}$  parameters.

## Output Configuration

MAX 3000A device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

The MAX 3000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 3000A devices to connect to systems with differing supply voltages. MAX 3000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for I/O output drivers ( $V_{CCIO}$ ).

The  $V_{CCIO}$  pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels lower than 3.0 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ . Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 11 summarizes the MAX 3000A MultiVolt I/O support.

<b>Table 11. MAX 3000A MultiVolt I/O Support</b>						
<b><math>V_{CCIO}</math> Voltage</b>	<b>Input Signal (V)</b>			<b>Output Signal (V)</b>		
	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓	✓	✓	✓

**Note:**

- (1) When  $V_{CCIO}$  is 3.3 V, a MAX 3000A device can drive a 2.5-V device that has 3.3-V tolerant inputs.

## Open-Drain Output Option

MAX 3000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Open-drain output pins on MAX 3000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high  $V_{IH}$ . When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V, thereby meeting CMOS requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

## Slew-Rate Control

The output buffer for each MAX 3000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

## Design Security

All MAX 3000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

MAX 3000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 8. Test patterns can be used and then erased during early stages of the production flow.



**Table 15. MAX 3000A Device Capacitance** Note (9)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input pin capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (4) These values are specified under the recommended operating conditions, as shown in Table 13 on page 23.
- (5) The parameter is measured with 50% of the outputs each sourcing the specified current. The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (6) The parameter is measured with 50% of the outputs each sinking the specified current. The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current.
- (7) This value is specified during normal device operation. During power-up, the maximum leakage current is  $\pm 300\text{ }\mu\text{A}$ .
- (8) This pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.
- (9) Capacitance is measured at  $25^\circ\text{ C}$  and is sample-tested only. The  $\text{OE1}$  pin (high-voltage pin during programming) has a maximum capacitance of  $20\text{ pF}$ .
- (10) The POR time for all MAX 3000A devices does not exceed  $100\text{ }\mu\text{s}$ . The sufficient  $V_{CCINT}$  voltage level for POR is  $3.0\text{ V}$ . The device is fully initialized within the POR time after  $V_{CCINT}$  reaches the sufficient POR voltage level.
- (11) These devices support in-system programming for  $-40^\circ$  to  $100^\circ\text{ C}$ . For in-system programming support between  $-40^\circ$  and  $0^\circ\text{ C}$ , contact Altera Applications.

Figure 9 shows the typical output drive characteristics of MAX 3000A devices.

Tables 16 through 23 show EPM3032A, EPM3064A, EPM3128A, EPM3256A, and EPM3512A timing information.

**Table 16. EPM3032A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non–registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t <sub>PD2</sub>	I/O input to non–registered output	C1 = 35 pF (2)		4.5		7.5		10	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.9		4.7		6.3		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.6		2.5		3.6		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.3		0.5		0.5		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.4	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		4.4		7.2		9.7	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	227.3		138.9		103.1		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		4.4		7.2		9.7	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	227.3		138.9		103.1		MHz

**Table 17. EPM3032A Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		1.2		1.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		1.2		1.5	ns
$t_{SEXP}$	Shared expander delay			1.9		3.1		4.0	ns
$t_{PEXP}$	Parallel expander delay			0.5		0.8		1.0	ns
$t_{LAD}$	Logic array delay			1.5		2.5		3.3	ns
$t_{LAC}$	Logic control array delay			0.6		1.0		1.2	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.3		1.8		2.3	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.3		2.0		2.8		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{RD}$	Register delay			0.7		1.2		1.5	ns
$t_{COMB}$	Combinatorial delay			0.6		1.0		1.3	ns
$t_{IC}$	Array clock delay			1.2		2.0		2.5	ns
$t_{EN}$	Register enable time			0.6		1.0		1.2	ns
$t_{GLOB}$	Global control delay			0.8		1.3		1.9	ns
$t_{PRE}$	Register preset time			1.2		1.9		2.6	ns
$t_{CLR}$	Register clear time			1.2		1.9		2.6	ns

**Table 17. EPM3032A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
$t_{PIA}$	PIA delay	(2)		0.9		1.5		2.1	ns
$t_{LPA}$	Low-power adder	(5)		2.5		4.0		5.0	ns

**Table 18. EPM3064A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		4.5		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	2.8		4.7		6.2		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.1	1.0	5.1	1.0	7.0	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.6		2.6		3.6		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.3		0.4		0.6		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	4.3	1.0	7.2	1.0	9.6	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		4.5		7.4		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	222.2		135.1		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		4.5		7.4		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	222.2		135.1		100.0		MHz

**Table 19. EPM3064A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
$t_{CLR}$	Register clear time			1.3		2.1		2.9	ns
$t_{PIA}$	PIA delay	(2)		1.0		1.7		2.3	ns
$t_{LPA}$	Low-power adder	(5)		3.5		4.0		5.0	ns

**Table 20. EPM3128A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−5		−7		−10		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non–registered output	C1 = 35 pF (2)		5.0		7.5		10	ns
t <sub>PD2</sub>	I/O input to non–registered output	C1 = 35 pF (2)		5.0		7.5		10	ns
t <sub>SU</sub>	Global clock setup time	(2)	3.3		4.9		6.6		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	3.4	1.0	5.0	1.0	6.6	ns
t <sub>CH</sub>	Global clock high time		2.0		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	1.8		2.8		3.8		ns
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.3		0.4		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	4.9	1.0	7.1	1.0	9.4	ns
t <sub>ACH</sub>	Array clock high time		2.0		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.0		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		5.2		7.7		10.2	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	192.3		129.9		98.0		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		5.2		7.7		10.2	ns

**Table 22. EPM3256A External Timing Parameters** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
t <sub>CNT</sub>	Minimum global clock period	(2)		7.9		10.5	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	126.6		95.2		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		7.9		10.5	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	126.6		95.2		MHz

**Table 23. EPM3256A Internal Timing Parameters (Part 1 of 2)** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.9		1.2	ns
$t_{IO}$	I/O input pad and buffer delay			0.9		1.2	ns
$t_{SEXP}$	Shared expander delay			2.8		3.7	ns
$t_{PEXP}$	Parallel expander delay			0.5		0.6	ns
$t_{LAD}$	Logic array delay			2.2		2.8	ns
$t_{LAC}$	Logic control array delay			1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.2		1.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.7		2.1	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		5.5	ns

**Table 23. EPM3256A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0	ns
$t_{SU}$	Register setup time		2.1		2.9		ns
$t_H$	Register hold time		0.9		1.2		ns
$t_{RD}$	Register delay			1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.8		1.2	ns
$t_{IC}$	Array clock delay			1.6		2.1	ns
$t_{EN}$	Register enable time			1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.5		2.0	ns
$t_{PRE}$	Register preset time			2.3		3.0	ns
$t_{CLR}$	Register clear time			2.3		3.0	ns
$t_{PIA}$	PIA delay	(2)		2.4		3.2	ns
$t_{LPA}$	Low-power adder	(5)		4.0		5.0	ns

**Table 24. EPM3512A External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF (2)		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF (2)		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time	(2)	5.6		7.6		ns
t <sub>H</sub>	Global clock hold time	(2)	0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF	1.0	4.7	1.0	6.3	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time	(2)	2.5		3.5		ns

**Table 24. EPM3512A External Timing Parameters** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.3		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	7.8	1.0	10.4	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		8.6		11.5	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	116.3		87.0		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		8.6		11.5	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	116.3		87.0		MHz

**Table 25. EPM3512A Internal Timing Parameters (Part 1 of 2)** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		0.9	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		0.9	ns
$t_{FIN}$	Fast input delay			3.1		3.6	ns
$t_{SEXP}$	Shared expander delay			2.7		3.5	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.5	ns
$t_{LAD}$	Logic array delay			2.2		2.8	ns
$t_{LAC}$	Logic control array delay			1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	C1 = 35 pF		1.0		1.5	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	C1 = 35 pF		1.5		2.0	ns



**Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.5	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		5.0	ns
$t_{SU}$	Register setup time		2.1		3.0		ns
$t_H$	Register hold time		0.6		0.8		ns
$t_{FSU}$	Register setup time of fast input		1.6		1.6		ns
$t_{FH}$	Register hold time of fast input		1.4		1.4		ns
$t_{RD}$	Register delay			1.3		1.7	ns
$t_{COMB}$	Combinatorial delay			0.6		0.8	ns
$t_{IC}$	Array clock delay			1.8		2.3	ns
$t_{EN}$	Register enable time			1.0		1.3	ns
$t_{GLOB}$	Global control delay			1.7		2.2	ns
$t_{PRE}$	Register preset time			1.0		1.4	ns
$t_{CLR}$	Register clear time			1.0		1.4	ns
$t_{PIA}$	PIA delay	(2)		3.0		4.0	ns
$t_{LPA}$	Low-power adder	(5)		4.5		5.0	ns

**Notes to tables:**

- These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.
- These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{\text{MAX}}$ , in MHz) for MAX 3000A devices is calculated with the following equation:

$$P = P_{\text{INT}} + P_{\text{IO}} = I_{\text{CCINT}} \times V_{\text{CC}} + P_{\text{IO}}$$

The  $P_{\text{IO}}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The  $I_{\text{CCINT}}$  value depends on the switching frequency and the application logic. The  $I_{\text{CCINT}}$  value is calculated with the following equation:

$$I_{\text{CCINT}} =$$

$$(A \times \text{MC}_{\text{TON}}) + [B \times (\text{MC}_{\text{DEV}} - \text{MC}_{\text{TON}})] + (C \times \text{MC}_{\text{USED}} \times f_{\text{MAX}} \times \text{tog}_{\text{LC}})$$

The parameters in the  $I_{\text{CCINT}}$  equation are:

- $\text{MC}_{\text{TON}}$  = Number of macrocells with the Turbo Bit™ option turned on, as reported in the Quartus II or MAX+PLUS II Report File (.rpt)
- $\text{MC}_{\text{DEV}}$  = Number of macrocells in the device
- $\text{MC}_{\text{USED}}$  = Total number of macrocells in the design, as reported in the RPT File
- $f_{\text{MAX}}$  = Highest clock frequency to the device
- $\text{tog}_{\text{LC}}$  = Average percentage of logic cells toggling at each clock (typically 12.5%)
- A, B, C = Constants (shown in Table 26)

**Table 26. MAX 3000A  $I_{\text{CC}}$  Equation Constants**

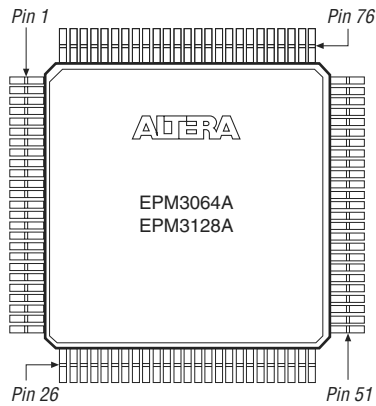
Device	A	B	C
EPM3032A	0.71	0.30	0.014
EPM3064A	0.71	0.30	0.014
EPM3128A	0.71	0.30	0.014
EPM3256A	0.71	0.30	0.014
EPM3512A	0.71	0.30	0.014

The  $I_{\text{CCINT}}$  calculation provides an  $I_{\text{CC}}$  estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual  $I_{\text{CC}}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

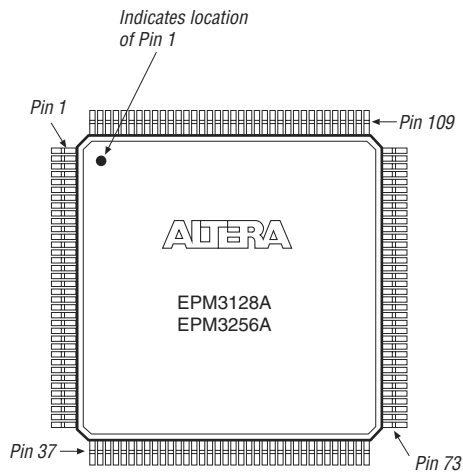
Figures 12 and 13 show the typical supply current versus frequency for MAX 3000A devices.

**Figure 15. 100-Pin TQFP Package Pin-Out Diagram**

Package outline not drawn to scale.

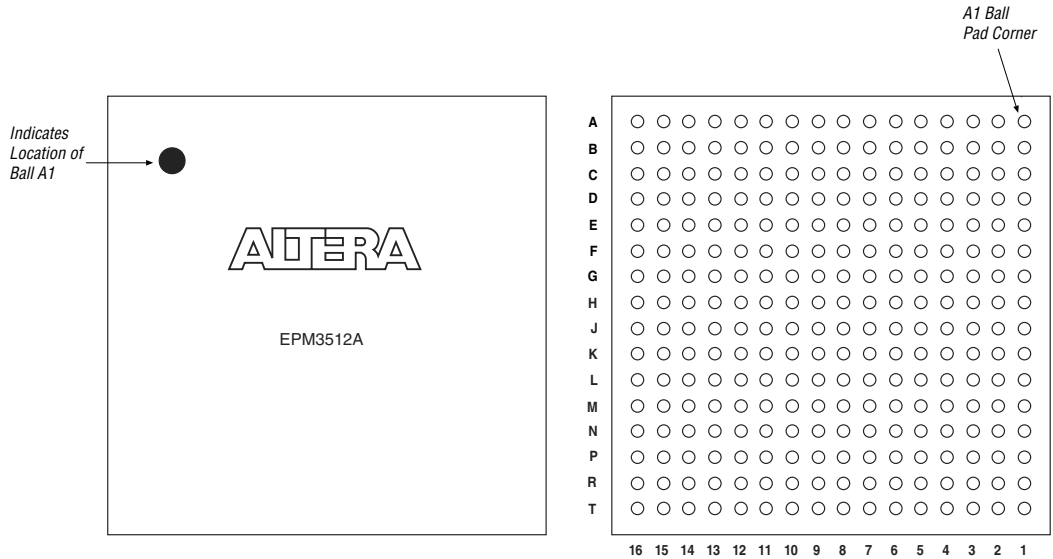
**Figure 16. 144-Pin TQFP Package Pin-Out Diagram**

Package outline not drawn to scale.



**Figure 18. 256-Pin FineLine BGA Package Pin-Out Diagram**

Package outline not drawn to scale.



## Revision History

The information contained in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5 supersedes information published in previous versions. The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5:

### Version 3.5

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.5:

- New paragraph added before “Expander Product Terms”.

### Version 3.4

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.4:

- Updated Table 1.

### Version 3.3

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.3:

- Updated Tables 3, 13, and 26.
- Added Tables 4 through 6.
- Updated Figures 12 and 13.
- Added “Programming Sequence” on page 14 and “Programming Times” on page 14

### Version 3.2

The following change were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.2:

- Updated the EPM3512 I<sub>CC</sub> versus frequency graph in Figure 13.

### Version 3.1

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.1:

- Updated timing information in Table 1 for the EPM3256A device.
- Updated *Note (10)* of Table 15.

### Version 3.0

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.0:

- Added EPM3512A device.
- Updated Tables 2 and 3.

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