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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	158
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm3256aqi208-10">https://www.e-xfl.com/product-detail/intel/epm3256aqi208-10</a>

## ...and More Features

- PCI compatible
- Bus-friendly architecture including programmable slew-rate control
- Open-drain output option
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a power reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- Enhanced architectural features, including:
  - 6 or 10 pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from third-party manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with the Altera master programming unit (MPU), MasterBlaster™ communications cable, ByteBlasterMV™ parallel port download cable, BitBlaster™ serial download cable as well as programming hardware from third-party manufacturers and any in-circuit tester that supports Jam™ Standard Test and Programming Language (STAPL) Files (.jam), Jam STAPL Byte-Code Files (.jbc), or Serial Vector Format Files (.svf)

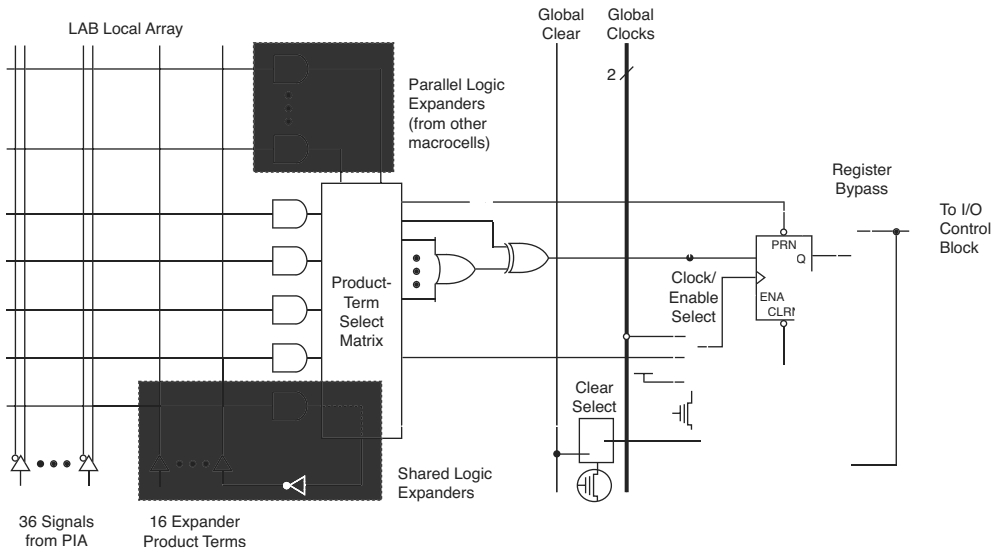
## General Description

MAX 3000A devices are low-cost, high-performance devices based on the Altera MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 3000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 3000A devices in the -4, -5, -6, -7, and -10 speed grades are compatible with the timing requirements of the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See Table 2.

## Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product-term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

**Figure 2. MAX 3000A Macrocell**



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development system software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal mode, which achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 3000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the two global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn).

All registers are cleared upon power-up. By default, all registered outputs drive low when the device is powered up. You can set the registered outputs to drive high upon power-up through the Quartus® II software. Quartus II software uses the NOT Gate Push-Back method, which uses an additional macrocell to set the output high. To set this in the Quartus II software, go to the Assignment Editor and set the **Power-Up Level** assignment for the register to **High**.

### *Parallel Expanders*

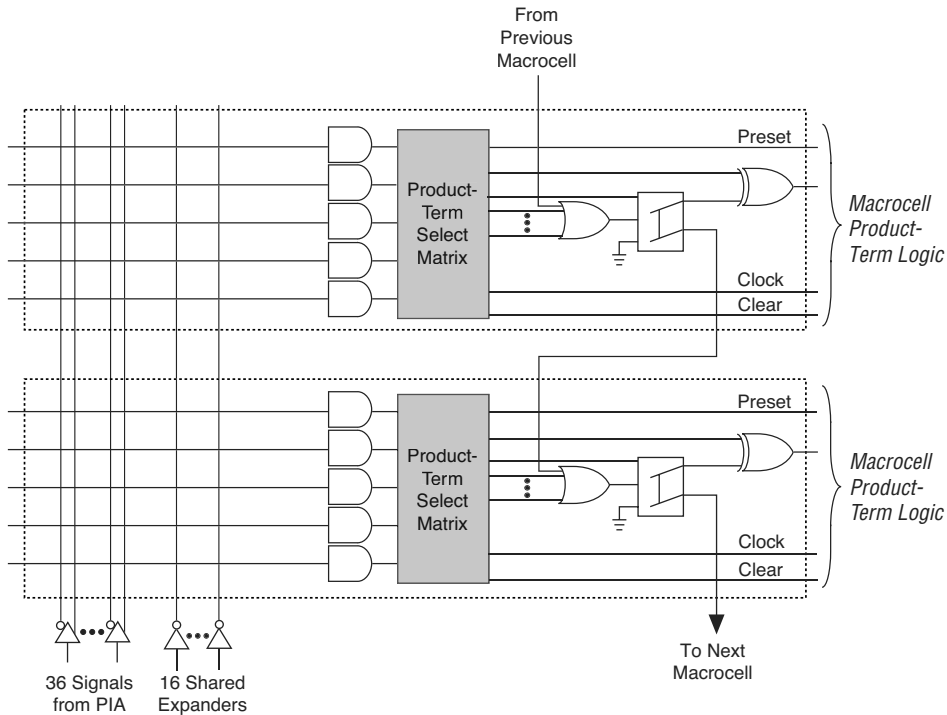
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

**Figure 4. MAX 3000A Parallel Expanders**

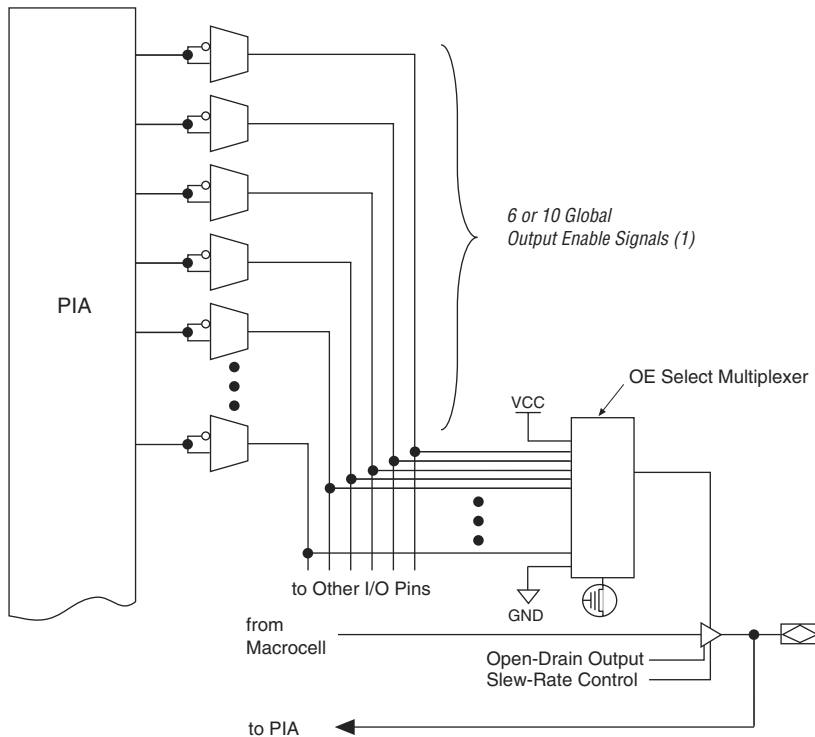
*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



## Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 6. I/O Control Block of MAX 3000A Devices

**Note:**

- (1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance), and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

The MAX 3000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 3000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.



The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary-scan register length and device IDCODE information for MAX 3000A devices.

**Table 8. MAX 3000A Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPM3032A	96
EPM3064A	192
EPM3128A	288
EPM3256A	480
EPM3512A	624

**Table 9. 32-Bit MAX 3000A Device IDCODE Value** Note (1)

Device	IDCODE (32 bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM3032A	0001	0111 0000 0011 0010	00001101110	1
EPM3064A	0001	0111 0000 0110 0100	00001101110	1
EPM3128A	0001	0111 0001 0010 1000	00001101110	1
EPM3256A	0001	0111 0010 0101 0110	00001101110	1
EPM3512A	0001	0111 0101 0001 0010	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

## Programmable Speed/Power Control

MAX 3000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 3000A device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{ACL}$ ,  $t_{EN}$ ,  $t_{CPPW}$  and  $t_{SEXP}$  parameters.

## Output Configuration

MAX 3000A device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

The MAX 3000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 3000A devices to connect to systems with differing supply voltages. MAX 3000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O pin operation. These devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for I/O output drivers ( $V_{CCIO}$ ).

The  $V_{CCIO}$  pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels lower than 3.0 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ . Inputs can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Table 11 summarizes the MAX 3000A MultiVolt I/O support.

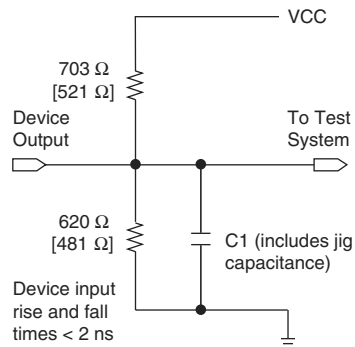
<b>Table 11. MAX 3000A MultiVolt I/O Support</b>						
<b><math>V_{CCIO}</math> Voltage</b>	<b>Input Signal (V)</b>			<b>Output Signal (V)</b>		
	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓	✓	✓	✓

**Note:**

- (1) When  $V_{CCIO}$  is 3.3 V, a MAX 3000A device can drive a 2.5-V device that has 3.3-V tolerant inputs.

**Figure 8. MAX 3000A AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V devices or outputs.



## Operating Conditions

Tables 12 through 15 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for MAX 3000A devices.

**Table 12. MAX 3000A Device Absolute Maximum Ratings**      *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	-0.5	4.6	V
$V_I$	DC input voltage		-2.0	5.75	V
$I_{OUT}$	DC output current, per pin		-25	25	mA
$T_{STG}$	Storage temperature	No bias	-65	150	°C
$T_A$	Ambient temperature	Under bias	-65	135	°C
$T_J$	Junction temperature	PQFP and TQFP packages, under bias		135	°C

**Table 13. MAX 3000A Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(10)	3.0	3.6	V
$V_{CCIO}$	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.3	2.7	V
$V_{CCISP}$	Supply voltage during ISP		3.0	3.6	V
$V_I$	Input voltage	(3)	-0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_A$	Ambient temperature	Commercial range	0	70	°C
		Industrial range	-40	85	°C
$T_J$	Junction temperature	Commercial range	0	90	°C
		Industrial range (11)	-40	105	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 14. MAX 3000A Device DC Operating Conditions** Note (4)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{IH}$	High-level input voltage		1.7	5.75	V
$V_{IL}$	Low-level input voltage		-0.5	0.8	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (5)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (5)	$V_{CCIO} - 0.2$		V
	2.5-V high-level output voltage	$I_{OH} = -100$ $\mu$ A DC, $V_{CCIO} = 2.30$ V (5)	2.1		V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (5)	2.0		V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (5)	1.7		V
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 8$ mA DC, $V_{CCIO} = 3.00$ V (6)		0.4	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (6)		0.2	V
	2.5-V low-level output voltage	$I_{OL} = 100$ $\mu$ A DC, $V_{CCIO} = 2.30$ V (6)		0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (6)		0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (6)		0.7	V
$I_I$	Input leakage current	$V_I = -0.5$ to 5.5 V (7)	-10	10	$\mu$ A
$I_{OZ}$	Tri-state output off-state current	$V_I = -0.5$ to 5.5 V (7)	-10	10	$\mu$ A
$R_{ISP}$	Value of I/O pin pull-up resistor when programming in-system or during power-up	$V_{CCIO} = 2.3$ to 3.6 V (8)	20	74	k $\Omega$

**Table 15. MAX 3000A Device Capacitance** Note (9)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input pin capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to tables:**

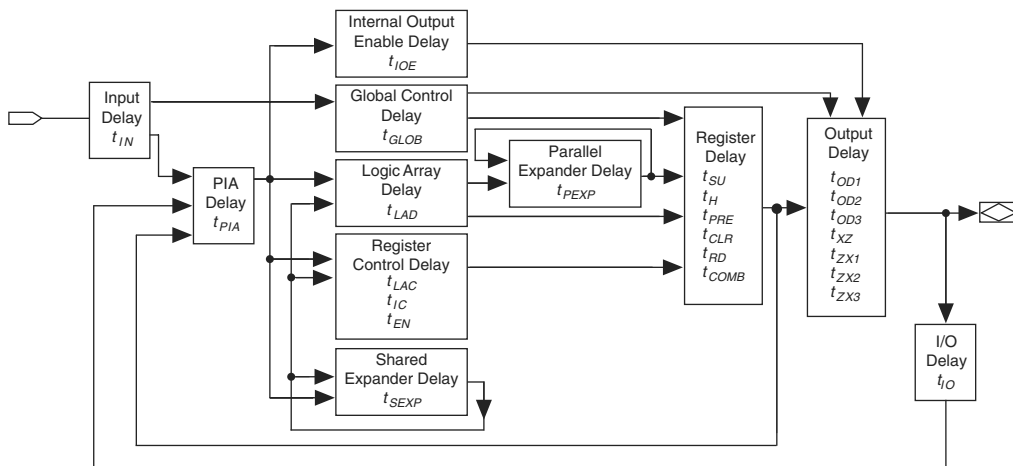
- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (4) These values are specified under the recommended operating conditions, as shown in Table 13 on page 23.
- (5) The parameter is measured with 50% of the outputs each sourcing the specified current. The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (6) The parameter is measured with 50% of the outputs each sinking the specified current. The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current.
- (7) This value is specified during normal device operation. During power-up, the maximum leakage current is  $\pm 300\text{ }\mu\text{A}$ .
- (8) This pull-up exists while devices are programmed in-system and in unprogrammed devices during power-up.
- (9) Capacitance is measured at  $25^\circ\text{ C}$  and is sample-tested only. The  $\text{OE1}$  pin (high-voltage pin during programming) has a maximum capacitance of  $20\text{ pF}$ .
- (10) The POR time for all MAX 3000A devices does not exceed  $100\text{ }\mu\text{s}$ . The sufficient  $V_{CCINT}$  voltage level for POR is  $3.0\text{ V}$ . The device is fully initialized within the POR time after  $V_{CCINT}$  reaches the sufficient POR voltage level.
- (11) These devices support in-system programming for  $-40^\circ$  to  $100^\circ\text{ C}$ . For in-system programming support between  $-40^\circ$  and  $0^\circ\text{ C}$ , contact Altera Applications.

Figure 9 shows the typical output drive characteristics of MAX 3000A devices.

## Timing Model

MAX 3000A device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 3000A devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

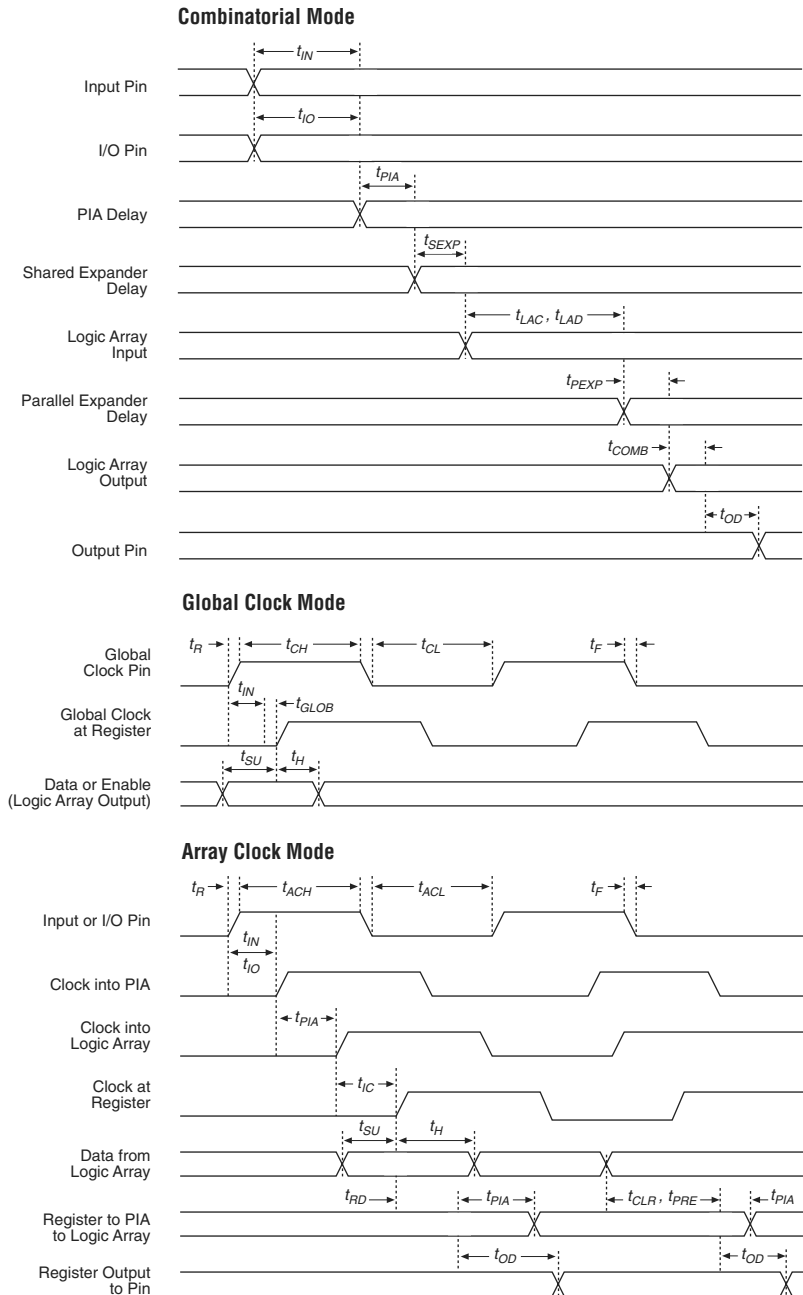
**Figure 10. MAX 3000A Timing Model**



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the timing relationship between internal and external delay parameters.

**Figure 11. MAX 3000A Switching Waveforms**

$t_R$  &  $t_F < 2$  ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



**Table 19. EPM3064A Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.6		1.1		1.4	ns
$t_{IO}$	I/O input pad and buffer delay			0.6		1.1		1.4	ns
$t_{SEXP}$	Shared expander delay			1.8		3.0		3.9	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.7		0.9	ns
$t_{LAD}$	Logic array delay			1.5		2.5		3.2	ns
$t_{LAC}$	Logic control array delay			0.6		1.0		1.2	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.3		1.8	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.3		1.8		2.3	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.3		6.8	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		1.3		2.0		2.9		ns
$t_H$	Register hold time		0.6		1.0		1.3		ns
$t_{RD}$	Register delay			0.7		1.2		1.6	ns
$t_{COMB}$	Combinatorial delay			0.6		0.9		1.3	ns
$t_{IC}$	Array clock delay			1.2		1.9		2.5	ns
$t_{EN}$	Register enable time			0.6		1.0		1.2	ns
$t_{GLOB}$	Global control delay			1.0		1.5		2.2	ns
$t_{PRE}$	Register preset time			1.3		2.1		2.9	ns



**Table 20. EPM3128A External Timing Parameters** Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			−5		−7		−10		
			Min	Max	Min	Max	Min	Max	
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	192.3		129.9		98.0		MHz

**Table 21. EPM3128A Internal Timing Parameters (Part 1 of 2)** Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		1.0		1.4	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		1.0		1.4	ns
$t_{SEXP}$	Shared expander delay			2.0		2.9		3.8	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.7		0.9	ns
$t_{LAD}$	Logic array delay			1.6		2.4		3.1	ns
$t_{LAC}$	Logic control array delay			0.7		1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		0.8		1.2		1.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.3		1.7		2.1	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		5.8		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		4.0		4.0		5.0	ns

**Table 22. EPM3256A External Timing Parameters** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
t <sub>CNT</sub>	Minimum global clock period	(2)		7.9		10.5	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	126.6		95.2		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		7.9		10.5	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	126.6		95.2		MHz

**Table 23. EPM3256A Internal Timing Parameters (Part 1 of 2)** Note (1)

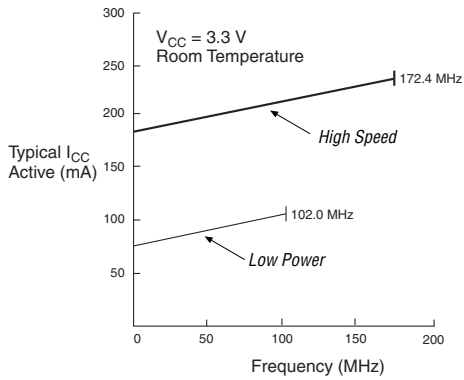
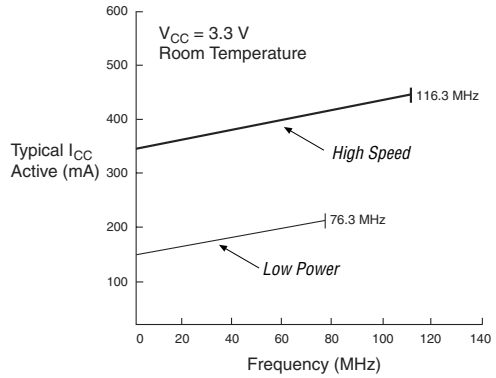
Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		−10		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.9		1.2	ns
$t_{IO}$	I/O input pad and buffer delay			0.9		1.2	ns
$t_{SEXP}$	Shared expander delay			2.8		3.7	ns
$t_{PEXP}$	Parallel expander delay			0.5		0.6	ns
$t_{LAD}$	Logic array delay			2.2		2.8	ns
$t_{LAC}$	Logic control array delay			1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.2		1.6	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.7		2.1	ns
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on $V_{CCIO} = 2.5\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$		6.2		6.6	ns
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		4.5		5.5	ns

**Table 24. EPM3512A External Timing Parameters** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t <sub>AH</sub>	Array clock hold time	(2)	0.2		0.3		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF (2)	1.0	7.8	1.0	10.4	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	3.0		4.0		ns
t <sub>CNT</sub>	Minimum global clock period	(2)		8.6		11.5	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(2), (4)	116.3		87.0		MHz
t <sub>ACNT</sub>	Minimum array clock period	(2)		8.6		11.5	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(2), (4)	116.3		87.0		MHz

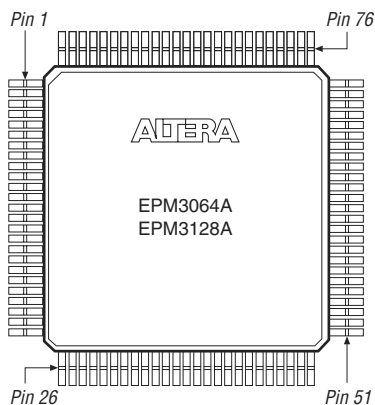
**Table 25. EPM3512A Internal Timing Parameters (Part 1 of 2)** Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.7		0.9	ns
$t_{IO}$	I/O input pad and buffer delay			0.7		0.9	ns
$t_{FIN}$	Fast input delay			3.1		3.6	ns
$t_{SEXP}$	Shared expander delay			2.7		3.5	ns
$t_{PEXP}$	Parallel expander delay			0.4		0.5	ns
$t_{LAD}$	Logic array delay			2.2		2.8	ns
$t_{LAC}$	Logic control array delay			1.0		1.3	ns
$t_{IOE}$	Internal output enable delay			0.0		0.0	ns
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$		1.0		1.5	ns
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off $V_{CCIO} = 2.5\text{ V}$	$C1 = 35\text{ pF}$		1.5		2.0	ns

**Figure 13.  $I_{CC}$  vs. Frequency for MAX 3000A Devices****EPM3256A****EPM3512A**

**Figure 15. 100-Pin TQFP Package Pin-Out Diagram**

Package outline not drawn to scale.

**Figure 16. 144-Pin TQFP Package Pin-Out Diagram**

Package outline not drawn to scale.

