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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 3V ~ 3.6V |
| Number of Logic Elements/Blocks | 16 |
| Number of Macrocells | 256 |
| Number of Gates | 5000 |
| Number of I/O | 116 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm3256atc144-7 |

*Table 2. MAX 3000A Speed Grades*

| Device | Speed Grade | | | | |
|---|---|---|---|---|---|
| | –4 | –5 | –6 | –7 | –10 |
| EPM3032A | ✓ | | | ✓ | ✓ |
| EPM3064A | ✓ | | | ✓ | ✓ |
| EPM3128A | | ✓ | | ✓ | ✓ |
| EPM3256A | | | | ✓ | ✓ |
| EPM3512A | | | | ✓ | ✓ |

The MAX 3000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high–density small-scale integration (SSI), medium-scale integration (MSI), and large-scale integration (LSI) logic functions. The MAX 3000A architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 3000A devices are available in a wide range of packages, including PLCC, PQFP, and TQFP packages. See Table 3.

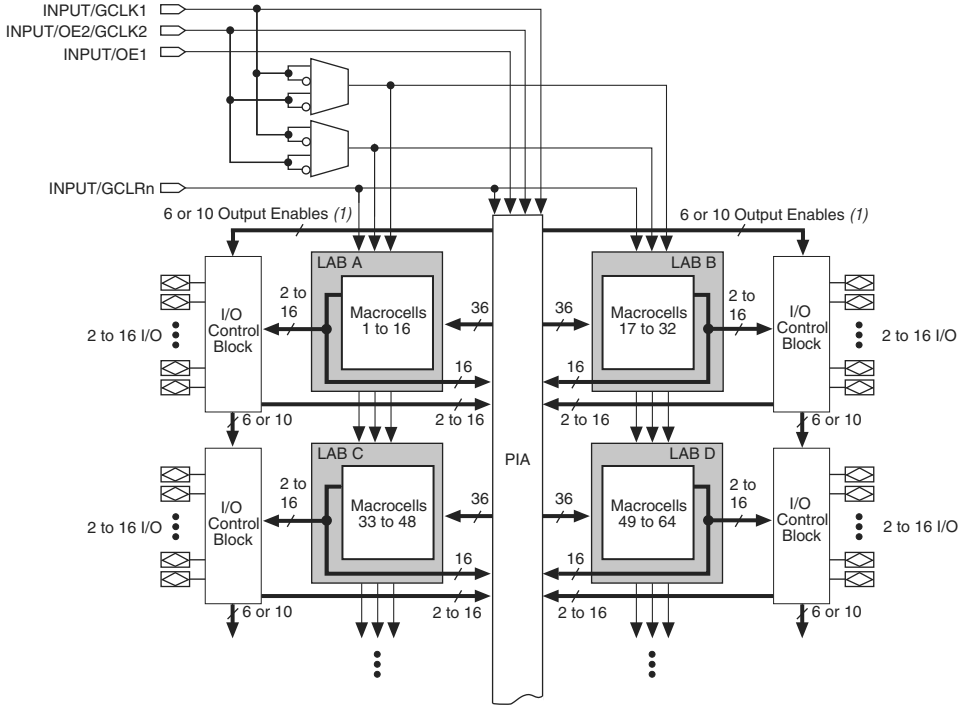
*Table 3. MAX 3000A Maximum User I/O Pins* *Note (1)*

| Device | 44–Pin PLCC | 44–Pin TQFP | 100–Pin TQFP | 144–Pin TQFP | 208–Pin PQFP | 256-Pin FineLine BGA |
|---|---|---|---|---|---|---|
| EPM3032A | 34 | 34 | | | | |
| EPM3064A | 34 | 34 | 66 | | | |
| EPM3128A | | | 80 | 96 | | 98 |
| EPM3256A | | | | 116 | 158 | 161 |
| EPM3512A | | | | | 172 | 208 |

*Note:*
(1) When the IEEE Std. 1149.1 (JTAG) interface is used for in–system programming or boundary–scan testing, four I/O pins become JTAG pins.

MAX 3000A devices use CMOS EEPROM cells to implement logic functions. The user–configurable MAX 3000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debugging cycles, and can be programmed and erased up to 100 times.

*Figure 1. MAX 3000A Device Block Diagram*




*Note:*

(1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

## Logic Array Blocks

The MAX 3000A device architecture is based on the linking of high–performance LABs. LABs consist of 16–macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

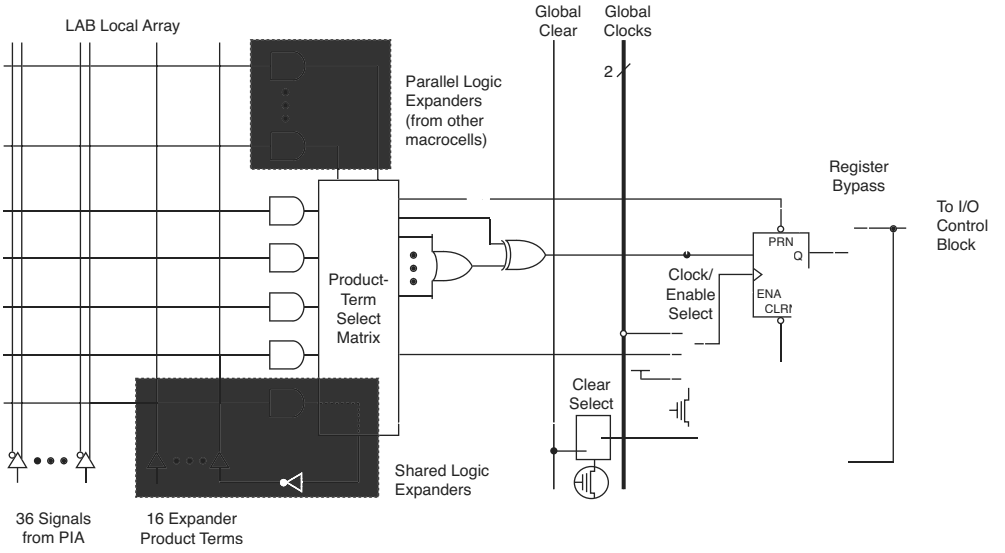
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions

## Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product–term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

***Figure 2. MAX 3000A Macrocell***




Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product–term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

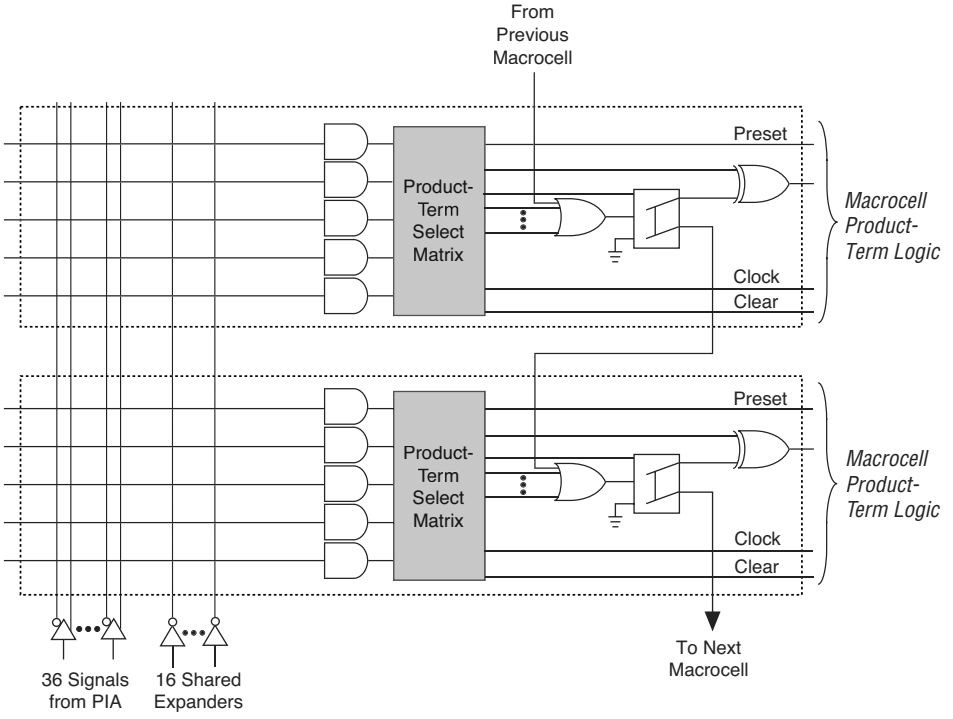
Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product–term allocation according to the logic requirements of the design.

*Figure 4. MAX 3000A Parallel Expanders*

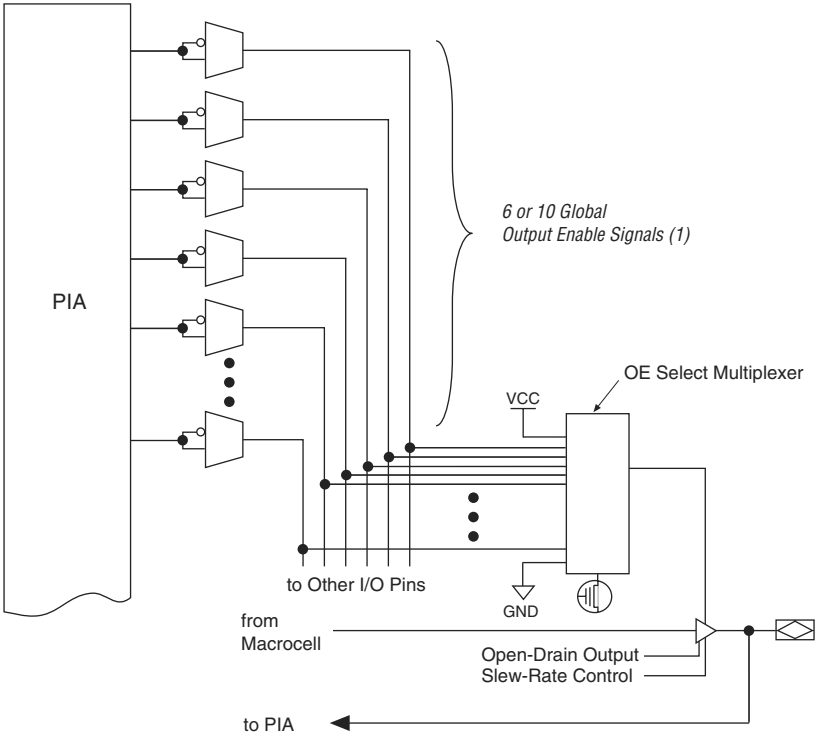
*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*




## Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

*Figure 6. I/O Control Block of MAX 3000A Devices*




*Note:*
(1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

When the tri–state buffer control is connected to ground, the output is tri-stated (high impedance), and the I/O pin can be used as a dedicated input. When the tri–state buffer control is connected to $V_{CC}$, the output is enabled.

The MAX 3000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 3000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

The programming times described in Tables 4 through 6 are associated with the worst-case method using the enhanced ISP algorithm.

*Table 4. MAX 3000A $t_{PULSE}$ & $Cycle_{TCK}$ Values*

| Device | Programming | | Stand-Alone Verification | |
|---|---|---|---|---|
| | $t_{PPULSE}$ (s) | $Cycle_{PTCK}$ | $t_{VPULSE}$ (s) | $Cycle_{VTCK}$ |
| EPM3032A | 2.00 | 55,000 | 0.002 | 18,000 |
| EPM3064A | 2.00 | 105,000 | 0.002 | 35,000 |
| EPM3128A | 2.00 | 205,000 | 0.002 | 68,000 |
| EPM3256A | 2.00 | 447,000 | 0.002 | 149,000 |
| EPM3512A | 2.00 | 890,000 | 0.002 | 297,000 |

Tables 5 and 6 show the in-system programming and stand alone verification times for several common test clock frequencies.

*Table 5. MAX 3000A In-System Programming Times for Different Test Clock Frequencies*

| Device | $f_{TCK}$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM3032A | 2.01 | 2.01 | 2.03 | 2.06 | 2.11 | 2.28 | 2.55 | 3.10 | s |
| EPM3064A | 2.01 | 2.02 | 2.05 | 2.11 | 2.21 | 2.53 | 3.05 | 4.10 | s |
| EPM3128A | 2.02 | 2.04 | 2.10 | 2.21 | 2.41 | 3.03 | 4.05 | 6.10 | s |
| EPM3256A | 2.05 | 2.09 | 2.23 | 2.45 | 2.90 | 4.24 | 6.47 | 10.94 | s |
| EPM3512A | 2.09 | 2.18 | 2.45 | 2.89 | 3.78 | 6.45 | 10.90 | 19.80 | s |

*Table 6. MAX 3000A Stand-Alone Verification Times for Different Test Clock Frequencies*

| Device | $f_{TCK}$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM3032A | 0.00 | 0.01 | 0.01 | 0.02 | 0.04 | 0.09 | 0.18 | 0.36 | s |
| EPM3064A | 0.01 | 0.01 | 0.02 | 0.04 | 0.07 | 0.18 | 0.35 | 0.70 | s |
| EPM3128A | 0.01 | 0.02 | 0.04 | 0.07 | 0.14 | 0.34 | 0.68 | 1.36 | s |
| EPM3256A | 0.02 | 0.03 | 0.08 | 0.15 | 0.30 | 0.75 | 1.49 | 2.98 | s |
| EPM3512A | 0.03 | 0.06 | 0.15 | 0.30 | 0.60 | 1.49 | 2.97 | 5.94 | s |

## Programming with External Hardware

MAX 3000A devices can be programmed on Windows–based PCs with an Altera Logic Programmer card, MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera software can use text– or waveform–format test vectors created with the Altera Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.

For more information, see *Programming Hardware Manufacturers*.

## IEEE Std. 1149.1 (JTAG) Boundary–Scan Support

MAX 3000A devices include the JTAG BST circuitry defined by IEEE Std. 1149.1–1990. Table 7 describes the JTAG instructions supported by MAX 3000A devices. The pin-out tables found on the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

*Table 7. MAX 3000A JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins |
| EXTEST | Allows the external circuitry and board–level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins |
| BYPASS | Places the 1–bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation |
| IDCODE | Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO` |
| USERCODE | Selects the 32–bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO` |
| ISP Instructions | These instructions are used when programming MAX 3000A devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, or BitBlaster cable, or when using a Jam STAPL file, JBC file, or SVF file via an embedded processor or test equipment |

The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary–scan register length and device IDCODE information for MAX 3000A devices.

*Table 8. MAX 3000A Boundary–Scan Register Length*

| Device | Boundary–Scan Register Length |
|---|---|
| EPM3032A | 96 |
| EPM3064A | 192 |
| EPM3128A | 288 |
| EPM3256A | 480 |
| EPM3512A | 624 |

*Table 9. 32–Bit MAX 3000A Device IDCODE Value* *Note (1)*

| Device | IDCODE (32 bits) | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer's Identity (11 Bits) | 1 (1 Bit) *(2)* |
| EPM3032A | 0001 | 0111 0000 0011 0010 | 00001101110 | 1 |
| EPM3064A | 0001 | 0111 0000 0110 0100 | 00001101110 | 1 |
| EPM3128A | 0001 | 0111 0001 0010 1000 | 00001101110 | 1 |
| EPM3256A | 0001 | 0111 0010 0101 0110 | 00001101110 | 1 |
| EPM3512A | 0001 | 0111 0101 0001 0010 | 00001101110 | 1 |

*Notes:*
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary–Scan Testing in Altera Devices)* for more information on JTAG BST.

## Programmable Speed/Power Control

MAX 3000A devices offer a power–saving mode that supports low-power operation across user–defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 3000A device for either high–speed or low–power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ($t_{LPA}$) for the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{EN}$, $t_{CPPW}$ and $t_{SEXP}$ parameters.

## Output Configuration

MAX 3000A device outputs can be programmed to meet a variety of system–level requirements.

### MultiVolt I/O Interface

The MAX 3000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 3000A devices to connect to systems with differing supply voltages. MAX 3000A devices in all packages can be set for 2.5–V, 3.3–V, or 5.0–V I/O pin operation. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3–V or 2.5–V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5–V power supply, the output levels are compatible with 2.5–V systems. When the VCCIO pins are connected to a 3.3–V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0–V systems. Devices operating with $V_{CCIO}$ levels lower than 3.0 V incur a nominally greater timing delay of $t_{OD2}$ instead of $t_{OD1}$. Inputs can always be driven by 2.5–V, 3.3–V, or 5.0–V signals.

Table 11 summarizes the MAX 3000A MultiVolt I/O support.

*Table 11. MAX 3000A MultiVolt I/O Support*

| $V_{CCIO}$ Voltage | Input Signal (V) | | | Output Signal (V) | | |
|---|---|---|---|---|---|---|
| | 2.5 | 3.3 | 5.0 | 2.5 | 3.3 | 5.0 |
| 2.5 | ✓ | ✓ | ✓ | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

*Note:*
(1) When $V_{CCIO}$ is 3.3 V, a MAX 3000A device can drive a 2.5–V device that has 3.3–V tolerant inputs.

*Table 13. MAX 3000A Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(10)* | 3.0 | 3.6 | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 3.3–V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers, 2.5–V operation | | 2.3 | 2.7 | V |
| $V_{CCISP}$ | Supply voltage during ISP | | 3.0 | 3.6 | V |
| $V_I$ | Input voltage | *(3)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | Commercial range | 0 | 70 | ° C |
| | | Industrial range | –40 | 85 | ° C |
| $T_J$ | Junction temperature | Commercial range | 0 | 90 | ° C |
| | | Industrial range *(11)* | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 14. MAX 3000A Device DC Operating Conditions* *Note (4)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High–level input voltage | | 1.7 | 5.75 | V |
| $V_{IL}$ | Low–level input voltage | | –0.5 | 0.8 | V |
| $V_{OH}$ | 3.3–V high–level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | 2.4 | | V |
| | 3.3–V high–level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(5)* | $V_{CCIO}$ – 0.2 | | V |
| | 2.5–V high–level output voltage | $I_{OH}$ = –100 µA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.1 | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 2.0 | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(5)* | 1.7 | | V |
| $V_{OL}$ | 3.3–V low–level TTL output voltage | $I_{OL}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.4 | V |
| | 3.3–V low–level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(6)* | | 0.2 | V |
| | 2.5–V low–level output voltage | $I_{OL}$ = 100 µA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(6)* | | 0.7 | V |
| $I_I$ | Input leakage current | $V_I$ = –0.5 to 5.5 V *(7)* | –10 | 10 | µA |
| $I_{OZ}$ | Tri–state output off–state current | $V_I$ = –0.5 to 5.5 V *(7)* | –10 | 10 | µA |
| $R_{ISP}$ | Value of I/O pin pull–up resistor when programming in–system or during power–up | $V_{CCIO}$ = 2.3 to 3.6 V *(8)* | 20 | 74 | kΩ |

*Table 19. EPM3064A Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –4 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CLR}$ | Register clear time | | | 1.3 | | 2.1 | | 2.9 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 1.0 | | 1.7 | | 2.3 | ns |
| $t_{LPA}$ | Low–power adder | *(5)* | | 3.5 | | 4.0 | | 5.0 | ns |

*Table 20. EPM3128A External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –5 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non–registered output | C1 = 35 pF *(2)* | | 5.0 | | 7.5 | | 10 | ns |
| $t_{PD2}$ | I/O input to non–registered output | C1 = 35 pF *(2)* | | 5.0 | | 7.5 | | 10 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 3.3 | | 4.9 | | 6.6 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 3.4 | 1.0 | 5.0 | 1.0 | 6.6 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 1.8 | | 2.8 | | 3.8 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.3 | | 0.4 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 4.9 | 1.0 | 7.1 | 1.0 | 9.4 | ns |
| $t_{ACH}$ | Array clock high time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 2.0 | | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 5.2 | | 7.7 | | 10.2 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(4)* | 192.3 | | 129.9 | | 98.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 5.2 | | 7.7 | | 10.2 | ns |

*Table 21. EPM3128A Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –5 | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | Register setup time | | 1.4 | | 2.1 | | 2.9 | | ns |
| $t_{H}$ | Register hold time | | 0.6 | | 1.0 | | 1.3 | | ns |
| $t_{RD}$ | Register delay | | | 0.8 | | 1.2 | | 1.6 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.5 | | 0.9 | | 1.3 | ns |
| $t_{IC}$ | Array clock delay | | | 1.2 | | 1.7 | | 2.2 | ns |
| $t_{EN}$ | Register enable time | | | 0.7 | | 1.0 | | 1.3 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.1 | | 1.6 | | 2.0 | ns |
| $t_{PRE}$ | Register preset time | | | 1.4 | | 2.0 | | 2.7 | ns |
| $t_{CLR}$ | Register clear time | | | 1.4 | | 2.0 | | 2.7 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 1.4 | | 2.0 | | 2.6 | ns |
| $t_{LPA}$ | Low–power adder | *(5)* | | 4.0 | | 4.0 | | 5.0 | ns |

*Table 22. EPM3256A External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non–registered output | C1 = 35 pF *(2)* | | 7.5 | | 10 | ns |
| $t_{PD2}$ | I/O input to non–registered output | C1 = 35 pF *(2)* | | 7.5 | | 10 | ns |
| $t_{SU}$ | Global clock setup time | *(2)* | 5.2 | | 6.9 | | ns |
| $t_{H}$ | Global clock hold time | *(2)* | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | 1.0 | 4.8 | 1.0 | 6.4 | ns |
| $t_{CH}$ | Global clock high time | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | *(2)* | 2.7 | | 3.6 | | ns |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.3 | | 0.5 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 7.3 | 1.0 | 9.7 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 3.0 | | 4.0 | | ns |

*Table 22. EPM3256A External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 7.9 | | 10.5 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(4)* | 126.6 | | 95.2 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 7.9 | | 10.5 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(4)* | 126.6 | | 95.2 | | MHz |

*Table 23. EPM3256A Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | –7 | | –10 | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.9 | | 1.2 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.9 | | 1.2 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 2.8 | | 3.7 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.5 | | 0.6 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.2 | | 2.8 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.0 | | 1.3 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.2 | | 1.6 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 1.7 | | 2.1 | ns |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.2 | | 6.6 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 4.5 | | 5.5 | ns |

*Table 24. EPM3512A External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | |
| $t_{AH}$ | Array clock hold time | *(2)* | 0.2 | | 0.3 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF *(2)* | 1.0 | 7.8 | 1.0 | 10.4 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 3.0 | | 4.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | *(2)* | | 8.6 | | 11.5 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(2)*, *(4)* | 116.3 | | 87.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | *(2)* | | 8.6 | | 11.5 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(2)*, *(4)* | 116.3 | | 87.0 | | MHz |

*Table 25. EPM3512A Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.7 | | 0.9 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.7 | | 0.9 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.1 | | 3.6 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 2.7 | | 3.5 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.4 | | 0.5 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.2 | | 2.8 | ns |
| $t_{LAC}$ | Logic control array delay | | | 1.0 | | 1.3 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 1.0 | | 1.5 | ns |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 1.5 | | 2.0 | ns |

*Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on $V_{CCIO}$ = 2.5 V or 3.3 V | C1 = 35 pF | | 6.0 | | 6.5 | ns |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off $V_{CCIO}$ = 2.5 V | C1 = 35 pF | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on $V_{CCIO}$ = 3.3 V | C1 = 35 pF | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 2.1 | | 3.0 | | ns |
| $t_{H}$ | Register hold time | | 0.6 | | 0.8 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.6 | | 1.6 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.4 | | 1.4 | | ns |
| $t_{RD}$ | Register delay | | | 1.3 | | 1.7 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.6 | | 0.8 | ns |
| $t_{IC}$ | Array clock delay | | | 1.8 | | 2.3 | ns |
| $t_{EN}$ | Register enable time | | | 1.0 | | 1.3 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.7 | | 2.2 | ns |
| $t_{PRE}$ | Register preset time | | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | Register clear time | | | 1.0 | | 1.4 | ns |
| $t_{PIA}$ | PIA delay | *(2)* | | 3.0 | | 4.0 | ns |
| $t_{LPA}$ | Low-power adder | *(5)* | | 4.5 | | 5.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.

(2) These values are specified for a PIA fan–out of one LAB (16 macrocells). For each additional LAB fan–out in these devices, add an additional 0.1 ns to the PIA timing value.

(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(4) These parameters are measured with a 16–bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in low–power mode.

*Figure 13. $I_{CC}$ vs. Frequency for MAX 3000A Devices*

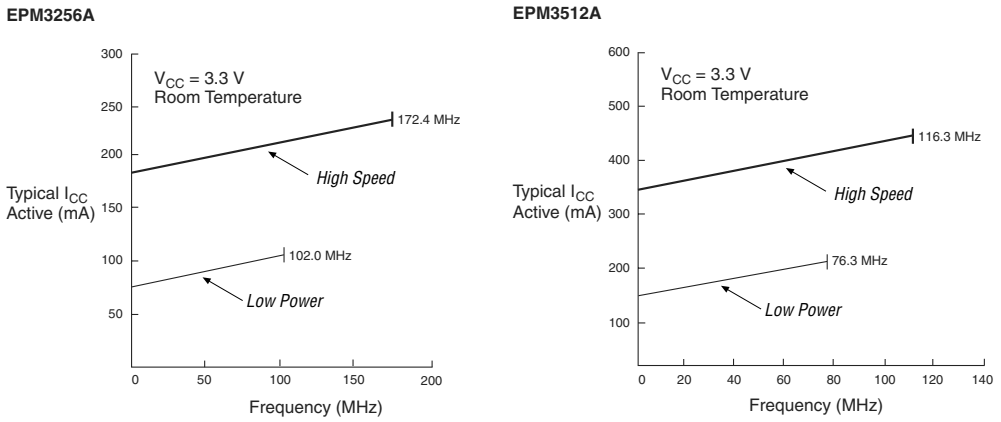


*Figure 15. 100–Pin TQFP Package Pin–Out Diagram*

*Package outline not drawn to scale.*

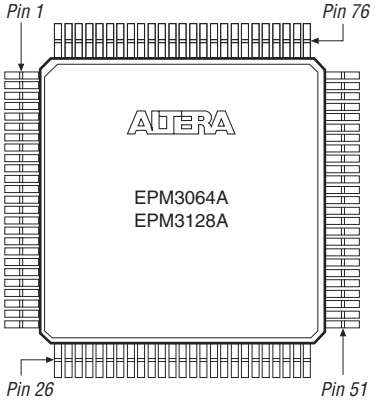



*Figure 16. 144–Pin TQFP Package Pin–Out Diagram*

*Package outline not drawn to scale.*

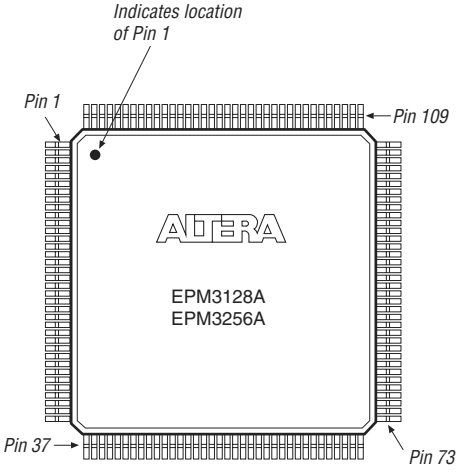
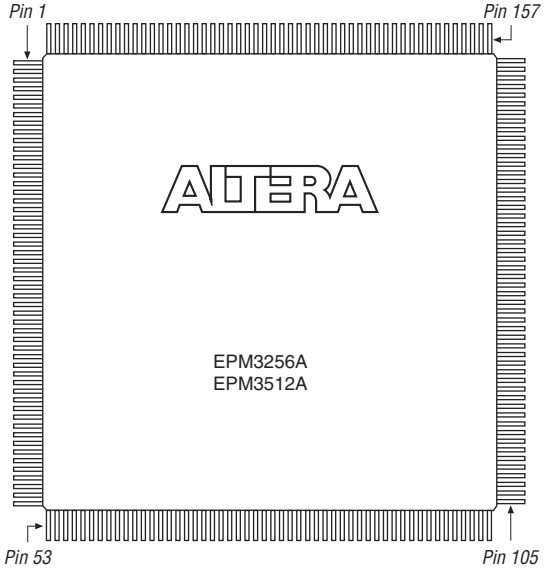


*Figure 17. 208–Pin PQFP Package Pin–Out Diagram*

*Package outline not drawn to scale.*



## Version 3.3

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.3:

- Updated Tables 3, 13, and 26.
- Added Tables 4 through 6.
- Updated Figures 12 and 13.
- Added "Programming Sequence" on page 14 and "Programming Times" on page 14

## Version 3.2

The following change were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.2:

- Updated the EPM3512 $I_{CC}$ versus frequency graph in Figure 13.

## Version 3.1

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.1:

- Updated timing information in Table 1 for the EPM3256A device.
- Updated *Note (10)* of Table 15.

## Version 3.0

The following changes were made in the *MAX 3000A Programmable Logic Device Data Sheet* version 3.0:

- Added EPM3512A device.
- Updated Tables 2 and 3.

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