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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	116
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm3256ati144-10

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MAX 3000A devices contain 32 to 512 macrocells, combined into groups of 16 macrocells called logic array blocks (LABs). Each macrocell has a programmable–AND/fixed–OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with shareable expander and high–speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 3000A devices provide programmable speed/power optimization. Speed–critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 3000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non–speed–critical signals are switching. The output drivers of all MAX 3000A devices can be set for 2.5 V or 3.3 V, and all input pins are 2.5–V, 3.3–V, and 5.0-V tolerant, allowing MAX 3000A devices to be used in mixed–voltage systems.

MAX 3000A devices are supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry–standard PC– and UNIX–workstation–based EDA tools. The software runs on Windows–based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 3000A architecture includes the following elements:

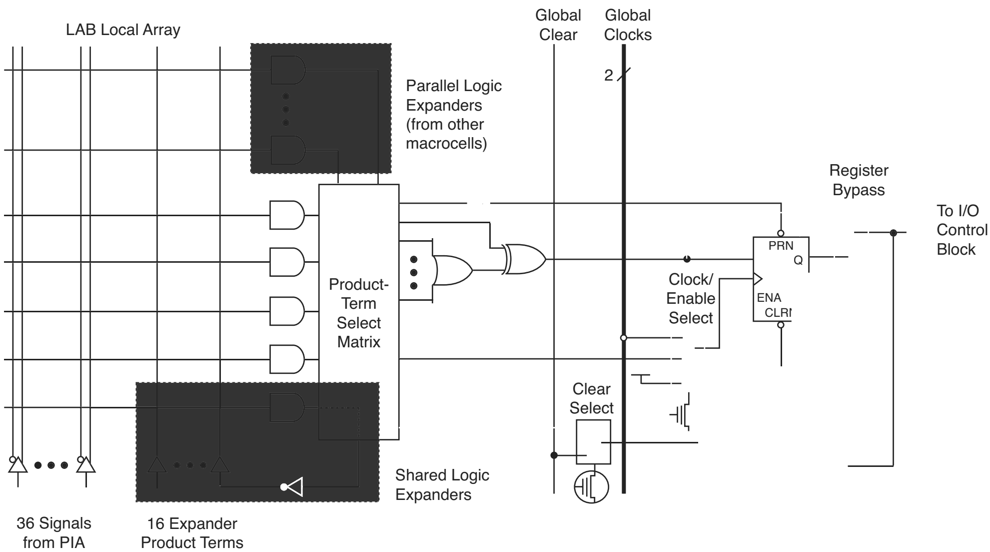
- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array (PIA)
- I/O control blocks

The MAX 3000A architecture includes four dedicated inputs that can be used as general–purpose inputs or as high–speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 3000A devices.

Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product–term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

Figure 2. MAX 3000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product–term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product–term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development system software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal mode, which achieves the fastest clock–to–output performance.
- Global clock signal enabled by an active–high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock–to–output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 3000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the two global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product–term select matrix allocates product terms to control these operations. Although the product–term–driven preset and clear from the register are active high, active–low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active–low dedicated global clear pin (`GCLRn`).

All registers are cleared upon power-up. By default, all registered outputs drive low when the device is powered up. You can set the registered outputs to drive high upon power-up through the Quartus® II software. Quartus II software uses the NOT Gate Push-Back method, which uses an additional macrocell to set the output high. To set this in the Quartus II software, go to the Assignment Editor and set the **Power-Up Level** assignment for the register to **High**.

Parallel Expanders

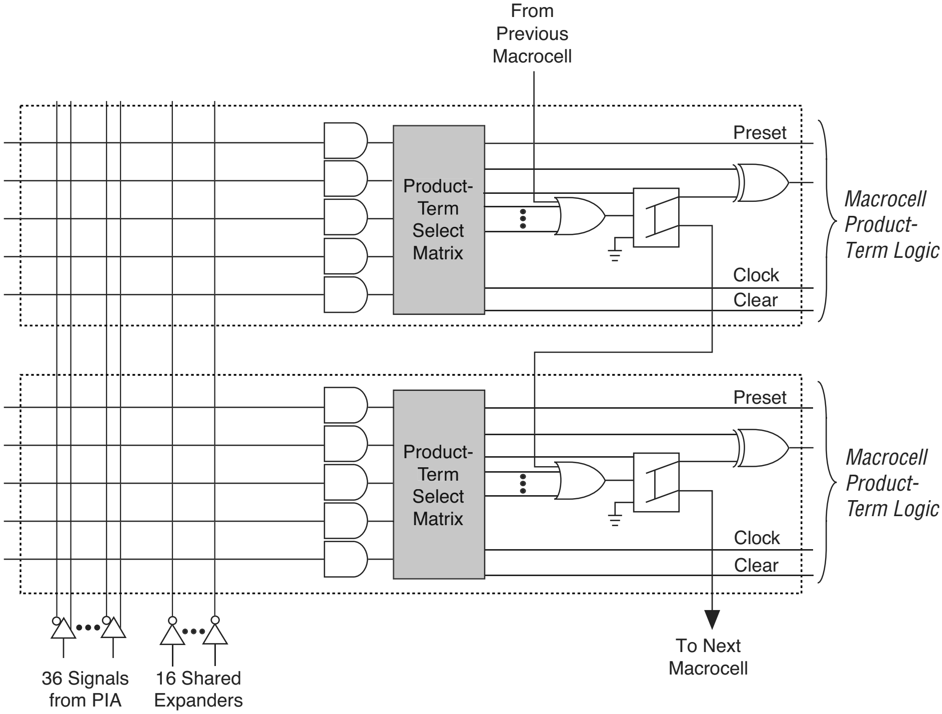
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower–numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest–numbered macrocell can only lend parallel expanders and the highest–numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 3000A Parallel Expanders

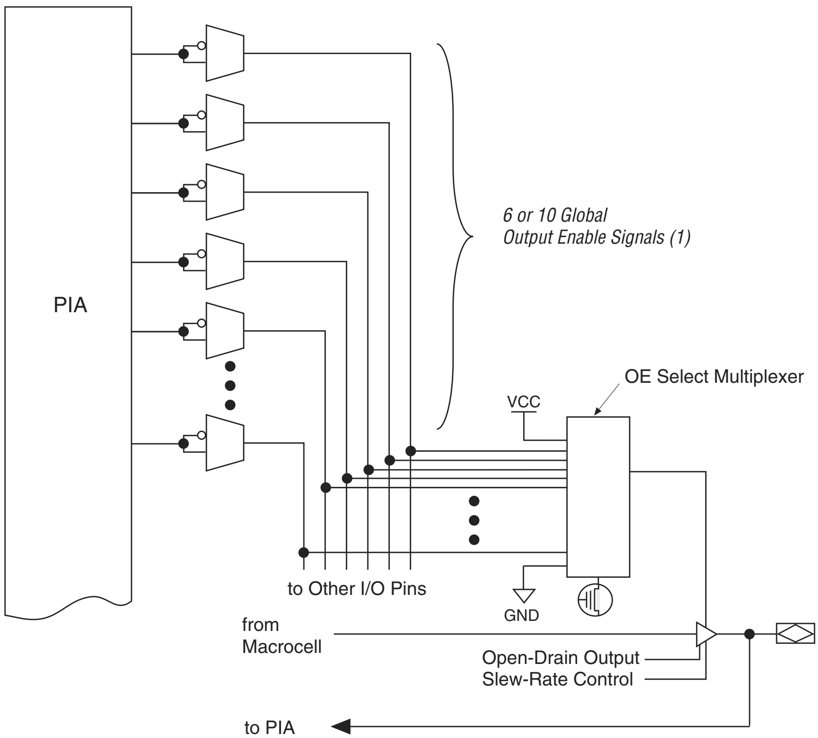
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input `AND` gate, which selects a PIA signal to drive into the LAB.

Figure 6. I/O Control Block of MAX 3000A Devices



Note:

(1) EPM3032A, EPM3064A, EPM3128A, and EPM3256A devices have six output enables. EPM3512A devices have 10 output enables.

When the tri–state buffer control is connected to ground, the output is tri-stated (high impedance), and the I/O pin can be used as a dedicated input. When the tri–state buffer control is connected to V_{CC}, the output is enabled.

The MAX 3000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In–System Programmability

MAX 3000A devices can be programmed in–system via an industry–standard four–pin IEEE Std. 1149.1-1990 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The MAX 3000A architecture internally generates the high programming voltages required to program its EEPROM cells, allowing in–system programming with only a single 3.3–V power supply. During in–system programming, the I/O pins are tri–stated and weakly pulled–up to eliminate board conflicts. The pull–up value is nominally 50 kΩ.

MAX 3000A devices have an enhanced ISP algorithm for faster programming. These devices also offer an `ISP_Done` bit that ensures safe operation when in–system programming is interrupted. This `ISP_Done` bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board (PCB) with standard pick–and–place equipment before they are programmed. MAX 3000A devices can be programmed by downloading the information via in–circuit testers, embedded processors, the MasterBlaster communications cable, the ByteBlasterMV parallel port download cable, and the BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high–pin–count packages (e.g., QFP packages) due to device handling. MAX 3000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

The Jam STAPL programming and test language can be used to program MAX 3000A devices with in–circuit testers, PCs, or embedded processors.

For more information on using the Jam STAPL programming and test language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)*, *Application Note 122 (Using Jam STAPL for ISP & ICR via an Embedded Processor)* and *AN 111 (Embedded Programming Using the 8051 and Jam Byte-Code)*.

The ISP circuitry in MAX 3000A devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 3000A Device

The time required to program a single MAX 3000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 3000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary–scan register length and device IDCODE information for MAX 3000A devices.

Table 8. MAX 3000A Boundary–Scan Register Length

Device	Boundary–Scan Register Length
EPM3032A	96
EPM3064A	192
EPM3128A	288
EPM3256A	480
EPM3512A	624

Table 9. 32–Bit MAX 3000A Device IDCODE Value *Note (1)*

Device	IDCODE (32 bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM3032A	0001	0111 0000 0011 0010	00001101110	1
EPM3064A	0001	0111 0000 0110 0100	00001101110	1
EPM3128A	0001	0111 0001 0010 1000	00001101110	1
EPM3256A	0001	0111 0010 0101 0110	00001101110	1
EPM3512A	0001	0111 0101 0001 0010	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary–Scan Testing in Altera Devices)* for more information on JTAG BST.

Programmable Speed/Power Control

MAX 3000A devices offer a power–saving mode that supports low-power operation across user–defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 3000A device for either high–speed or low–power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, t_{CPPW} and t_{SEXP} parameters.

Output Configuration

MAX 3000A device outputs can be programmed to meet a variety of system–level requirements.

MultiVolt I/O Interface

The MAX 3000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 3000A devices to connect to systems with differing supply voltages. MAX 3000A devices in all packages can be set for 2.5–V, 3.3–V, or 5.0–V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCIO` pins can be connected to either a 3.3–V or 2.5–V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 2.5–V power supply, the output levels are compatible with 2.5–V systems. When the `VCCIO` pins are connected to a 3.3–V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0–V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}. Inputs can always be driven by 2.5–V, 3.3–V, or 5.0–V signals.

Table 11 summarizes the MAX 3000A MultiVolt I/O support.

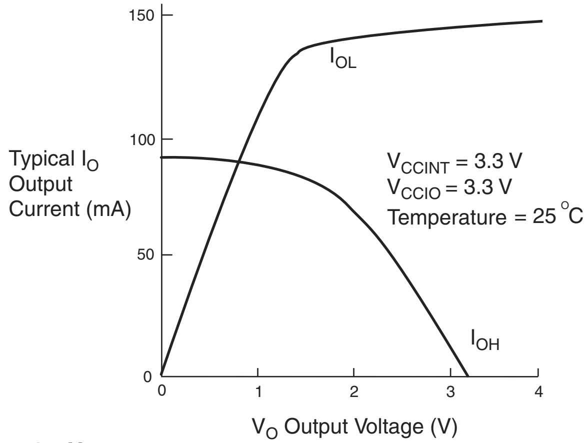
Table 11. MAX 3000A MultiVolt I/O Support

V_{CCIO} Voltage	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓	✓	✓	✓

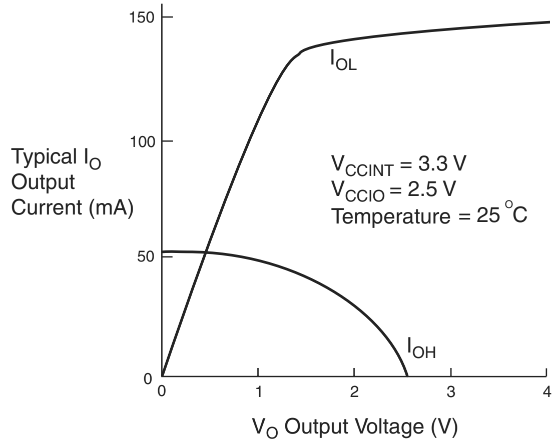
Note:
(1) When V_{CCIO} is 3.3 V, a MAX 3000A device can drive a 2.5–V device that has 3.3–V tolerant inputs.

Figure 9. Output Drive Characteristics of MAX 3000A Devices

3.3 V



2.5 V



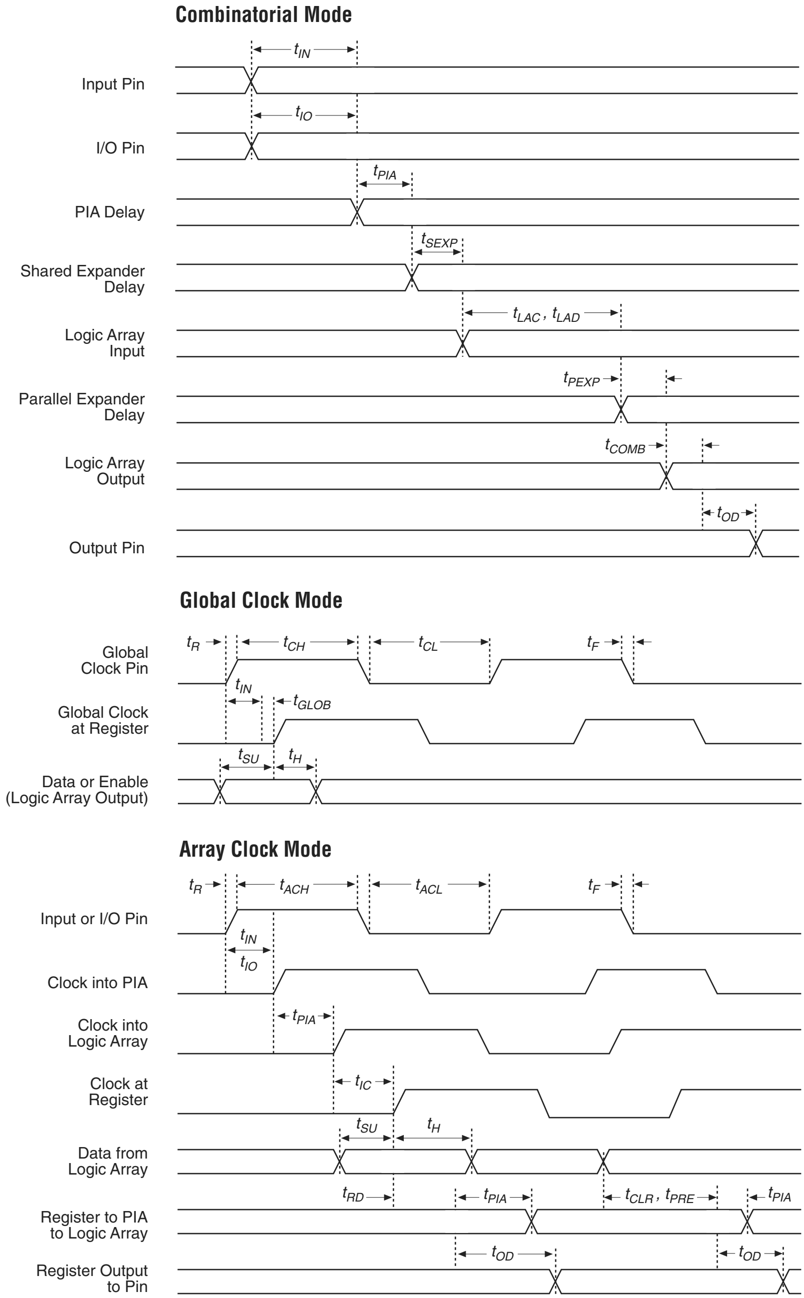
Power Sequencing & Hot–Socketing

Because MAX 3000A devices can be used in a mixed–voltage environment, they have been designed specifically to tolerate any possible power–up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 3000A devices before and during power-up without damaging the device. In addition, MAX 3000A devices do not drive out during power-up. Once operating conditions are reached, MAX 3000A devices operate as specified by the user.

Figure 11. MAX 3000A Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Tables 16 through 23 show EPM3032A, EPM3064A, EPM3128A, EPM3256A, and EPM3512A timing information.

Table 16. EPM3032A External Timing Parameters *Note (1)*									
Symbol	**Parameter**	**Conditions**	**Speed Grade**						**Unit**
			–4		**–7**		**–10**		
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{PD1}	Input to non–registered output	C1 = 35 pF *(2)*		4.5		7.5		10	ns
t_{PD2}	I/O input to non–registered output	C1 = 35 pF *(2)*		4.5		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	2.9		4.7		6.3		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.0	1.0	5.0	1.0	6.7	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.6		2.5		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.3		0.5		0.5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.3	1.0	7.2	1.0	9.4	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.4		7.2		9.7	ns
f_{CNT}	Maximum internal global clock frequency	*(2), (4)*	227.3		138.9		103.1		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.4		7.2		9.7	ns
f_{ACNT}	Maximum internal array clock frequency	*(2), (4)*	227.3		138.9		103.1		MHz

Table 17. EPM3032A Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–4		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{PIA}	PIA delay	*(2)*		0.9		1.5		2.1	ns
t_{LPA}	Low–power adder	*(5)*		2.5		4.0		5.0	ns

Table 18. EPM3064A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–4		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non–registered output	C1 = 35 pF *(2)*		4.5		7.5		10.0	ns
t_{PD2}	I/O input to non–registered output	C1 = 35 pF *(2)*		4.5		7.5		10.0	ns
t_{SU}	Global clock setup time	*(2)*	2.8		4.7		6.2		ns
t_{H}	Global clock hold time	*(2)*	0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.1	1.0	5.1	1.0	7.0	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	1.6		2.6		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.3		0.4		0.6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	4.3	1.0	7.2	1.0	9.6	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(2)*		4.5		7.4		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(2)*, *(4)*	222.2		135.1		100.0		MHz
t_{ACNT}	Minimum array clock period	*(2)*		4.5		7.4		10.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(2)*, *(4)*	222.2		135.1		100.0		MHz

Table 20. EPM3128A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–5		–7		–10		
			Min	Max	Min	Max	Min	Max	
f_{ACNT}	Maximum internal array clock frequency	*(2), (4)*	192.3		129.9		98.0		MHz

Table 21. EPM3128A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			–5		–7		–10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.7		1.0		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.7		1.0		1.4	ns
t_{SEXP}	Shared expander delay			2.0		2.9		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.6		2.4		3.1	ns
t_{LAC}	Logic control array delay			0.7		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.3		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns

Table 22. EPM3256A External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			–7		–10		
			Min	Max	Min	Max	
t_{CNT}	Minimum global clock period	*(2)*		7.9		10.5	ns
f_{CNT}	Maximum internal global clock frequency	*(2), (4)*	126.6		95.2		MHz
t_{ACNT}	Minimum array clock period	*(2)*		7.9		10.5	ns
f_{ACNT}	Maximum internal array clock frequency	*(2), (4)*	126.6		95.2		MHz

Table 23. EPM3256A Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			–7		–10		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.9		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.9		1.2	ns
t_{SEXP}	Shared expander delay			2.8		3.7	ns
t_{PEXP}	Parallel expander delay			0.5		0.6	ns
t_{LAD}	Logic array delay			2.2		2.8	ns
t_{LAC}	Logic control array delay			1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		5.5	ns

Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2) *Note (1)*							
Symbol	**Parameter**	**Conditions**	**Speed Grade**				**Unit**
			-7		**-10**		
			Min	**Max**	**Min**	**Max**	
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.0		6.5	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0	ns
t_{SU}	Register setup time		2.1		3.0		ns
t_{H}	Register hold time		0.6		0.8		ns
t_{FSU}	Register setup time of fast input		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		ns
t_{RD}	Register delay			1.3		1.7	ns
t_{COMB}	Combinatorial delay			0.6		0.8	ns
t_{IC}	Array clock delay			1.8		2.3	ns
t_{EN}	Register enable time			1.0		1.3	ns
t_{GLOB}	Global control delay			1.7		2.2	ns
t_{PRE}	Register preset time			1.0		1.4	ns
t_{CLR}	Register clear time			1.0		1.4	ns
t_{PIA}	PIA delay	*(2)*		3.0		4.0	ns
t_{LPA}	Low-power adder	*(5)*		4.5		5.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.
(2) These values are specified for a PIA fan–out of one LAB (16 macrocells). For each additional LAB fan–out in these devices, add an additional 0.1 ns to the PIA timing value.
(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(4) These parameters are measured with a 16–bit loadable, enabled, up/down counter programmed into each LAB.
(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in low–power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 3000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

I_{CCINT} =

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in the I_{CCINT} equation are:

MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the Quartus II or MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Total number of macrocells in the design, as reported in the RPT File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants (shown in Table 26)

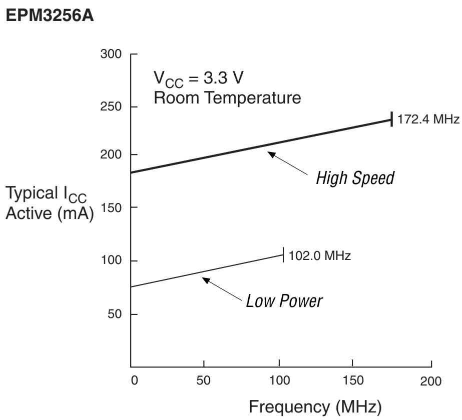
Table 26. MAX 3000A I_{CC} Equation Constants

Device	A	B	C
EPM3032A	0.71	0.30	0.014
EPM3064A	0.71	0.30	0.014
EPM3128A	0.71	0.30	0.014
EPM3256A	0.71	0.30	0.014
EPM3512A	0.71	0.30	0.014

The I_{CCINT} calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16–bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figures 12 and 13 show the typical supply current versus frequency for MAX 3000A devices.

Figure 13. I_{CC} vs. Frequency for MAX 3000A Devices



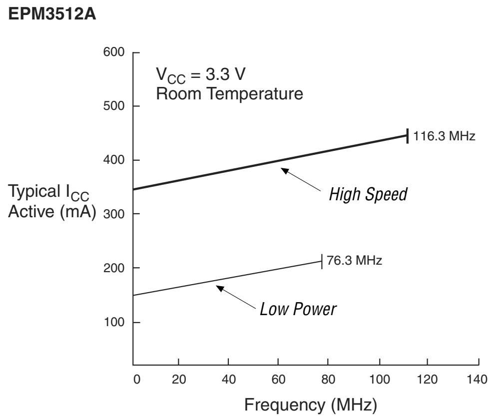


Figure 17. 208–Pin PQFP Package Pin–Out Diagram

Package outline not drawn to scale.