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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	512
Number of Gates	10000
Number of I/O	208
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm3512afc256-10n

...and More Features

- PCI compatible
- Bus–friendly architecture including programmable slew–rate control
- Open–drain output option
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power–saving mode for a power reduction of over 50% in each macrocell
- Configurable expander product–term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- Enhanced architectural features, including:
  - 6 or 10 pin– or logic–driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Programmable output slew–rate control
- Software design support and automatic place–and–route provided by Altera's development systems for Windows–based PCs and Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from third–party manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with the Altera master programming unit (MPU), MasterBlaster™ communications cable, ByteBlasterMV™ parallel port download cable, BitBlaster™ serial download cable as well as programming hardware from third–party manufacturers and any in–circuit tester that supports Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**), Jam STAPL Byte-Code Files (**.jbc**), or Serial Vector Format Files (**.svf**)

General Description

MAX 3000A devices are low–cost, high–performance devices based on the Altera MAX architecture. Fabricated with advanced CMOS technology, the EEPROM–based MAX 3000A devices operate with a 3.3-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 4.5 ns, and counter speeds of up to 227.3 MHz. MAX 3000A devices in the –4, –5, –6, –7, and –10 speed grades are compatible with the timing requirements of the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See Table 2.

Table 2. MAX 3000A Speed Grades

Device	Speed Grade				
	−4	−5	−6	−7	−10
EPM3032A	✓			✓	✓
EPM3064A	✓			✓	✓
EPM3128A		✓		✓	✓
EPM3256A				✓	✓
EPM3512A				✓	✓

The MAX 3000A architecture supports 100% transistor-to-transistor logic (TTL) emulation and high–density small-scale integration (SSI), medium-scale integration (MSI), and large-scale integration (LSI) logic functions. The MAX 3000A architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 3000A devices are available in a wide range of packages, including PLCC, PQFP, and TQFP packages. See Table 3.

Table 3. MAX 3000A Maximum User I/O Pins   Note (1)

| Device	44–Pin PLCC	44–Pin TQFP	100–Pin TQFP	144–Pin TQFP	208–Pin PQFP	256-Pin FineLine BGA
EPM3032A	34	34				
EPM3064A	34	34	66			
EPM3128A			80	96		98
EPM3256A				116	158	161
EPM3512A					172	208

Note:
(1)   When the IEEE Std. 1149.1 (JTAG) interface is used for in–system programming or boundary–scan testing, four I/O pins become JTAG pins.

MAX 3000A devices use CMOS EEPROM cells to implement logic functions. The user–configurable MAX 3000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debugging cycles, and can be programmed and erased up to 100 times.

Macrocells

MAX 3000A macrocells can be individually configured for either sequential or combinatorial logic operation. Macrocells consist of three functional blocks: logic array, product–term select matrix, and programmable register. Figure 2 shows a MAX 3000A macrocell.

Figure 2. MAX 3000A Macrocell
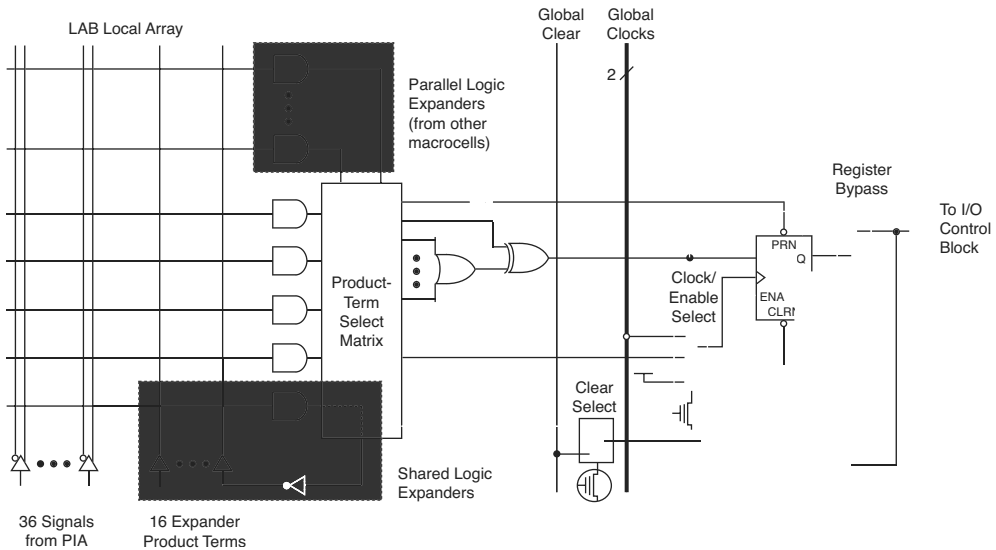
Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product–term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

■ Shareable expanders, which are inverted product terms that are fed back into the logic array
■ Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product–term allocation according to the logic requirements of the design.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The Altera development system compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms, and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower–numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest–numbered macrocell can only lend parallel expanders and the highest–numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 3000A Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.
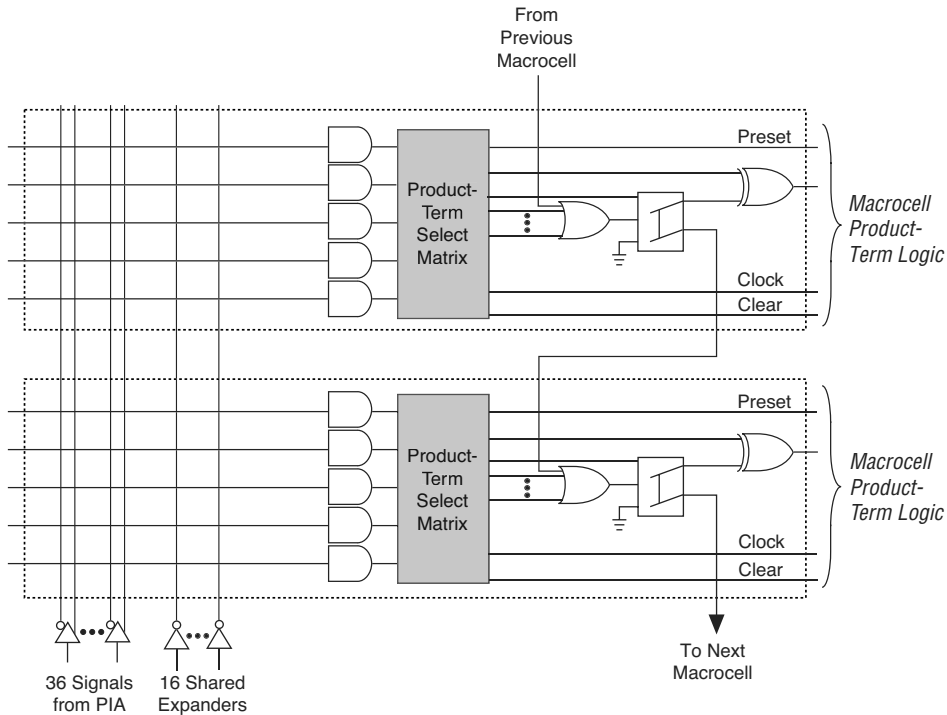
Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 3000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 3000A device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 3000A Device

The time required to program a single MAX 3000A device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:
t_{PROG}	= Programming time
t_{PPULSE}	= Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$	= Number of TCK cycles to program a device
f_{TCK}	= TCK frequency

The ISP times for a stand-alone verification of a single MAX 3000A device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:
t_{VER}	= Verify time
t_{VPULSE}	= Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$	= Number of TCK cycles to verify a device

The programming times described in Tables 4 through 6 are associated with the worst-case method using the enhanced ISP algorithm.

Table 4. MAX 3000A t_{PULSE} & Cycle$_{TCK}$ Values				
Device	**Programming**		**Stand-Alone Verification**	
	t_{PPULSE} (s)	Cycle$_{PTCK}$	t_{VPULSE} (s)	Cycle$_{VTCK}$
EPM3032A	2.00	55,000	0.002	18,000
EPM3064A	2.00	105,000	0.002	35,000
EPM3128A	2.00	205,000	0.002	68,000
EPM3256A	2.00	447,000	0.002	149,000
EPM3512A	2.00	890,000	0.002	297,000

Tables 5 and 6 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 5. MAX 3000A In-System Programming Times for Different Test Clock Frequencies									
Device	f_{TCK}								**Units**
	10 MHz	**5 MHz**	**2 MHz**	**1 MHz**	**500 kHz**	**200 kHz**	**100 kHz**	**50 kHz**	
EPM3032A	2.01	2.01	2.03	2.06	2.11	2.28	2.55	3.10	s
EPM3064A	2.01	2.02	2.05	2.11	2.21	2.53	3.05	4.10	s
EPM3128A	2.02	2.04	2.10	2.21	2.41	3.03	4.05	6.10	s
EPM3256A	2.05	2.09	2.23	2.45	2.90	4.24	6.47	10.94	s
EPM3512A	2.09	2.18	2.45	2.89	3.78	6.45	10.90	19.80	s

Table 6. MAX 3000A Stand-Alone Verification Times for Different Test Clock Frequencies									
Device	f_{TCK}								**Units**
	10 MHz	**5 MHz**	**2 MHz**	**1 MHz**	**500 kHz**	**200 kHz**	**100 kHz**	**50 kHz**	
EPM3032A	0.00	0.01	0.01	0.02	0.04	0.09	0.18	0.36	s
EPM3064A	0.01	0.01	0.02	0.04	0.07	0.18	0.35	0.70	s
EPM3128A	0.01	0.02	0.04	0.07	0.14	0.34	0.68	1.36	s
EPM3256A	0.02	0.03	0.08	0.15	0.30	0.75	1.49	2.98	s
EPM3512A	0.03	0.06	0.15	0.30	0.60	1.49	2.97	5.94	s

The instruction register length of MAX 3000A devices is 10 bits. The IDCODE and USERCODE register length is 32 bits. Tables 8 and 9 show the boundary–scan register length and device IDCODE information for MAX 3000A devices.

Table 8. MAX 3000A Boundary–Scan Register Length

Device	Boundary–Scan Register Length
EPM3032A	96
EPM3064A	192
EPM3128A	288
EPM3256A	480
EPM3512A	624

Table 9. 32–Bit MAX 3000A Device IDCODE Value   *Note (1)*

Device	IDCODE (32 bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM3032A	0001	0111 0000 0011 0010	00001101110	1
EPM3064A	0001	0111 0000 0110 0100	00001101110	1
EPM3128A	0001	0111 0001 0010 1000	00001101110	1
EPM3256A	0001	0111 0010 0101 0110	00001101110	1
EPM3512A	0001	0111 0101 0001 0010	00001101110	1

Notes:
(1)   The most significant bit (MSB) is on the left.
(2)   The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary–Scan Testing in Altera Devices)* for more information on JTAG BST.

Programmable Speed/Power Control

MAX 3000A devices offer a power–saving mode that supports low-power operation across user–defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 3000A device for either high–speed or low–power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, t_{CPPW} and t_{SEXP} parameters.

Output Configuration

MAX 3000A device outputs can be programmed to meet a variety of system–level requirements.

MultiVolt I/O Interface

The MAX 3000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 3000A devices to connect to systems with differing supply voltages. MAX 3000A devices in all packages can be set for 2.5–V, 3.3–V, or 5.0–V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3–V or 2.5–V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5–V power supply, the output levels are compatible with 2.5–V systems. When the VCCIO pins are connected to a 3.3–V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0–V systems. Devices operating with V_{CCIO} levels lower than 3.0 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}. Inputs can always be driven by 2.5–V, 3.3–V, or 5.0–V signals.

Table 11 summarizes the MAX 3000A MultiVolt I/O support.

Table 11. MAX 3000A MultiVolt I/O Support						
V_{CCIO} **Voltage**	**Input Signal (V)**			**Output Signal (V)**		
	2.5	**3.3**	**5.0**	**2.5**	**3.3**	**5.0**
2.5	✓	✓	✓	✓		
3.3	✓	✓	✓	✓	✓	✓

Note:

(1)   When V_{CCIO} is 3.3 V, a MAX 3000A device can drive a 2.5–V device that has 3.3–V tolerant inputs.

Open–Drain Output Option

MAX 3000A devices provide an optional open–drain (equivalent to open-collector) output for each I/O pin. This open–drain output enables the device to provide system–level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired–OR plane.

Open-drain output pins on MAX 3000A devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a high V_{IH}. When the open-drain pin is active, it will drive low. When the pin is inactive, the resistor will pull up the trace to 5.0 V, thereby meeting CMOS requirements. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor

Slew–Rate Control

The output buffer for each MAX 3000A I/O pin has an adjustable output slew rate that can be configured for low–noise or high–speed performance. A faster slew rate provides high–speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low–noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin–by–pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Design Security

All MAX 3000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 3000A devices are fully tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 8. Test patterns can be used and then erased during early stages of the production flow.

Table 15. MAX 3000A Device Capacitance   *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:
(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(4) These values are specified under the recommended operating conditions, as shown in Table 13 on page 23.
(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high–level TTL or CMOS output current.
(6) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low–level TTL, PCI, or CMOS output current.
(7) This value is specified during normal device operation. During power-up, the maximum leakage current is ±300 μA.
(8) This pull–up exists while devices are programmed in–system and in unprogrammed devices during power–up.
(9) Capacitance is measured at 25° C and is sample–tested only. The OE1 pin (high–voltage pin during programming) has a maximum capacitance of 20 pF.
(10) The POR time for all MAX 3000A devices does not exceed 100 μs. The sufficient V_{CCINT} voltage level for POR is 3.0 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
(11) These devices support in-system programming for –40° to 100° C. For in-system programming support between –40° and 0° C, contact Altera Applications.

Figure 9 shows the typical output drive characteristics of MAX 3000A devices.

Table 19. EPM3064A Internal Timing Parameters (Part 1 of 2)   Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		**−7**		**−10**		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		1.1		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.6		1.1		1.4	ns
t_{SEXP}	Shared expander delay			1.8		3.0		3.9	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.5		2.5		3.2	ns
t_{LAC}	Logic control array delay			0.6		1.0		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.3		1.8	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.3		1.8		2.3	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.3		6.8	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.0		2.9		ns
t_{H}	Register hold time		0.6		1.0		1.3		ns
t_{RD}	Register delay			0.7		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.6		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.9		2.5	ns
t_{EN}	Register enable time			0.6		1.0		1.2	ns
t_{GLOB}	Global control delay			1.0		1.5		2.2	ns
t_{PRE}	Register preset time			1.3		2.1		2.9	ns

Table 19. EPM3064A Internal Timing Parameters (Part 2 of 2) Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			−4		−7		−10		
			Min	Max	Min	Max	Min	Max	
t_{CLR}	Register clear time			1.3		2.1		2.9	ns
t_{PIA}	PIA delay	(2)		1.0		1.7		2.3	ns
t_{LPA}	Low–power adder	(5)		3.5		4.0		5.0	ns

Table 20. EPM3128A External Timing Parameters Note (1)

Symbol	Parameter	Conditions	Speed Grade						Unit
			−5		−7		−10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non–registered output	C1 = 35 pF (2)		5.0		7.5		10	ns
t_{PD2}	I/O input to non–registered output	C1 = 35 pF (2)		5.0		7.5		10	ns
t_{SU}	Global clock setup time	(2)	3.3		4.9		6.6		ns
t_{H}	Global clock hold time	(2)	0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.4	1.0	5.0	1.0	6.6	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	(2)	1.8		2.8		3.8		ns
t_{AH}	Array clock hold time	(2)	0.2		0.3		0.4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF (2)	1.0	4.9	1.0	7.1	1.0	9.4	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	(3)	2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	(2)		5.2		7.7		10.2	ns
f_{CNT}	Maximum internal global clock frequency	(2), (4)	192.3		129.9		98.0		MHz
t_{ACNT}	Minimum array clock period	(2)		5.2		7.7		10.2	ns

Table 21. EPM3128A Internal Timing Parameters (Part 2 of 2)   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			−5		**−7**		**−10**		
			Min	Max	Min	Max	Min	Max	
t_{SU}	Register setup time		1.4		2.1		2.9		ns
t_H	Register hold time		0.6		1.0		1.3		ns
t_{RD}	Register delay			0.8		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.9		1.3	ns
t_{IC}	Array clock delay			1.2		1.7		2.2	ns
t_{EN}	Register enable time			0.7		1.0		1.3	ns
t_{GLOB}	Global control delay			1.1		1.6		2.0	ns
t_{PRE}	Register preset time			1.4		2.0		2.7	ns
t_{CLR}	Register clear time			1.4		2.0		2.7	ns
t_{PIA}	PIA delay	*(2)*		1.4		2.0		2.6	ns
t_{LPA}	Low–power adder	*(5)*		4.0		4.0		5.0	ns

Table 22. EPM3256A External Timing Parameters   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		**−10**		
			Min	Max	Min	Max	
t_{PD1}	Input to non–registered output	C1 = 35 pF *(2)*		7.5		10	ns
t_{PD2}	I/O input to non–registered output	C1 = 35 pF *(2)*		7.5		10	ns
t_{SU}	Global clock setup time	*(2)*	5.2		6.9		ns
t_H	Global clock hold time	*(2)*	0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	4.8	1.0	6.4	ns
t_{CH}	Global clock high time		3.0		4.0		ns
t_{CL}	Global clock low time		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(2)*	2.7		3.6		ns
t_{AH}	Array clock hold time	*(2)*	0.3		0.5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(2)*	1.0	7.3	1.0	9.7	ns
t_{ACH}	Array clock high time		3.0		4.0		ns
t_{ACL}	Array clock low time		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	3.0		4.0		ns

Table 22. EPM3256A External Timing Parameters   Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		**−10**		
			Min	Max	Min	Max	
t_{CNT}	Minimum global clock period	(2)		7.9		10.5	ns
f_{CNT}	Maximum internal global clock frequency	(2), (4)	126.6		95.2		MHz
t_{ACNT}	Minimum array clock period	(2)		7.9		10.5	ns
f_{ACNT}	Maximum internal array clock frequency	(2), (4)	126.6		95.2		MHz

Table 23. EPM3256A Internal Timing Parameters (Part 1 of 2)   Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			−7		**−10**		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.9		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.9		1.2	ns
t_{SEXP}	Shared expander delay			2.8		3.7	ns
t_{PEXP}	Parallel expander delay			0.5		0.6	ns
t_{LAD}	Logic array delay			2.2		2.8	ns
t_{LAC}	Logic control array delay			1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0	ns
t_{OD1}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		1.2		1.6	ns
t_{OD2}	Output buffer and pad delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		1.7		2.1	ns
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		5.5	ns

Table 25. EPM3512A Internal Timing Parameters (Part 2 of 2)							Note (1)
Symbol	Parameter	Conditions	Speed Grade				Unit
			-7		-10		
			Min	Max	Min	Max	
t_{OD3}	Output buffer and pad delay, slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		6.0		6.5	ns
t_{ZX1}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay, slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay, slow slew rate = on V_{CCIO} = 3.3 V	C1 = 35 pF		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0	ns
t_{SU}	Register setup time		2.1		3.0		ns
t_H	Register hold time		0.6		0.8		ns
t_{FSU}	Register setup time of fast input		1.6		1.6		ns
t_{FH}	Register hold time of fast input		1.4		1.4		ns
t_{RD}	Register delay			1.3		1.7	ns
t_{COMB}	Combinatorial delay			0.6		0.8	ns
t_{IC}	Array clock delay			1.8		2.3	ns
t_{EN}	Register enable time			1.0		1.3	ns
t_{GLOB}	Global control delay			1.7		2.2	ns
t_{PRE}	Register preset time			1.0		1.4	ns
t_{CLR}	Register clear time			1.0		1.4	ns
t_{PIA}	PIA delay	(2)		3.0		4.0	ns
t_{LPA}	Low-power adder	(5)		4.5		5.0	ns

Notes to tables:
(1) These values are specified under the recommended operating conditions, as shown in Table 13 on page 23. See Figure 11 on page 27 for more information on switching waveforms.
(2) These values are specified for a PIA fan–out of one LAB (16 macrocells). For each additional LAB fan–out in these devices, add an additional 0.1 ns to the PIA timing value.
(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(4) These parameters are measured with a 16–bit loadable, enabled, up/down counter programmed into each LAB.
(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, **t_{ACL}**, and **t_{CPPW}** parameters for macrocells running in low–power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX}, in MHz) for MAX 3000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times f_{MAX} \times tog_{LC})$$

The parameters in the I_{CCINT} equation are:

MC_{TON}	=	Number of macrocells with the Turbo Bit™ option turned on, as reported in the Quartus II or MAX+PLUS II Report File (**.rpt**)
MC_{DEV}	=	Number of macrocells in the device
MC_{USED}	=	Total number of macrocells in the design, as reported in the RPT File
f_{MAX}	=	Highest clock frequency to the device
tog_{LC}	=	Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C	=	Constants (shown in Table 26)

Table 26. MAX 3000A I_{CC} Equation Constants

Device	A	B	C
EPM3032A	0.71	0.30	0.014
EPM3064A	0.71	0.30	0.014
EPM3128A	0.71	0.30	0.014
EPM3256A	0.71	0.30	0.014
EPM3512A	0.71	0.30	0.014

The I_{CCINT} calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16–bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figures 12 and 13 show the typical supply current versus frequency for MAX 3000A devices.
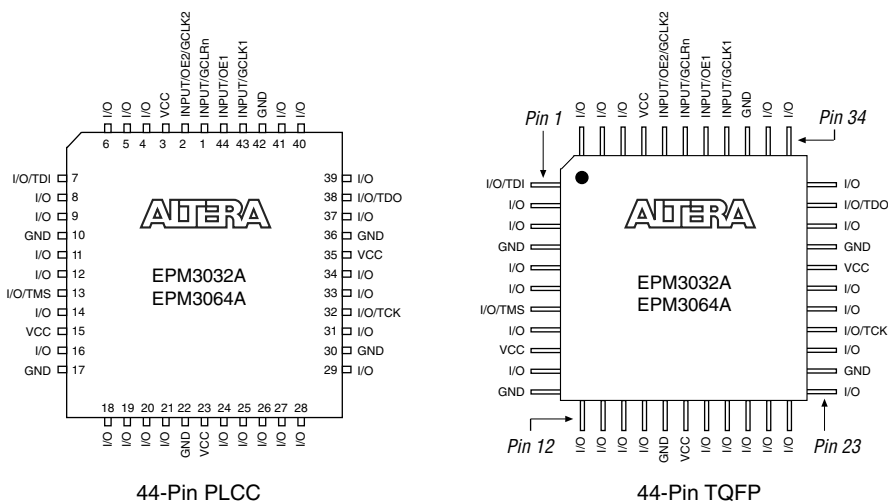
Device Pin–Outs

See the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin–out information.

Figures 14 through 18 show the package pin–out diagrams for MAX 3000A devices.

Figure 14. 44–Pin PLCC/TQFP Package Pin–Out Diagram

Package outlines not drawn to scale.

44-Pin PLCC

44-Pin TQFP

Figure 17. 208–Pin PQFP Package Pin–Out Diagram

Package outline not drawn to scale.