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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f65k90-i-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Pin Number Pin Buffer		Description		
Fill Name	TQFP	Туре	Туре	Description
				PORTJ is a bidirectional I/O port.
RJ0	62	I/O	ST	Digital I/O.
RJ1/SEG33 RJ1 SEG33	61	I/O O	ST Analog	Digital I/O. SEG33 output for LCD.
RJ2/SEG34 RJ2 SEG34	60	I/O O	ST Analog	Digital I/O. SEG34 output for LCD.
RJ3/SEG35 RJ3 SEG35	59	I/O O	ST Analog	Digital I/O. SEG35 output for LCD.
RJ4/SEG39 RJ4 SEG39	39	I/O O	ST Analog	Digital I/O. SEG39 output for LCD.
RJ5/SEG38 RJ5 SEG38	40	I/O O	ST Analog	Digital I/O SEG38 output for LCD.
RJ6/SEG37 RJ6 SEG37	41	I/O O	ST Analog	Digital I/O. SEG37 output for LCD.
RJ7/SEG36 RJ7 SEG36	42	I/O O	ST Analog	Digital I/O. SEG36 output for LCD.
Vss	11, 31, 51, 70	Р	—	Ground reference for logic and I/O pins.
VDD	32, 48, 71	Р	—	Positive supply for logic and I/O pins.
AVss	26	Р	—	Ground reference for analog modules.
AVDD	25	Р	—	Positive supply for analog modules.
ENVREG	24	I	ST	Enable for on-chip voltage regulator.
	12			Core logic power or external filter capacitor connection.
VCAP		Р	—	External filter capacitor connection (regulator enabled/disabled).
Legend: TTL = TTL co ST = Schmi I = Input P = Power $I^2C^{TM} = I^2C/SM$	ompatible input tt Trigger input IBus	with C	MOS leve	CMOS = CMOS compatible input or output Analog = Analog input O = Output OD = Open-Drain (no P diode to VDD)

TABLE 1-4:	PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

3: Not available on PIC18F65K90 and PIC18F85K90 devices.

4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

3.0 OSCILLATOR CONFIGURATIONS

3.1 Oscillator Types

The PIC18F87K90 family of devices can be operated in the following oscillator modes:

- EC External Clock, RA6 available
- ECIO External Clock, Clock Out RA6 (Fosc/4 on RA6)
- HS High-Speed Crystal/Resonator
- XT Crystal/Resonator
- LP Low-Power Crystal
- RC External Resistor/Capacitor, RA6 available
- RCIO External Resistor/Capacitor, Clock Out RA6 (Fosc/4 on RA6)
- INTIO2 Internal Oscillator with I/O on RA6 and RA7
- INTIO1 Internal Oscillator with Fosc/4 Output on RA6 and I/O on RA7

There is also an option for running the 4xPLL on any of the clock sources in the input frequency range of 4 to 16 MHz.

The PLL is enabled by setting the PLLCFG bit (CONFIG1H<4>) or the PLLEN bit (OSCTUNE<6>).

For the EC and HS mode, the PLLEN (software) or PLLCFG (CONFIG) bit can be used to enable the PLL.

For the INTIOx modes (HF-INTOSC):

- Only the PLLEN can enable the PLL (PLLCFG is ignored).
- When the oscillator is configured for the internal oscillator (OSC<3:0> = 100x), the PLL can be enabled only when the HF-INTOSC frequency is 8 or 16 MHz.

When the RA6 and RA7 pins are not used for an oscillator function or CLKOUT function, they are available as general purpose I/Os. To optimize power consumption when using EC/HS/ XT/LP/RC as the primary oscillator, the frequency input range can be configured to yield an optimized power bias:

- Low-Power Bias External frequency less than 160 kHz
- Medium Power Bias External frequency between 160 kHz and 16 MHz
- High-Power Bias External frequency greater than 16 MHz

All of these modes are selected by the user by programming the OSC<3:0> Configuration bits (CONFIG1H<3:0>). In addition, PIC18F87K90 family devices can switch between different clock sources, either under software control or under certain conditions, automatically. This allows for additional power savings by managing device clock speed in real time without resetting the application. The clock sources for the PIC18F87K90 family of devices are shown in Figure 3-1.

For the HS and EC mode, there are additional power modes of operation – depending on the frequency of operation.

HS1 is the Medium Power mode with a frequency range of 4 MHz to 16 MHz. HS2 is the High-Power mode where the oscillator frequency can go from 16 MHz to 25 MHz. HS1 and HS2 are achieved by setting the CONFIG1H<3:0> correctly. (For details, see Register 28-2 on page 428.)

EC mode has these modes of operation:

- EC1 For low power with a frequency range up to 160 kHz
- EC2 Medium power with a frequency range of 160 kHz to 16 MHz
- EC3 High power with a frequency range of 16 MHz to 64 MHz

EC1, EC2 and EC3 are achieved by setting the CONFIG1H<3:0> correctly. (For details, see Register 28-2 on page 428.)

Table 3-1 shows the HS and EC modes' frequency range and OSC<3:0> settings.

6.3 Data Memory Organization

Note:	The operation of some aspects of data
	memory are changed when the PIC18
	extended instruction set is enabled. See
	Section 6.6 "Data Memory and the
	Extended Instruction Set" for more
	information.

The data memory in PIC18 devices is implemented as static RAM. Each register in the data memory has a 12-bit address, allowing up to 4,096 bytes of data memory. The memory space is divided into as many as 16 banks that contain 256 bytes each. PIC18FX6K90 and PIC18FX7K90 devices implement all 16 complete banks, for a total of 4 Kbytes. PIC18FX5K90 devices implement only the first eight complete banks, for a total of 2 Kbytes.

Figure 6-6 and Figure 6-7 show the data memory organization for the devices.

The data memory contains Special Function Registers (SFRs) and General Purpose Registers (GPRs). The SFRs are used for control and status of the controller and peripheral functions, while GPRs are used for data storage and scratchpad operations in the user's application. Any read of an unimplemented location will read as '0's.

The instruction set and architecture allow operations across all banks. The entire data memory may be accessed by Direct, Indirect or Indexed Addressing modes. Addressing modes are discussed later in this section.

To ensure that commonly used registers (select SFRs and select GPRs) can be accessed in a single cycle, PIC18 devices implement an Access Bank. This is a 256-byte memory space that provides fast access to select SFRs and the lower portion of GPR Bank 0 without using the Bank Select Register. For details on the Access RAM, see **Section 6.3.2 "Access Bank"**.

6.3.1 BANK SELECT REGISTER

Large areas of data memory require an efficient addressing scheme to make possible rapid access to any address. Ideally, this means that an entire address does not need to be provided for each read or write operation. For PIC18 devices, this is accomplished with a RAM banking scheme. This divides the memory space into 16 contiguous banks of 256 bytes. Depending on the instruction, each location can be addressed directly by its full 12-bit address, or an 8-bit, low-order address and a 4-bit Bank Pointer.

Most instructions in the PIC18 instruction set make use of the Bank Pointer, known as the Bank Select Register (BSR). This SFR holds the four Most Significant bits of a location's address. The instruction itself includes the eight Least Significant bits. Only the four lower bits of the BSR are implemented (BSR<3:0>). The upper four bits are unused, always read as '0' and cannot be written to. The BSR can be loaded directly by using the MOVLB instruction.

The value of the BSR indicates the bank in data memory. The eight bits in the instruction show the location in the bank and can be thought of as an offset from the bank's lower boundary. The relationship between the BSR's value and the bank division in data memory is shown in Figure 6-7.

Since up to 16 registers may share the same low-order address, the user must always be careful to ensure that the proper bank is selected before performing a data read or write. For example, writing what should be program data to an 8-bit address of F9h while the BSR is 0Fh, will end up resetting the Program Counter.

While any bank can be selected, only those banks that are actually implemented can be read or written to. Writes to unimplemented banks are ignored, while reads from unimplemented banks will return '0's. Even so, the STATUS register will still be affected as if the operation was successful. The data memory map in Figure 6-6 indicates which banks are implemented.

In the core PIC18 instruction set, only the MOVFF instruction fully specifies the 12-bit address of the source and target registers. When this instruction executes, it ignores the BSR completely. All other instructions include only the low-order address as an operand and must use either the BSR or the Access Bank to locate their target registers.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	78
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	78
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	78
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	INTEDG3	TMR0IP	INT3IP	RBIP	75
INTCON3	INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF	75
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE09	SE08	83
LCDSE3	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	83

TABLE 11-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Legend: Shaded cells are not used by PORTB.

IADLE II	-13. 301010		EGISTER	S ASSUCI		HFURIF			
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1		78
LATF	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	—	78
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—	78
ANCON0	ANSEL7	ANSEL6	ANSEL5	ANSEL4	ANSEL3	ANSEL2	ANSEL1	ANSEL0	81
ANCON1	ANSEL15	ANSEL14	ANSEL13	ANSEL12	ANSEL11	ANSEL10	ANSEL9	ANSEL8	81
CMSTAT	CMP3OUT	CMP2OUT	CMP10UT	—		—	_	—	77
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	77
LCDSE2	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	83
LCDSE3	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	83

TABLE 11-13: SUMMARY OF REGISTERS ASSOCIATED WITH PORTF

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTF.

15.0 TIMER3/5/7 MODULES

The Timer3/5/7 timer/counter modules incorporate these features:

- Software-selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMRxH and TMRxL)
- Selectable clock source (internal or external) with device clock or SOSC oscillator internal options
- Interrupt-on-overflow
- · Module Reset on ECCP Special Event Trigger

Timer7 is unimplemented for devices with a program memory of 32 Kbytes (PIC18FX5K90).

Note: Throughout this section, generic references are used for register and bit names that are the same, except for an 'x' variable that indicates the item's association with the Timer3, Timer5 or Timer7 module. For example, the control register is named TxCON and refers to T3CON, T5CON and T7CON.

A simplified block diagram of the Timer3/5/7 module is shown in Figure 15-1.

The Timer3/5/7 module is controlled through the TxCON register (Register 15-1). It also selects the clock source options for the ECCP modules. (For more information, see **Section 19.1.1 "ECCP Module and Timer Resources"**.)

The Fosc clock source should not be used with the ECCP capture/compare features. If the timer will be used with the capture or compare features, always select one of the other timer clocking options.

17.2.4 LEAP YEAR

Since the year range on the RTCC module is 2000 to 2099, the leap year calculation is determined by any year divisible by four in the above range. Only February is affected in a leap year.

February will have 29 days in a leap year and 28 days in any other year.

17.2.5 GENERAL FUNCTIONALITY

All Timer registers containing a time value of seconds or greater are writable. The user configures the time by writing the required year, month, day, hour, minutes and seconds to the Timer registers, via Register Pointers. (See Section 17.2.8 "Register Mapping".)

The timer uses the newly written values and proceeds with the count from the required starting point.

The RTCC is enabled by setting the RTCEN bit (RTCCFG<7>). If enabled, while adjusting these registers, the timer still continues to increment. However, any time the MINSEC register is written to, both of the timer prescalers are reset to '0'. This allows fraction of a second synchronization.

The Timer registers are updated in the same cycle as the write instruction's execution by the CPU. The user must ensure that when RTCEN = 1, the updated registers will not be incremented at the same time. This can be accomplished in several ways:

- By checking the RTCSYNC bit (RTCCFG<4>)
- By checking the preceding digits from which a carry can occur
- By updating the registers immediately following the seconds pulse (or an alarm interrupt)

The user has visibility to the half-second field of the counter. This value is read-only and can be reset only by writing to the lower half of the SECONDS register.

17.2.6 SAFETY WINDOW FOR REGISTER READS AND WRITES

The RTCSYNC bit indicates a time window during which the RTCC Clock Domain registers can be safely read and written without concern about a rollover. When RTCSYNC = 0, the registers can be safely accessed by the CPU.

Whether RTCSYNC = 1 or 0, the user should employ a firmware solution to ensure that the data read did not fall on a rollover boundary, resulting in an invalid or partial read. This firmware solution would consist of reading each register twice and then comparing the two values. If the two values matched, then a rollover did not occur.

17.2.7 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RTCCFG<5>) must be set.

To avoid accidental writes to the RTCC Timer register, it is recommended that the RTCWREN bit (RTCCFG<5>) be kept clear when not writing to the register. For the RTCWREN bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN. For that reason, it is recommended that users follow the code example in Example 17-1.

EXAMPLE 17-1: SETTING THE RTCWREN BIT

movlw	0x55	
movwf	EECON2	
movlw	0xAA	
movwf	EECON2	
bsf	RTCCFG, RTCWREN	

17.2.8 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Timer registers are accessed through corresponding Register Pointers. The RTCC Value register window (RTCVALH and RTCVALL) uses the RTCPTRx bits (RTCCFG<1:0>) to select the required Timer register pair.

By reading or writing to the RTCVALH register, the RTCC Pointer value (RTCPTR<1:0>) decrements by '1' until it reaches '00'. When '00' is reached, the MINUTES and SECONDS value is accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

TABLE 17-3:	RTCVALH AND RTCVALL
	REGISTER MAPPING

	RTCC Value Register Window				
RICFIRCI.0>	RTCVALH	RTCVALL			
00	MINUTES	SECONDS			
01	WEEKDAY	HOURS			
10	MONTH	DAY			
11	—	YEAR			

The Alarm Value register windows (ALRMVALH and ALRMVALL) use the ALRMPTR bits (ALRMCFG<1:0>) to select the desired alarm register pair.

By reading or writing to the ALRMVALH register, the Alarm Pointer value, ALRMPTR<1:0>, decrements by one until it reaches '00'. When it reaches '00', the ALRMMIN and ALRMSEC value is accessible through ALRMVALH and ALRMVALL until the pointer value is manually changed.



When a shutdown event occurs, two things happen:

- The ECCPxASE bit is set to '1'. The ECCPxASE will remain set until cleared in firmware or an auto-restart occurs. (See Section 19.4.5 "Auto-Restart Mode".)
- The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs: PxA/PxC and PxB/PxD. The state of each pin pair is determined by the PSSxAC and PSSxBD bits (ECCPxAS<3:2> and <1:0>, respectively).

Each pin pair may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

REGISTER 19-3: ECCPxAS: ECCPx AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPxASE	ECCPxAS2	ECCPxAS1	ECCPxAS0	PSSxAC1	PSSxAC0	PSSxBD1	PSSxBD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	ECCPxASE: ECCP Auto-Shutdown Event Status bit
	 1 = A shutdown event has occurred; ECCP outputs are in a shutdown state 0 = ECCP outputs are operating
bit 6-4	ECCPxAS<2:0>: ECCP Auto-Shutdown Source Select bits
	 000 = Auto-shutdown is disabled 001 = Comparator C10UT output is high 010 = Comparator C20UT output is high 011 = Either Comparator C10UT or C20UT is high 100 = VIL on FLT0 pin 101 = VIL on FLT0 pin or Comparator C10UT output is high 110 = VIL on FLT0 pin or Comparator C20UT output is high 111 = VIL on FLT0 pin, Comparator C10UT or Comparator C20UT is high
bit 3-2	PSSxAC<1:0>: Pins PxA and PxC Shutdown State Control bits
	00 = Drive the PxA and PxC pins to '0' 01 = Drive the PxA and PxC pins to '1' 1x = PxA and PxC pins tri-state
bit 1-0	PSSxBD<1:0>: Pins PxB and PxD Shutdown State Control bits
	00 = Drive the PxB and PxD pins to '0' 01 = Drive the PxB and PxD pins to '1' 1x = PxB and PxD pins tri-state
Note:	The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level present, the auto-shutdown will persist.

Writing to the ECCPxASE bit is disabled while an auto-shutdown condition persists. Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

is



19.4.7.1 Steering Synchronization

The STRSYNC bit of the PSTRxCON register gives the user two choices for when the steering event will happen. When the STRSYNC bit is '0', the steering event will happen at the end of the instruction that writes to the PSTRxCON register. In this case, the output signal at the Px<D:A> pins may be an incomplete PWM waveform. This operation is useful when the user firmware needs to immediately remove a PWM signal from the pin.

When the STRSYNC bit is '1', the effective steering update will happen at the beginning of the next PWM period. In this case, steering on/off the PWM output will always produce a complete PWM waveform.

Figures 19-17 and 19-18 illustrate the timing diagrams of the PWM steering depending on the STRSYNC setting.

FIGURE 19-17: EXAMPLE OF STEERING EVENT AT END OF INSTRUCTION (STRSYNC = 0)



FIGURE 19-18: EXAMPLE OF STEERING EVENT AT BEGINNING OF INSTRUCTION (STRSYNC = 1)









FIGURE 20-14: TYPE-A WAVEFORMS IN 1/3 MUX, 1/3 BIAS DRIVE



21.4.6.1 I²C Master Mode Operation

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDAx while SCLx outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted, 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/\overline{W} bit. In this case, the R/\overline{W} bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address, followed by a '1' to indicate the receive bit. Serial data is received via SDAx, while SCLx outputs the serial clock. Serial data is received, 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

The Baud Rate Generator, used for the SPI mode operation, is used to set the SCLx clock frequency for either 100 kHz, 400 kHz or 1 MHz I²C operation. See **Section 21.4.7 "Baud Rate"** for more details.

A typical transmit sequence would go as follows:

- 1. The user generates a Start condition by setting the Start Enable bit, SEN (SSPxCON2<0>).
- SSPxIF is set. The MSSPx module will wait the required start time before any other operation takes place.
- 3. The user loads the SSPxBUF with the slave address to transmit.
- 4. Address is shifted out the SDAx pin until all 8 bits are transmitted.
- 5. The MSSPx module shifts in the ACK bit from the slave device and writes its value into the SSPxCON2 register (SSPxCON2<6>).
- The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
- 7. The user loads the SSPxBUF with 8 bits of data.
- 8. Data is shifted out the SDAx pin until all 8 bits are transmitted.
- The MSSPx module shifts in the ACK bit from the slave device and writes its value into the SSPxCON2 register (SSPxCON2<6>).
- 10. The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
- 11. The user generates a Stop condition by setting the Stop Enable bit, PEN (SSPxCON2<2>).
- 12. An interrupt is generated once the Stop condition is complete.

21.4.9 I²C[™] MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit (SSPxCON2<1>) is programmed high and the I²C logic module is in the Idle state. When the RSEN bit is set, the SCLx pin is asserted low. When the SCLx pin is sampled low, the Baud Rate Generator is loaded with the contents of SSPxADD<5:0> and begins counting. The SDAx pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, and if SDAx is sampled high, the SCLx pin will be deasserted (brought high). When SCLx is sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<6:0> and begins counting. SDAx and SCLx must be sampled high for one TBRG. This action is then followed by assertion of the SDAx pin (SDAx = 0) for one TBRG while SCLx is high. Following this, the RSEN bit (SSPxCON2<1>) will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDAx pin held low. As soon as a Start condition is detected on the SDAx and SCLx pins, the S bit (SSPxSTAT<3>) will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

- Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.
 - **2:** A bus collision during the Repeated Start condition occurs if:
 - SDAx is sampled low when SCLx goes from low-to-high.
 - SCLx goes low before SDAx is asserted low. This may indicate that another master is attempting to transmit a data '1'.

Immediately following the SSPxIF bit getting set, the user may write the SSPxBUF with the 7-bit address in 7-bit mode or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode) or eight bits of data (7-bit mode).

21.4.9.1 WCOL Status Flag

If the user writes the SSPxBUF when a Repeated Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing of the lower 5 bits of SSPxCON2 is disabled until the Repeated Start condition is complete.

FIGURE 21-22: REPEATED START CONDITION WAVEFORM



Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	TMR1GIF	TMR2IF	TMR1IF	77
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	TMR1GIE	TMR2IE	TMR1IE	77
IPR1	_	ADIP	RC1IP	TX1IP	SSP1IP	TMR1GIP	TMR2IP	TMR1IP	77
ADRESH	A/D Result	t Register H	igh Byte						76
ADRESL	A/D Result Register Low Byte							76	
ADCON0	_	CHS4	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	76
ADCON1	TRIGSEL1	TRIGSEL0	VCFG1	VCFG0	VNCFG	CHSN2	CHSN1	CHSN0	76
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	76
ANCON0	ANSEL7	ANSEL6	ANSEL5	ANSEL4	ANSEL3	ANSEL2	ANSEL1	ANSEL0	81
ANCON1	ANSEL15	ANSEL14	ANSEL13	ANSEL12	ANSEL11	ANSEL10	ANSEL9	ANSEL8	81
ANCON2	ANSEL23	ANSEL22	ANSEL21	ANSEL20	ANSEL19	ANSEL18	ANSEL17	ANSEL16	81
CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	80
PORTA	RA7 ⁽²⁾	RA6 ⁽²⁾	RA5	RA4	RA3	RA2	RA1	RA0	78
TRISA	TRISA7 ⁽²⁾	TRISA6(2)	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	78
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	—	78
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—	78
PORTG	_	_	RG5 ⁽³⁾	RG4	RG3	RG2	RG1	RG0	78
TRISG	_	—	_	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	78
PORTH ⁽¹⁾	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	78
TRISH ⁽¹⁾	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	78

TABLE 23-2:SUMMARY OF A/D REGISTERS

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: This register is not implemented on 64-pin devices.

2: These bits are available only in certain oscillator modes, when the OSC2 Configuration bit = 0. If that Configuration bit is cleared, this signal is not implemented.

3: This bit is available when Master Clear is disabled (MCLRE = 0). When MCLRE is set, the bit is unimplemented.

REGISTER 28-3: CONFIG2L: CONFIGURATION REGISTER 2 LOW (BYTE ADDRESS 300002h)

U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
_	BORPWR1 ⁽¹⁾	BORPWR0 ⁽¹⁾	BORV1 ⁽¹⁾	BORV0 ⁽¹⁾	BOREN1 ⁽²⁾	BOREN0 ⁽²⁾	PWRTEN ⁽²⁾
bit 7							bit 0

Legend:	P = Programmable bit					
R = Readable bit	W = Writable bit U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 7	Unimplemented: Read as '0'					
bit 6-5	BORPWR<1:0>: BORMV Power Level bits ⁽¹⁾					
	 11 = ZPBORVMV instead of BORMV is selected 10 = BORMV is set to high-power level 01 = BORMV is set to medium-power level 00 = BORMV is set to low-power level 					
bit 4-3	BORV<1:0>: Brown-out Reset Voltage bits ⁽¹⁾					
	11 = VBORMV is set to 1.8V 10 = VBORMV is set to 2.0V 01 = VBORMV is set to 2.7V 00 = VBORMV is set to 3.0V					
bit 2-1	BOREN<1:0>: Brown-out Reset Enable bits ⁽²⁾					
	 11 = Brown-out Reset is enabled in hardware only (SBOREN is disabled) 10 = Brown-out Reset is enabled in hardware only and disabled in Sleep mode (SBOREN is disabled) 01 = Brown-out Reset is enabled and controlled by software (SBOREN is enabled) 00 = Brown-out Reset is disabled in hardware and software 					
bit 0	PWRTEN: Power-up Timer Enable bit ⁽²⁾					
	1 = PWRT is disabled 0 = PWRT is enabled					
Note 1:	For the specifications, see Section 31.1 "DC Characteristics: Supply Voltage PIC18F87K90 Family (Industrial/Extended)".					

2: The Power-up Timer is decoupled from Brown-out Reset, allowing these features to be independently controlled.

R/C-1	R/C-1	R-1	U-0	U-0	U-0	U-0	U-0			
WRTD	WRTB	WRTC ⁽¹⁾	—	_		_	_			
bit 7							bit 0			
Legend:		C = Clearable bit								
R = Readable I	oit	W = Writable	l as '0'							
-n = Value at P	OR	'1' = Bit is set	= Bit is set '0' = Bit is cleared				x = Bit is unknown			
bit 7	WRTD: Data	EEPROM Write	e Protection b	it						
	1 = Data EEPROM is not write-protected									
	0 = Data EEPROM is write-protected									
bit 6	WRTB: Boot Block Write Protection bit									
1 = Boot block is not write-protected										
	0 = Boot block	k is write-prote	cted							
bit 5	it 5 WRTC: Configuration Register Write Protection bit ⁽¹⁾									
	1 = Configuration registers are not write-protected									
	0 = Configuration registers are write-protected									

REGISTER 28-11: CONFIG6H: CONFIGURATION REGISTER 6 HIGH (BYTE ADDRESS 30000Bh)⁽²⁾

bit 4-0 Unimplemented: Read as '0'

Note 1: This bit is read-only in Normal Execution mode; it can be written only in Program mode.

2: For the memory size of the blocks, refer to Figure 28-6.