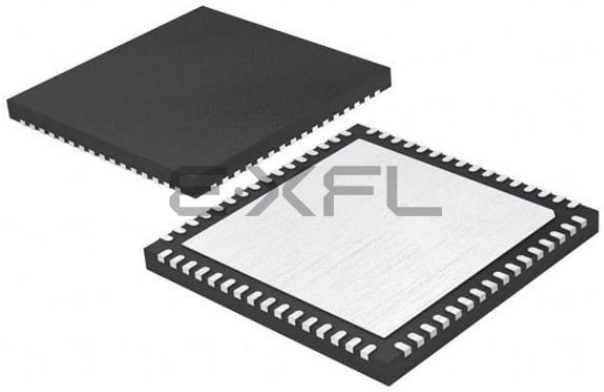

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f65k90-i-mrrsl

TABLE 1-4: PIC18F8XK9 0 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB6/KBI2/PGC	52			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	47			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
I^2C = I ^{2}C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

4.7 Ultra Low-Power Wake-up

The Ultra Low-Power Wake-up (ULPWU) on pin, RA0, allows a slow falling voltage to generate an interrupt without excess current consumption.

To use this feature:

1. Charge the capacitor on RA0 by configuring the RA0 pin to an output and setting it to 1 .
2. Stop charging the capacitor by configuring RA0 as an input.
3. Discharge the capacitor by setting the ULPEN and ULPSINK bits in the WDTCON register.
4. Configure Sleep mode.
5. Enter Sleep mode.

When the voltage on RA0 drops below VIL, the device wakes up and executes the next instruction.

This feature provides a low-power technique for periodically waking up the device from Sleep mode.

The time-out is dependent on the discharge time of the RC circuit on RA0.

When the ULPWU module wakes the device from Sleep mode, the ULPLVL bit (WDTCON<5>) is set. Software can check this bit upon wake-up to determine the wake-up source.

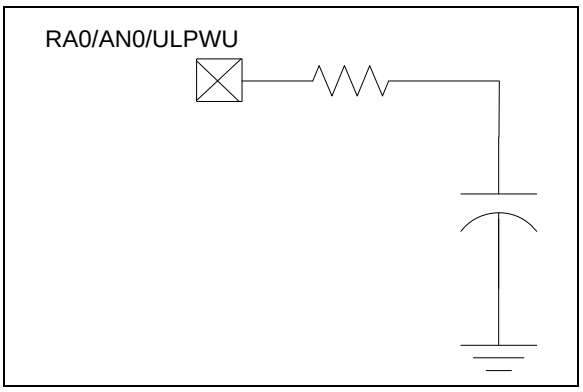
See Example 4-1 for initializing the ULPWU module.

EXAMPLE 4-1: ULTRA LOW-POWER WAKE-UP INITIALIZATION

```
                //****************************
                //Charge the capacitor on RA0
                //****************************
TRISAbits.TRISA0 = 0;
PORTAbits.RA0 = 1;
for(i = 0; i < 10000; i++) Nop();
                //******************************
                //Stop Charging the capacitor
                //on RA0
                //******************************
TRISAbits.TRISA0 = 1;
                //******************************
                //Enable the Ultra Low Power
                //Wakeup module and allow
                //capacitor discharge
                //******************************
WDTCONbits.ULPEN = 1;
WDTCONbits.ULPSINK = 1;
                //For Sleep
OSCCONbits.IDLEN = 0;
                //Enter Sleep Mode
                //
Sleep();
                //for sleep, execution will
                //resume here
```

A series resistor, between RA0 and the external capacitor, provides overcurrent protection for the RA0/AN0/ULPWU pin and enables software calibration of the time-out (see Figure 4-9).

FIGURE 4-9: ULTRA LOW-POWER WAKE-UP INITIALIZATION



A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired delay in Sleep. This technique compensates for the affects of temperature, voltage and component accuracy. The peripheral can also be configured as a simple programmable Low-Voltage Detect (LVD) or temperature sensor.

Note: For more information, see *AN 879, "Using the Microchip Ultra Low-Power Wake-up Module"* (DS00879).

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, **RESET** Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
TOSU	PIC18F6XK90	PIC18F8XK90	---0 0000	---0 0000	---0 uuuu (1)
TOSH	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu (1)
TOSL	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu (1)
STKPTR	PIC18F6XK90	PIC18F8XK90	00-0 0000	uu-0 0000	uu-u uuuu (1)
PCLATU	PIC18F6XK90	PIC18F8XK90	---0 0000	---0 0000	---u uuuu
PCLATH	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PCL	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	PC + 2(2)
TBLPTRU	PIC18F6XK90	PIC18F8XK90	--00 0000	--00 0000	--uu uuuu
TBLPTRH	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
TABLAT	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PRODH	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	PIC18F6XK90	PIC18F8XK90	0000 000x	0000 000u	uuuu uuuu (3)
INTCON2	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu (3)
INTCON3	PIC18F6XK90	PIC18F8XK90	1100 0000	1100 0000	uuuu uuuu (3)
INDF0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTINC0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTDEC0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PREINC0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PLUSW0	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
FSR0H	PIC18F6XK90	PIC18F8XK90	---- 0000	---- 0000	---- uuuu
FSR0L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTINC1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTDEC1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PREINC1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PLUSW1	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
FSR1H	PIC18F6XK90	PIC18F8XK90	---- 0000	---- 0000	---- uuuu
FSR1L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
BSR	PIC18F6XK90	PIC18F8XK90	---- 0000	---- 0000	---- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as 0 , q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for the Reset value for a specific condition.

NOTES:

REGISTER 10-12: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR5GIE	LCDIE(1)	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 7 TMR5GIE: Timer5 Gate Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 6 LCDIE: LCD Interrupt Enable bit(1)
1 = Enabled
0 = Disabled

bit 5 RC2IE: AUSART Receive Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 4 TX2IE: AUSART Transmit Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 3 CTMUIE: CTMU Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 CCP2IE: ECCP2 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 CCP1IE: ECCP1 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 RTCCIE: RTCC Interrupt Enable bit
1 = Enabled
0 = Disabled

Note 1: This bit is valid when the Type-B waveform with Non-Static mode is selected.

REGISTER 10-13: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP10IE(1)	CCP9IE(1)	CCP8IE	CCP7IE	CCP6IE	CCP5IE	CCP4IE	CCP3IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 7-0 CCP10IE:CCP3IE: CCP<10:3> Interrupt Enable bits(1)
1 = Enabled
0 = Disabled

Note 1: CCP10IE and CCP9IE are unimplemented in devices with a program memory of 32 Kbytes (PIC18FX5K90).

REGISTER 10-20: IPR5: PERIPHERAL INTERRUPT PRIORITY REGISTER 5

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR7GIP(1)	TMR12IP(1)	TMR10IP(1)	TMR8IP	TMR7IP(1)	TMR6IP	TMR5IP	TMR4IP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 7 TMR7GIP: TMR7 Gate Interrupt Priority bit(1)
1 = High priority
0 = Low priority

bit 6 TMR12IP: TMR12 to PR12 Match Interrupt Priority bit(1)
1 = High priority
0 = Low priority

bit 5 TMR10IP: TMR10 to PR10 Match Interrupt Priority bit(1)
1 = High priority
0 = Low priority

bit 4 TMR8IP: TMR8 to PR8 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 3 TMR7IP: TMR7 Overflow Interrupt Priority bit(1)
1 = High priority
0 = Low priority

bit 2 TMR6IP: TMR6 to PR6 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1 TMR5IP: TMR5 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

bit 0 TMR4IP: TMR4 to PR4 Match Interrupt Priority bit
1 = High priority
0 = Low priority

Note 1: Unimplemented in devices with a program memory of 32 Kbytes (PIC18FX5K90).

15.5.4 TIMER3/5/7 GATE SINGLE PULSE MODE

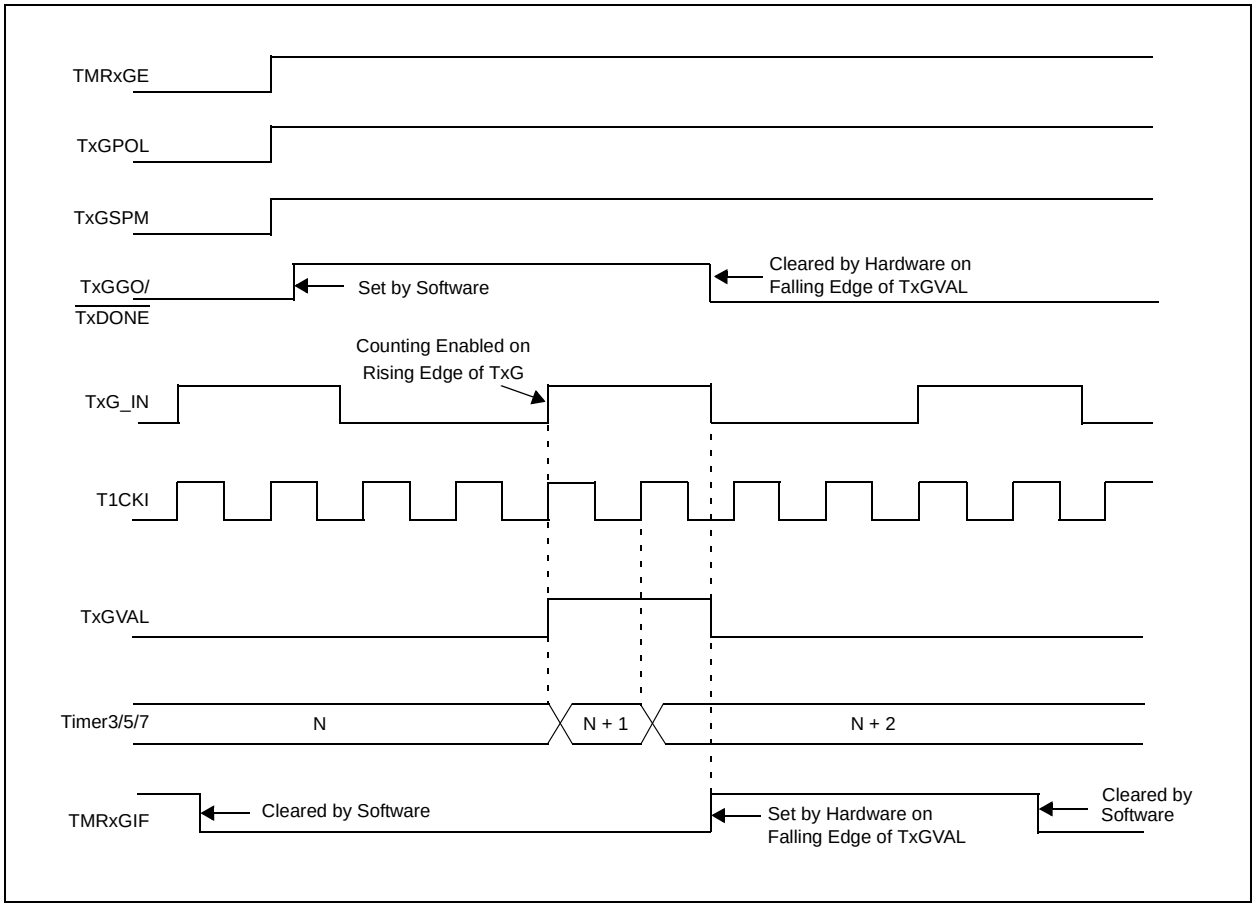
When Timer3/5/7 Gate Single Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer3/5/7 Gate Single Pulse mode is first enabled by setting the TxGSPM bit (TxGCON<4>). Next, the TxGGO/TxDONE bit (TxGCON<3>) must be set.

The Timer3/5/7 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the TxGGO/TxDONE bit will automatically be cleared. No other gate events will be allowed to increment Timer3/5/7 until the TxGGO/TxDONE bit is once again set in software.

Clearing the TxGSPM bit also will clear the TxGGO/TxDONE bit. (For timing details, see Figure 15-4.)

Simultaneously enabling the Toggle mode and the Single Pulse mode will permit both sections to work together. This allows the cycle times on the Timer3/5/7 gate source to be measured. (For timing details, see Figure 15-5.)

FIGURE 15-4: TIMER3/5/7 GATE SINGLE PULSE MODE



REGISTER 17-4: ALRMCFG: AL ARM CONFIGURATION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 7 ALRMEN: Alarm Enable bit

1 = Alarm is enabled (cleared automatically after an alarm event whenever ALRMPTR<1:0> = 00 and CHIME = 0)
0 = Alarm is disabled

bit 6 CHIME: Chime Enable bit

1 = Chime is enabled; ALRMPTR<1:0> bits are allowed to roll over from 00h to FFh
0 = Chime is disabled; ALRMPTR<1:0> bits stop once they reach 00h

bit 5-2 AMASK<3:0>: Alarm Mask Configuration bits

0000 = Every half second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29th, once every four years)
101x = Reserved Do not use
11xx = Reserved Do not use

bit 1-0 ALRMPTR<1:0>: Alarm Value Register Window Pointer bits

Points to the corresponding Alarm Value registers when reading the ALRMVALH and ALRMVALL registers. The ALRMPTR<1:0> value decrements on every read or write of ALRMVALH until it reaches 00 .

ALRMVALH:
00 = ALRMMIN
01 = ALRMWD
10 = ALRMMNTH
11 = Unimplemented

ALRMVALL:
00 = ALRMSEC
01 = ALRMHR
10 = ALRMDAY
11 = Unimplemented

18.1.2 OPEN-DRAIN OUTPUT OPTION

When operating in Output mode (the Compare or PWM modes), the drivers for the CCPx pins can be optionally configured as open-drain outputs. This feature allows the voltage level on the pin to be pulled to a higher level through an external pull-up resistor and allows the output to communicate with external circuits without the need for additional level shifters.

The open-drain output option is controlled by the CCPxOD bits (ODCON2<7:2>). Setting the appropriate bit configures the pin for the corresponding module for open-drain operation.

18.1.3 PIN ASSIGNMENT FOR CCP6, CCP7, CCP8 AND CCP9

The pin assignment for CCP6/7/8/9 (Capture input, Compare and PWM output) can change, based on the device configuration.

The ECCPMX Configuration bit (CONFIG3H<1>) determines the pin to which CCP6/7/8/9 is multiplexed. The pin assignments for these CCP modules are given in Table 18-4.

TABLE 18-4: CCP PIN ASSIGNMENT

ECCPMX Value	Pin Mapped To			
	CCP6	CCP7	CCP8	CC9
1 (Default)	RE6	RE5	RE4	RE3
0	RH7	RH6	RH5	RH4

18.2 Capture Mode

In Capture mode, the CCPR4H:CCPR4L register pair captures the 16-bit value of the TMR1 or TMR3 register when an event occurs on the CCP4 pins. An event is defined as one of the following:

Every falling edge
Every rising edge
Every 4th rising edge
Every 16th rising edge

The event is selected by the mode select bits, CCP4M<3:0> (CCP4CON<3:0>). When a capture is made, the interrupt request flag bit, CCP4IF (PIR4<1>), is set. (It must be cleared in software.) If another capture occurs before the value in CCPR4 is read, the old captured value is overwritten by the new captured value.

Figure 18-1 shows the Capture mode block diagram.

18.2.1 CCP PIN CONFIGURATION

In Capture mode, the appropriate CCPx pin should be configured as an input by setting the corresponding TRIS direction bit.

Note:	If RC1 or RE7 is configured as a CCP4 output, a write to the PORT causes a capture condition.

18.2.2 TIMER1/3/5/7 MODE SELECTION

For the available timers (1/3/5/7) to be used for the capture feature, the used timers must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work.

The timer to be used with each CCP module is selected in the CCPTMRSx registers. (See Section 18.1.1 CCP Modules and Timer Resources .)

Details of the timer assignments for the CCP modules are given in Table 18-2 and Table 18-3.

19.0 ENHANCED CAPTURE/COMPARE/PWM (ECCP) MODULE

PIC18F87K90 family devices have three Enhanced Capture/Compare/PWM (ECCP) modules: ECCP1, ECCP2 and ECCP3. These modules contain a 16-bit register, which can operate as a 16-bit Capture register, a 16-bit Compare register or a PWM Master/Slave Duty Cycle register. These ECCP modules are upward compatible with CCP

Note:	Throughout this section, generic references are used for register and bit names that are the same, except for an x variable that indicates the item s association with the ECCP1, ECCP2 or ECCP3 module. For example, the control register is named CCPxCON and refers to CCP1CON, CCP2CON and CCP3CON.

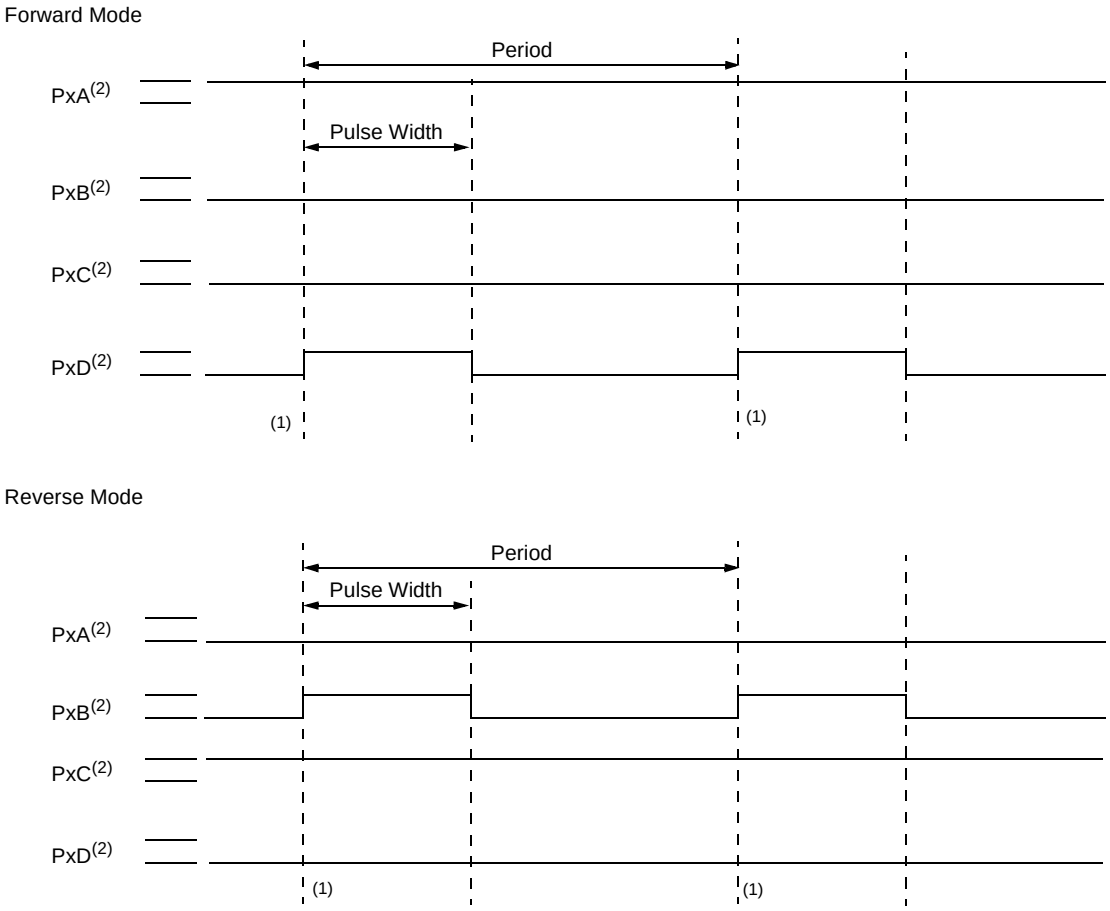
ECCP1, ECCP2 and ECCP3 are implemented as standard CCP modules with Enhanced PWM capabilities. These include:

- Provision for two or four output channels
- Output Steering modes
- Programmable polarity
- Programmable dead-band control
- Automatic shutdown and restart

The enhanced features are discussed in detail in Section 19.4 PWM (Enhanced Mode) .

The ECCP1, ECCP2 and ECCP3 modules use the control registers, CCP1CON, CCP2CON and CCP3CON. The control registers, CCP4CON through CCP10CON, are for the CCP4 through CCP10 modules.

FIGURE 19-9: EXAMPLE OF FULL-BRIDGE PWM OUTPUT



Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: The output signal is shown as active-high.

REGISTER 28-3: CONFIG2L: CONFIGURATION REGISTER 2 LOW (BYTE ADDRESS 300002h)

U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
	BORPWR1 (1)	BORPWR0(1)	BORV1(1)	BORV0(1)	BOREN1(2)	BOREN0(2)	$\overline{\text{PWRTEN}}$(2)
bit 7							bit 0

Legend:	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 7 Unimplemented: Read as 0

bit 6-5 BORPWR<1:0>: BORMV Power Level bits(1)

11 = ZPBORVMV instead of BORMV is selected
10 = BORMV is set to high-power level
01 = BORMV is set to medium-power level
00 = BORMV is set to low-power level

bit 4-3 BORV<1:0>: Brown-out Reset Voltage bits(1)

11 = VBORMV is set to 1.8V
10 = VBORMV is set to 2.0V
01 = VBORMV is set to 2.7V
00 = VBORMV is set to 3.0V

bit 2-1 BOREN<1:0>: Brown-out Reset Enable bits(2)

11 = Brown-out Reset is enabled in hardware only (SBOREN is disabled)
10 = Brown-out Reset is enabled in hardware only and disabled in Sleep mode (SBOREN is disabled)
01 = Brown-out Reset is enabled and controlled by software (SBOREN is enabled)
00 = Brown-out Reset is disabled in hardware and software

bit 0 $\overline{\text{PWRTEN}}$: Power-up Timer Enable bit(2)

1 = PWRT is disabled
0 = PWRT is enabled

Note 1: For the specifications, see Section 31.1 DC Characteristics: Supply Voltage PIC18F87K90 Family (Industrial/Extended) .

2: The Power-up Timer is decoupled from Brown-out Reset, allowing these features to be independently controlled.

TABLE 29-2: PIC18F87K90 FAMILY INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
BYTE-ORIENTED OPERATIONS									
ADDWF	f, d, a	Add WREG and f	1	0010	01da	ffff	ffff	C, DC, Z, OV, N	1, 2
ADDWFC	f, d, a	Add WREG and Carry bit to f	1	0010	00da	ffff	ffff	C, DC, Z, OV, N	1, 2
ANDWF	f, d, a	AND WREG with f	1	0001	01da	ffff	ffff	Z, N	1, 2
CLRF	f, a	Clear f	1	0110	101a	ffff	ffff	Z	2
COMF	f, d, a	Complement f	1	0001	11da	ffff	ffff	Z, N	1, 2
CPFSEQ	f, a	Compare f with WREG, Skip =	1 (2 or 3)	0110	001a	ffff	ffff	None	4
CPFSGT	f, a	Compare f with WREG, Skip >	1 (2 or 3)	0110	010a	ffff	ffff	None	4
CPFSLT	f, a	Compare f with WREG, Skip <	1 (2 or 3)	0110	000a	ffff	ffff	None	1, 2
DECF	f, d, a	Decrement f	1	0000	01da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
DECFSZ	f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010	11da	ffff	ffff	None	1, 2, 3, 4
DCFSNZ	f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100	11da	ffff	ffff	None	1, 2
INCF	f, d, a	Increment f	1	0010	10da	ffff	ffff	C, DC, Z, OV, N	1, 2, 3, 4
INCFSZ	f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011	11da	ffff	ffff	None	4
INFSNZ	f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100	10da	ffff	ffff	None	1, 2
IORWF	f, d, a	Inclusive OR WREG with f	1	0001	00da	ffff	ffff	Z, N	1, 2
MOVF	f, d, a	Move f	1	0101	00da	ffff	ffff	Z, N	1
MOVFF	f_s, f_d	Move f_s (source) to 1st word	2	1100	ffff	ffff	ffff	None	
		f_d (destination) 2nd word		1111	ffff	ffff	ffff		
MOVWF	f, a	Move WREG to f	1	0110	111a	ffff	ffff	None	
MULWF	f, a	Multiply WREG with f	1	0000	001a	ffff	ffff	None	1, 2
NEGF	f, a	Negate f	1	0110	110a	ffff	ffff	C, DC, Z, OV, N	
RLCF	f, d, a	Rotate Left f through Carry	1	0011	01da	ffff	ffff	C, Z, N	1, 2
RLNCF	f, d, a	Rotate Left f (No Carry)	1	0100	01da	ffff	ffff	Z, N	
RRCF	f, d, a	Rotate Right f through Carry	1	0011	00da	ffff	ffff	C, Z, N	
RRNCF	f, d, a	Rotate Right f (No Carry)	1	0100	00da	ffff	ffff	Z, N	
SETF	f, a	Set f	1	0110	100a	ffff	ffff	None	1, 2
SUBFWB	f, d, a	Subtract f from WREG with Borrow	1	0101	01da	ffff	ffff	C, DC, Z, OV, N	
SUBWF	f, d, a	Subtract WREG from f	1	0101	11da	ffff	ffff	C, DC, Z, OV, N	1, 2
SUBWFB	f, d, a	Subtract WREG from f with Borrow	1	0101	10da	ffff	ffff	C, DC, Z, OV, N	
SWAPF	f, d, a	Swap Nibbles in f	1	0011	10da	ffff	ffff	None	4
TSTFSZ	f, a	Test f, Skip if 0	1 (2 or 3)	0110	011a	ffff	ffff	None	1, 2
XORWF	f, d, a	Exclusive OR WREG with f	1	0001	10da	ffff	ffff	Z, N	

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is 1 for a pin configured as input and is driven low by an external device, the data will be written back with a 0 .

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

TABLE 29-2: PIC18F87K90 FAMILY INSTRUCTION SET (CONTINUED)

Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
				MSb			LSb		
BIT-ORIENTED OPERATIONS									
BCF	f, b, a	Bit Clear f	1	1001	bbba	ffff	ffff	None	1, 2
BSF	f, b, a	Bit Set f	1	1000	bbba	ffff	ffff	None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011	bbba	ffff	ffff	None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010	bbba	ffff	ffff	None	3, 4
BTG	f, b, a	Bit Toggle f	1	0111	bbba	ffff	ffff	None	1, 2
CONTROL OPERATIONS									
BC	n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	
BN	n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC	n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ	n	Branch if Not Zero	1 (2)	1110	0001	nnnn	nnnn	None	
BOV	n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA	n	Branch Unconditionally	2	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL	n, s	Call Subroutine 1st word	2	1110	110s	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
CLRWDT		Clear Watchdog Timer	1	0000	0000	0000	0100	$\overline{TO}$, $\overline{PD}$	
DAW		Decimal Adjust WREG	1	0000	0000	0000	0111	C	
GOTO	n	Go to Address 1st word	2	1110	1111	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
NOP		No Operation	1	0000	0000	0000	0000	None	
NOP		No Operation	1	1111	xxxx	xxxx	xxxx	None	4
POP		Pop Top of Return Stack (TOS)	1	0000	0000	0000	0110	None	
PUSH		Push Top of Return Stack (TOS)	1	0000	0000	0000	0101	None	
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET		Software Device Reset	1	0000	0000	1111	1111	All	
RETFIE	s	Return from Interrupt Enable	2	0000	0000	0001	000s	GIE/GIEH, PEIE/GIEL	
RETLW	k	Return with Literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN	s	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP		Go into Standby mode	1	0000	0000	0000	0011	$\overline{TO}$, $\overline{PD}$	

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is 1 for a pin configured as input and is driven low by an external device, the data will be written back with a 0 .

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.

3: If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

ADDWFC ADD W and Carry bit to f

Syntax: ADDWFC f {,d {,a}}

Operands: 0 df d255
d • [0,1]
a • [0,1]

Operation: (W) + (f) + (C) o dest

Status Affected: N,OV, C, DC, Z

Encoding:

0010	00da	ffff	ffff

Description: Add W, the Carry flag and data memory location f . If d is 0 , the result is placed in W. If d is 1 , the result is placed in data memory location f .

If a is 0 , the Access Bank is selected. If a is 1 , the BSR is used to select the GPR bank.

If a is 0 and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f d95 (5Fh). See Section 29.2.3 Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register f	Process Data	Write to destination

Example: ADDWFC REG, 0, 1

Before Instruction
Carry bit = 1
REG = 02h
W = 4Dh
After Instruction
Carry bit = 0
REG = 02h
W = 50h

ANDLW AND Literal with W

Syntax: ANDLW k

Operands: 0 dk d255

Operation: (W) .AND. k o W

Status Affected: N, Z

Encoding:

0000	1011	kkkk	kkkk

Description: The contents of W are ANDed with the 8-bit literal k . The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal k	Process Data	Write to W

Example: ANDLW 05Fh

Before Instruction
W = A3h
After Instruction
W = 03h

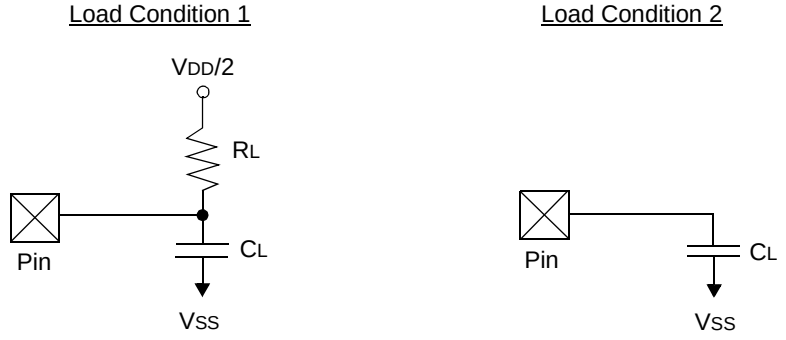
31.5.2 TIMING CONDITIONS

The temperature and voltages specified in Table 31-5 apply to all timing specifications unless otherwise noted. Figure 31-3 specifies the load conditions for the timing specifications.

TABLE 31-5: TEMPERATURE AND VOLTAGE SPECIFICATIONS AC

AC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40℃ dTA d+85℃ for industrial -40℃ dTA d+125℃ for extended Operating voltage VDD range as described in Section 31.1 and Section 31.3 .

FIGURE 31-3: LOAD CONDITIONS FOR DE VICE TIMING SPECIFICATIONS



RL = 464 :

CL = 50 pF for all pins except OSC2/CLKO/RA6 and including D and E outputs as ports

CL = 15 pF for OSC2/CLKO/RA6