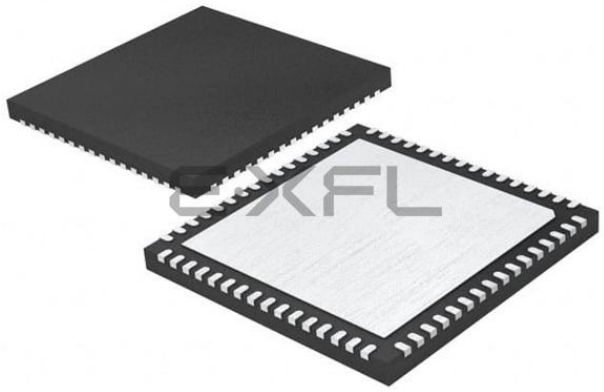

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f65k90t-i-mr

TABLE 1-4: PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RH7/SEG43/CCP6/P1B/ AN15	19			
RH7		I/O	ST	Digital I/O.
SEG43		O	Analog	SEG43 output for LCD.
CCP6(4)		I/O	ST	Capture 6 input/Compare 6 output/PWM6 output.
P1B		O	—	ECCP1 PWM Output B.
AN15		I	Analog	Analog Input 15.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to V_{DD}); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

3.0 OSCILLATOR CONFIGURATIONS

3.1 Oscillator Types

The PIC18F87K90 family of devices can be operated in the following oscillator modes:

- EC External Clock, RA6 available
- ECIO External Clock, Clock Out RA6 (FOSC/4 on RA6)
- HS High-Speed Crystal/Resonator
- XT Crystal/Resonator
- LP Low-Power Crystal
- RC External Resistor/Capacitor, RA6 available
- RCIO External Resistor/Capacitor, Clock Out RA6 (FOSC/4 on RA6)
- INTIO2 Internal Oscillator with I/O on RA6 and RA7
- INTIO1 Internal Oscillator with FOSC/4 Output on RA6 and I/O on RA7

There is also an option for running the 4xPLL on any of the clock sources in the input frequency range of 4 to 16 MHz.

The PLL is enabled by setting the PLLCFG bit (CONFIG1H<4>) or the PLLEN bit (OSCTUNE<6>).

For the EC and HS mode, the PLLEN (software) or PLLCFG (CONFIG) bit can be used to enable the PLL.

For the INTIOx modes (HF-INTOSC):

- Only the PLLEN can enable the PLL (PLLCFG is ignored).
- When the oscillator is configured for the internal oscillator (OSC<3:0> = 100x), the PLL can be enabled only when the HF-INTOSC frequency is 8 or 16 MHz.

When the RA6 and RA7 pins are not used for an oscillator function or CLKOUT function, they are available as general purpose I/Os.

To optimize power consumption when using EC/HS/XT/LP/RC as the primary oscillator, the frequency input range can be configured to yield an optimized power bias:

- Low-Power Bias – External frequency less than 160 kHz
- Medium Power Bias – External frequency between 160 kHz and 16 MHz
- High-Power Bias – External frequency greater than 16 MHz

All of these modes are selected by the user by programming the OSC<3:0> Configuration bits (CONFIG1H<3:0>). In addition, PIC18F87K90 family devices can switch between different clock sources, either under software control or under certain conditions, automatically. This allows for additional power savings by managing device clock speed in real time without resetting the application. The clock sources for the PIC18F87K90 family of devices are shown in Figure 3-1.

For the HS and EC mode, there are additional power modes of operation – depending on the frequency of operation.

HS1 is the Medium Power mode with a frequency range of 4 MHz to 16 MHz. HS2 is the High-Power mode where the oscillator frequency can go from 16 MHz to 25 MHz. HS1 and HS2 are achieved by setting the CONFIG1H<3:0> correctly. (For details, see Register 28-2 on page 428.)

EC mode has these modes of operation:

- EC1 – For low power with a frequency range up to 160 kHz
- EC2 – Medium power with a frequency range of 160 kHz to 16 MHz
- EC3 – High power with a frequency range of 16 MHz to 64 MHz

EC1, EC2 and EC3 are achieved by setting the CONFIG1H<3:0> correctly. (For details, see Register 28-2 on page 428.)

Table 3-1 shows the HS and EC modes' frequency range and OSC<3:0> settings.

If the IRCF bits and the INTSRC bit are all clear, the INTOSC output (HF-INTOSC/MF-INTOSC) is not enabled, and the HFIOFS and MFIOFS bits will remain clear. There will be no indication of the current clock source. The LF-INTOSC source is providing the device clocks.

If the IRCF bits are changed from all clear (thus, enabling the INTOSC output) or if INTSRC or MFIOSEL is set, the HFIOFS or MFIOFS bit is set after the INTOSC output becomes stable. For details, see Table 4-3.

TABLE 4-3: INTERNAL OSCILLATOR FREQUENCY STABILITY BITS

IRCF<2:0>	INTSRC	MFIOSEL	Status of MFIOFS or HFIOFS when INTOSC is Stable
000	0	x	MFIOFS = 0, HFIOFS = 0 and clock source is LF-INTOSC
000	1	0	MFIOFS = 0, HFIOFS = 1 and clock source is HF-INTOSC
000	1	1	MFIOFS = 1, HFIOFS = 0 and clock source is MF-INTOSC
Non-Zero	x	0	MFIOFS = 0, HFIOFS = 1 and clock source is HF-INTOSC
Non-Zero	x	1	MFIOFS = 1, HFIOFS = 0 and clock source is MF-INTOSC

Clocks to the device continue while the INTOSC source stabilizes after an interval of TIOBST (Parameter 39, Table 31-10).

If the IRCF bits were previously at a non-zero value, or if INTSRC was set before setting SCS1, and the INTOSC source was already stable, the HFIOFS or MFIOFS bit will remain set.

On transitions from RC_RUN mode to PRI_RUN mode, the device continues to be clocked from the INTOSC multiplexer while the primary clock is started. When the primary clock becomes ready, a clock switch to the primary clock occurs (see Figure 4-4). When the clock switch is complete, the HFIOFS or MFIOFS bit is cleared, the OSTS bit is set and the primary clock is providing the device clock. The IDLEN and SCS bits are not affected by the switch. The LF-INTOSC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

TABLE 4-4: EXIT DELAY ON WAKE-UP BY RESET FROM SLEEP MODE OR ANY IDLE MODE (BY CLOCK SOURCES)

Power-Managed Mode	Clock Source[5]	Exit Delay	Clock Ready Status Bits
PRI_IDLE mode	LP, XT, HS	T_{CSD}[1]	OSTS
	HSPLL		
	EC, RC		
	HF-INTOSC[2]		HFIOFS
	MF-INTOSC[2]		MFIOFS
	LF-INTOSC		None
SEC_IDLE mode	SOSC	T_{CSD}[1]	SOSCRUN
RC_IDLE mode	HF-INTOSC[2]	T_{CSD}[1]	HFIOFS
	MF-INTOSC[2]		MFIOFS
	LF-INTOSC		None
Sleep mode	LP, XT, HS	T_{OST}[3]	OSTS
	HSPLL	$T_{OST} + t_{rc}$[3]	
	EC, RC	T_{CSD}[1]	
	HF-INTOSC[2]	T_{IOBST}[4]	HFIOFS
	MF-INTOSC[2]		MFIOFS
	LF-INTOSC		None

Note 1: T_{CSD} (Parameter 38, Table 31-10) is a required delay when waking from Sleep and all Idle modes, and runs concurrently with any other required delays (see **Section 4.4 “Idle Modes”**).

2: Includes postscaler derived frequencies. On Reset, INTOSC defaults to HF-INTOSC at 8 MHz.

3: T_{OST} is the Oscillator Start-up Timer (Parameter 32, Table 31-10). T_{RC} is the PLL Lock-out Timer (Parameter F12, Table 31-7); it is also designated as T_{PLL}.

4: Execution continues during T_{IOBST} (Parameter 39, Table 31-10), the INTOSC stabilization period.

5: The clock source is dependent upon the settings of the SCS (OSCCON<1:0>), IRCF (OSCCON<6:4>) and FOSC (CONFIG1H<3:0>) bits.

5.2 Master Clear ($\overline{MCLR}$)

The $\overline{MCLR}$ pin provides a method for triggering a hard external Reset of the device. A Reset is generated by holding the pin low. PIC18 extended microcontroller devices have a noise filter in the $\overline{MCLR}$ Reset path which detects and ignores small pulses.

The $\overline{MCLR}$ pin is not driven low by any internal Resets, including the WDT.

5.3 Power-on Reset (POR)

A Power-on Reset condition is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the $\overline{MCLR}$ pin through a resistor (1 kΩ to 10 kΩ) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (Parameter D004). For a slow rise time, see Figure 5-2.

When the device starts normal operation (exiting the Reset condition), device operating parameters (such as voltage, frequency and temperature) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

Power-on Reset events are captured by the $\overline{POR}$ bit (RCON<1>). The state of the bit is set to '0' whenever a Power-on Reset occurs and does not change for any other Reset event. $\overline{POR}$ is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any Power-on Reset.

5.4 Brown-out Reset (BOR)

The PIC18F87K90 family has four BOR modes:

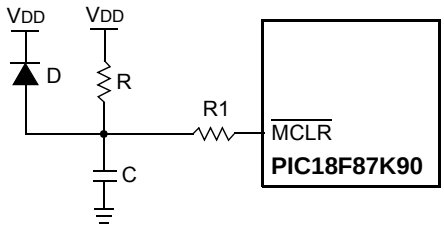
- High-Power BOR
- Medium Power BOR
- Low-Power BOR
- Zero-Power BOR

Each power mode is selected by the BORPWR<1:0> bits setting (CONFIG2L<6:5>). For low, medium and high-power BOR, the module monitors the VDD depending on the BORV<1:0> setting (CONFIG1L<3:2>). A BOR event re-arms the Power-on Reset. It also causes a Reset depending on which of the trip levels has been set: 1.8V, 2V, 2.7V or 3V. The typical (ΔIBOR) trip level for the Low and Medium Power BOR will be 0.75 μA and 3 μA.

In Zero-Power BOR (ZPBORMV), the module monitors the VDD voltage and re-arms the POR at about 2V. ZPBORMV does not cause a Reset, but re-arms the POR.

The BOR accuracy varies with its power level. The lower the power setting, the less accurate the BOR trip levels are. So, the high-power BOR has the highest accuracy and the low-power BOR has the lowest accuracy. The trip levels (BVDD, Parameter D005), current consumption (**Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F87K90 Family (Industrial/Extended)"**) and time required below BVDD (TBOR, Parameter 35) can all be found in **Section 31.0 "Electrical Characteristics"**

FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode, D, helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.

3: R1 ≥ 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor, C, in the event of $\overline{MCLR}$/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

5.4.1 DETECTING BOR

The $\overline{BOR}$ bit always resets to '0' on any Brown-out Reset or Power-on Reset event. This makes it difficult to determine if a Brown-out Reset event has occurred just by reading the state of $\overline{BOR}$ alone. A more reliable method is to simultaneously check the state of both $\overline{POR}$ and $\overline{BOR}$. This assumes that the $\overline{POR}$ bit is reset to '1' in software immediately after any Power-on Reset event. If $\overline{BOR}$ is '0' while $\overline{POR}$ is '1', it can be reliably assumed that a Brown-out Reset event has occurred.

LP-BOR cannot be detected with the $\overline{BOR}$ bit in the RCON register. LP-BOR can rearm the $\overline{POR}$ and can cause a Power-on Reset.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets, WDT Reset, RESET Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
CCPR10L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP10CON	PIC18F6XK90	PIC18F8XK90	--00 0000	--00 0000	--uu uuuu
TMR7H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR7L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
T7CON	PIC18F6XK90	PIC18F8XK90	0000 0000	uuuu uuuu	uuuu -uuu
T7GCON	PIC18F6XK90	PIC18F8XK90	0000 0x00	0000 0x00	uuuu uuuu
TMR6	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PR6	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
T6CON	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu
TMR8	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PR8	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
T8CON	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu
TMR10	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PR10	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
T10CON	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu
TMR12	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PR12	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
T12CON	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu
CM2CON	PIC18F6XK90	PIC18F8XK90	0001 1111	0001 1111	uuuu uuuu
CM3CON	PIC18F6XK90	PIC18F8XK90	0001 1111	0001 1111	uuuu uuuu
CCPTMRS0	PIC18F6XK90	PIC18F8XK90	0000 0000	uuuu uuuu	uuuu uuuu
CCPTMRS1	PIC18F6XK90	PIC18F8XK90	00-0 -000	uu-u -uuu	uu-u -uuu
CCPTMRS2	PIC18F6XK90	PIC18F8XK90	---0 -000	---u -uuu	---u -uuu
REFOCON	PIC18F6XK90	PIC18F8XK90	0-00 0000	u-uu uuuu	u-uu uuuu
ODCON1	PIC18F6XK90	PIC18F8XK90	000- ---0	uuu- ---u	uuu- ---u
ODCON2	PIC18F6XK90	PIC18F8XK90	0000 0000	uuuu uuuu	uuuu uuuu
ODCON3	PIC18F6XK90	PIC18F8XK90	00-- ---0	uu-- ---u	uu-- ---u
ANCON0	PIC18F6XK90	PIC18F8XK90	1111 1111	uuuu uuuu	uuuu uuuu
ANCON1	PIC18F6XK90	PIC18F8XK90	1111 1111	uuuu uuuu	uuuu uuuu
ANCON2	PIC18F6XK90	PIC18F8XK90	1111 1111	uuuu uuuu	uuuu uuuu
RCSTA2	PIC18F6XK90	PIC18F8XK90	0000 000x	0000 000x	uuuu uuuu
TXSTA2	PIC18F6XK90	PIC18F8XK90	0000 0010	0000 0010	uuuu uuuu
BAUDCON2	PIC18F6XK90	PIC18F8XK90	0100 0-00	0100 0-00	uuuu u-uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for the Reset value for a specific condition.

8.3 Reading the Data EEPROM Memory

To read a data memory location, the user must write the address to the EEADRH:EEADR register pair, clear the EEPGD control bit (EECON1<7>) and then set control bit, RD (EECON1<0>). After one cycle, the data is available in the EEDATA register; therefore, it can be read after one NOP instruction. EEDATA will hold this value until another read operation, or until it is written to by the user (during a write operation). The basic process is shown in Example 8-1.

8.4 Writing to the Data EEPROM Memory

To write an EEPROM data location, the address must first be written to the EEADRH:EEADR register pair and the data written to the EEDATA register. The sequence in Example 8-2 must be followed to initiate the write cycle.

The write will not begin if this sequence is not exactly followed (write 0x55 to EECON2, write 0xAA to EECON2, then set WR bit) for each byte. It is strongly recommended that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable writes. This mechanism prevents accidental writes to data EEPROM due to unexpected code execution (i.e., runaway programs). The WREN bit should be kept clear at all times, except when updating the EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, EECON1, EEADRH:EEADR and EEDATA cannot be modified. The WR bit will be inhibited from being set unless the WREN bit is set. The WREN bit must be set on a previous instruction. Both WR and WREN cannot be set with the same instruction.

At the completion of the write cycle, the WR bit is cleared in hardware and the EEPROM Interrupt Flag bit (EEIF) is set. The user may either enable this interrupt, or poll this bit. EEIF must be cleared by software.

8.5 Write Verify

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit.

Note:	Self-write execution to Flash and EEPROM memory cannot be done while running in LP Oscillator mode (Low-Power mode). Therefore, executing a self-write will put the device into High-Power mode.

EXAMPLE 8-1: DATA EEPROM READ

```
        MOVLW   DATA_EE_ADDRH      ;
        MOVWF   EEADRH             ; Upper bits of Data Memory Address to read
        MOVLW   DATA_EE_ADDR       ;
        MOVWF   EEADR              ; Lower bits of Data Memory Address to read
        BCF     EECON1, EEPGD      ; Point to DATA memory
        BCF     EECON1, CFGS       ; Access EEPROM
        BSF     EECON1, RD         ; EEPROM Read
        NOP
        MOVF    EEDATA, W          ; W = EEDATA
```

EXAMPLE 8-2: DATA EEPROM WRITE

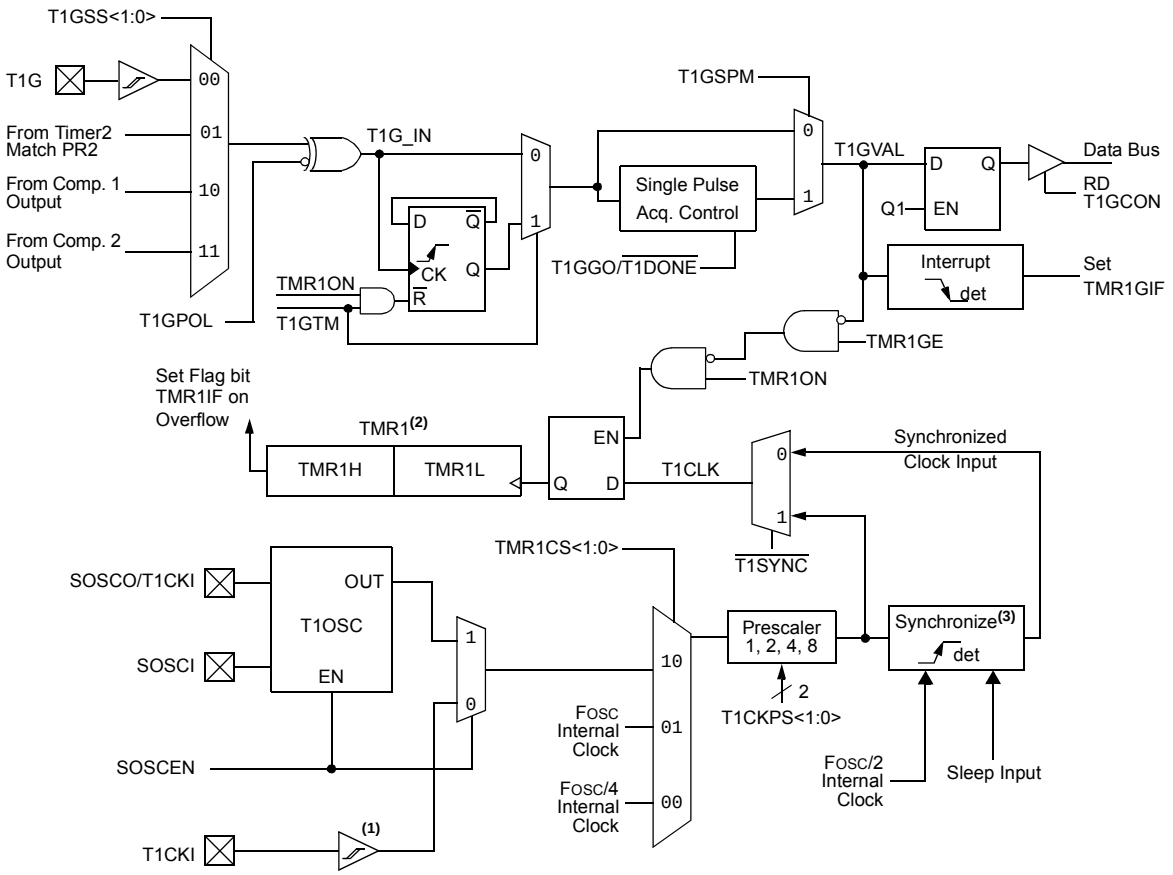
```
                MOVLW   DATA_EE_ADDRH      ;
                MOVWF   EEADRH             ; Upper bits of Data Memory Address to write
                MOVLW   DATA_EE_ADDR       ;
                MOVWF   EEADR              ; Lower bits of Data Memory Address to write
                MOVLW   DATA_EE_DATA       ;
                MOVWF   EEDATA             ; Data Memory Value to write
                BCF     EECON1, EEPGD      ; Point to DATA memory
                BCF     EECON1, CFGS       ; Access EEPROM
                BSF     EECON1, WREN       ; Enable writes

                BCF     INTCON, GIE        ; Disable Interrupts
                MOVLW   0x55               ;
  Required      MOVWF   EECON2             ; Write 55h
  Sequence      MOVLW   0xAA               ;
                MOVWF   EECON2             ; Write 0AAh
                BTFSC   EECON1, WR         ; Wait for write to complete
                GOTO    $-2
                BSF     INTCON, GIE        ; Enable Interrupts

                                           ; User code execution
                BCF     EECON1, WREN       ; Disable writes on write complete (EEIF set)
```

TABLE 11-1: PORTA FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0/ULPWU	RA0	0	O	DIG	LATA<0> data output; not affected by analog input.
		1	I	TTL	PORTA<0> data input; disabled when analog input is enabled.
	AN0	1	I	ANA	A/D Input Channel 0. Default input configuration on POR; does not affect digital output.
	ULPWU	1	I	ANA	Ultra Low-Power Wake-up (ULPWU) input.
RA1/AN1/SEG18	RA1	0	O	DIG	LATA<1> data output; not affected by analog input.
		1	I	TTL	PORTA<1> data input; disabled when analog input is enabled.
	AN1	1	I	ANA	A/D Input Channel 1. Default input configuration on POR; does not affect digital output.
	SEG18	1	O	ANA	LCD Segment 18 output; disables all other pin functions.
RA2/AN2/VREF-	RA2	0	O	DIG	LATA<2> data output; not affected by analog input.
		1	I	TTL	PORTA<2> data input; disabled when analog functions are enabled.
	AN2	1	I	ANA	A/D Input Channel 2. Default input configuration on POR.
	VREF-	1	I	ANA	A/D and comparator low reference voltage input.
RA3/AN3/VREF+	RA3	0	O	DIG	LATA<3> data output; not affected by analog input.
		1	I	TTL	PORTA<3> data input; disabled when analog input is enabled.
	AN3	1	I	ANA	A/D Input Channel 3. Default input configuration on POR.
	VREF+	1	I	ANA	A/D and comparator high reference voltage input.
RA4/T0CKI/ SEG14	RA4	0	O	DIG	LATA<4> data output.
		1	I	ST	PORTA<4> data input. Default configuration on POR.
	T0CKI	x	I	ST	Timer0 clock input.
	SEG14	1	O	ANA	LCD Segment 14 output; disables all other pin functions.
RA5/AN4/SEG15/ T1CKI/T3G/ HLVDIN	RA5	0	O	DIG	LATA<5> data output; not affected by analog input.
		1	I	TTL	PORTA<5> data input; disabled when analog input is enabled.
	AN4	1	I	ANA	A/D Input Channel 4. Default configuration on POR.
	SEG15	1	O	ANA	LCD Segment 15 output; disables all other pin functions.
	T1CKI	x	I	ST	Timer1 clock input.
	T3G	x	I	ST	Timer3 external clock gate input.
	HLVDIN	1	I	ANA	High/Low-Voltage Detect (HLVD) external trip point input.
OSC2/CLKO/RA6	OSC2	x	O	ANA	Main oscillator feedback output connection (HS, XT and LP modes).
	CLKO	x	O	DIG	System cycle clock output (FOSC/4, EC and INTOSC modes).
	RA6	0	O	DIG	LATA<6> data output; disabled when OSC2 Configuration bit is set.
		1	I	TTL	PORTA<6> data input; disabled when OSC2 Configuration bit is set.
OSC1/CLKI/RA7	OSC1	x	I	ANA	Main oscillator input connection (HS, XT and LP modes).
	CLKI	x	I	ANA	Main external clock source input (EC modes).
	RA7	0	O	DIG	LATA<7> data output; disabled when OSC2 Configuration bit is set.
		1	I	TTL	PORTA<7> data input; disabled when OSC2 Configuration bit is set.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



Note 1: The ST buffer is a high-speed type when using T1CKI.
2: Timer1 register increments on the rising edge.
3: Synchronization does not operate while in Sleep.

14.0 TIMER2 MODULE

The Timer2 module incorporates the following features:

- 8-bit Timer and Period registers (TMR2 and PR2, respectively)
- Both registers are readable and writable
- Software programmable prescaler (1:1, 1:4 and 1:16)
- Software programmable postscaler (1:1 through 1:16)
- Interrupt on TMR2 to PR2 match
- Optional use as the shift clock for the MSSP modules

This module is controlled through the T2CON register (Register 14-1) that enables or disables the timer, and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

A simplified block diagram of the module is shown in Figure 14-1.

14.1 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock (FOSC/4). A 4-bit counter/prescaler on the clock input gives the prescale options of direct input, divide-by-4 or divide-by-16. These are selected by the prescaler control bits, T2CKPS<1:0> (T2CON<1:0>).

The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler. (See **Section 14.2 "Timer2 Interrupt"**.)

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR2 register
- A write to the T2CON register
- Any device Reset (Power-on Reset (POR), $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset (WDTR) or Brown-out Reset [BOR])

TMR2 is not cleared when T2CON is written.

Note:	The CCP and ECCP modules use Timers, 1 through 8, for some modes. The assignment of a particular timer to a CCP/ECCP module is determined by the Timer to CCP enable bits in the CCPTMRSx registers. For more details, see Register 18-2, Register 18-3 and Register 19-2.

REGISTER 14-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **T2OUTPS<3:0>:** Timer2 Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2 **TMR2ON:** Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits
00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

FIGURE 17-5: ALARM MASK SETTINGS

Alarm Mask Setting AMASK<3:0>	Day of the Week	Month	Day	Hours	Minutes	Seconds
0000 – Every half second 0001 – Every second						
0010 – Every 10 seconds						s
0011 – Every minute						s s
0100 – Every 10 minutes					m	s s
0101 – Every hour					m m	s s
0110 – Every day				h h	m m	s s
0111 – Every week	d			h h	m m	s s
1000 – Every month			d d	h h	m m	s s
1001 – Every year(1)		m m	d d	h h	m m	s s

Note 1: Annually, except when configured for February 29.

When ALRMCFG = 00 and the CHIME bit = 0 (ALRMCFG<6>), the repeat function is disabled and only a single alarm will occur. The alarm can be repeated up to 255 times by loading the ALRMRPT register with FFh.

After each alarm is issued, the ALRMRPT register is decremented by one. Once the register has reached '00', the alarm will be issued one last time.

After the alarm is issued a last time, the ALRMEN bit is cleared automatically and the alarm is turned off. Indefinite repetition of the alarm can occur if the CHIME bit = 1.

When CHIME = 1, the alarm is not disabled when the ALRMRPT register reaches '00', but it rolls over to FF and continues counting indefinitely.

17.3.2 ALARM INTERRUPT

At every alarm event, an interrupt is generated. Additionally, an alarm pulse output is provided that operates at half the frequency of the alarm.

The alarm pulse output is completely synchronous with the RTCC clock and can be used as a trigger clock to other peripherals. This output is available on the RTCC pin. The output pulse is a clock with a 50% duty cycle and a frequency half that of the alarm event (see Figure 17-6).

The RTCC pin also can output the seconds clock. The user can select between the alarm pulse, generated by the RTCC module, or the seconds clock output.

The RTSECSEL<1:0> bits (PADCFG1<2:1>) select between these two outputs:

- Alarm pulse – RTSECSEL<1:0> = 00
- Seconds clock – RTSECSEL<1:0> = 01

19.3 Compare Mode

In Compare mode, the 16-bit CCPRx register value is constantly compared against either the TMR1 or TMR3 register pair value. When a match occurs, the ECCPx pin can be:

- Driven high
- Driven low
- Toggled (high-to-low or low-to-high)
- Unchanged (that is, reflecting the state of the I/O latch)

The action on the pin is based on the value of the mode select bits (CCPxM<3:0>). At the same time, the interrupt flag bit, CCPxIF, is set.

19.3.1 ECCP PIN CONFIGURATION

Users must configure the ECCPx pin as an output by clearing the appropriate TRIS bit.

Note:	Clearing the CCPxCON register will force the ECCPx compare output latch (depending on device configuration) to the default low level. This is not the PORTx I/O data latch.

19.3.2 TIMER1/TIMER3 MODE SELECTION

Timer1 and/or Timer3 must be running in Timer mode or Synchronized Counter mode if the ECCP module is using the compare feature. In Asynchronous Counter mode, the compare operation will not work reliably.

19.3.3 SOFTWARE INTERRUPT MODE

When the Generate Software Interrupt mode is chosen (CCPxM<3:0> = 1010), the ECCPx pin is not affected; only the CCPxIF interrupt flag is affected.

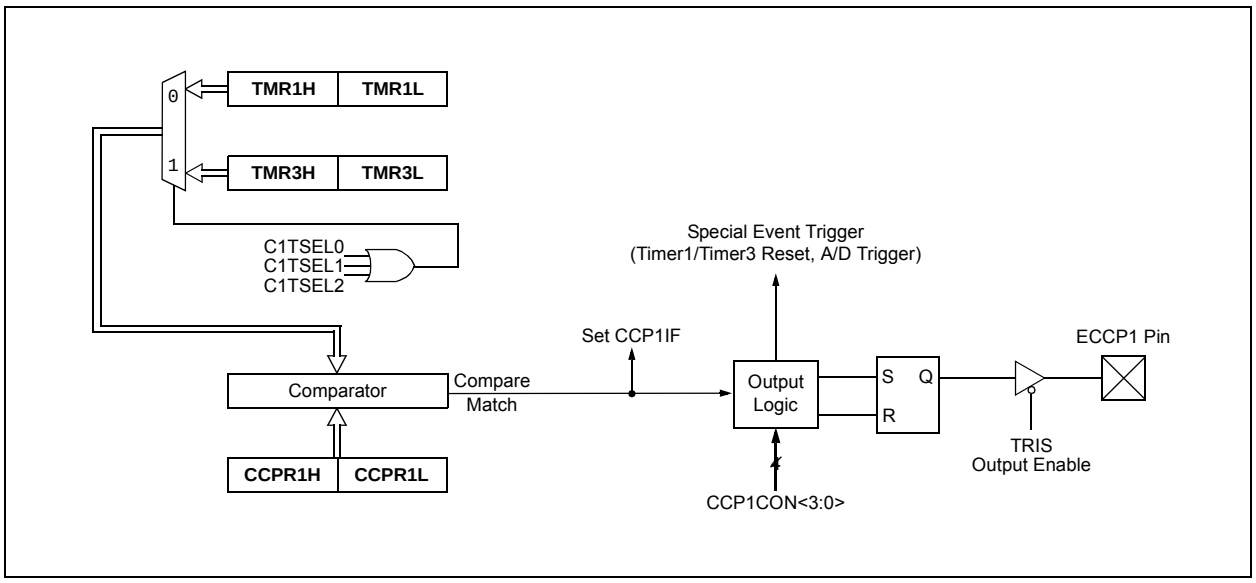
19.3.4 SPECIAL EVENT TRIGGER

The ECCP module is equipped with a Special Event Trigger. This is an internal hardware signal generated in Compare mode to trigger actions by other modules. The Special Event Trigger is enabled by selecting the Compare Special Event Trigger mode (CCPxM<3:0> = 1011).

The Special Event Trigger resets the Timer register pair for whichever timer resource is currently assigned as the module's time base. This allows the CCPRx registers to serve as a programmable Period register for either timer.

The Special Event Trigger can also start an A/D conversion. In order to do this, the A/D Converter must already be enabled.

FIGURE 19-2: COMPARE MODE OPERATION BLOCK DIAGRAM



19.4.2 FULL-BRIDGE MODE

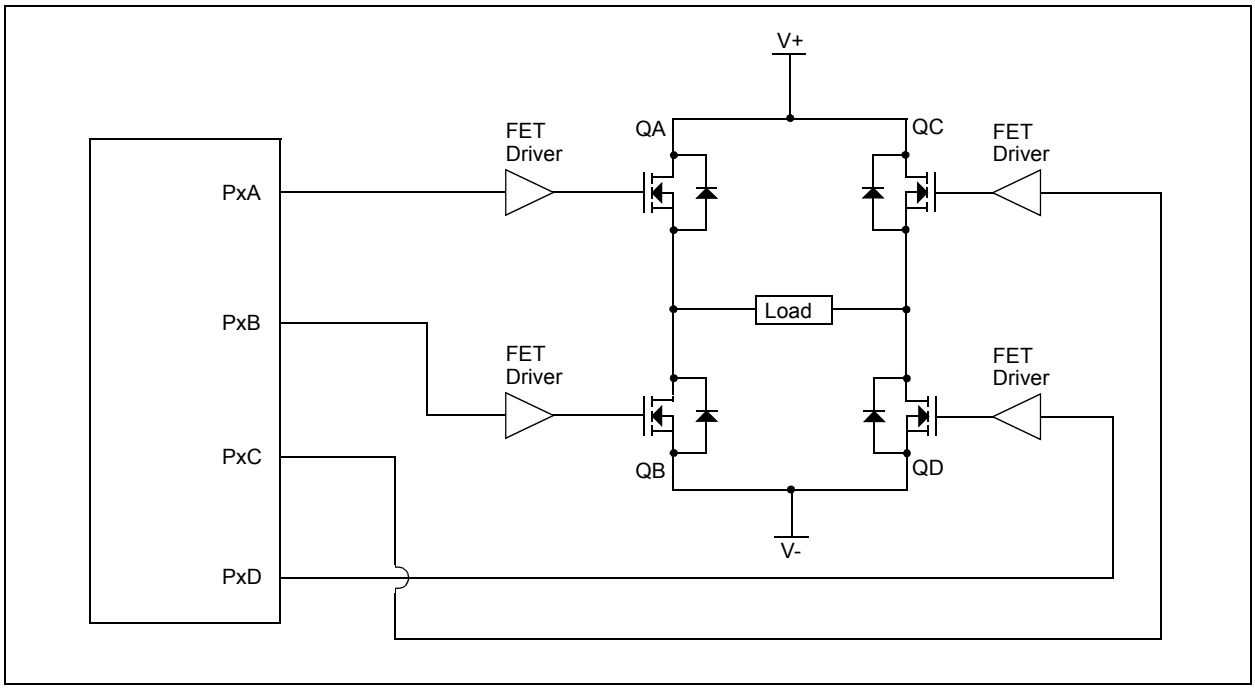
In Full-Bridge mode, all four pins are used as outputs. An example of a full-bridge application is provided in Figure 19-8.

In the Forward mode, the PxA pin is driven to its active state and the PxD pin is modulated, while the PxB and PxC pins are driven to their inactive state, as provided in Figure 19-9.

In the Reverse mode, the PxC pin is driven to its active state and the PxB pin is modulated, while the PxA and PxD pins are driven to their inactive state, as provided Figure 19-9.

The PxA, PxB, PxC and PxD outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the PxA, PxB, PxC and PxD pins as outputs.

FIGURE 19-8: EXAMPLE OF FULL-BRIDGE APPLICATION



21.3.6 MASTER MODE

The master can initiate the data transfer at any time because it controls the SCKx. The master determines when the slave (Processor 1, Figure 21-2) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPxBUF register is written to. If the SPI is only going to receive, the SDOx output could be disabled (programmed as an input). The SSPxSR register will continue to shift in the signal present on the SDIx pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPxBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a “Line Activity Monitor” mode.

The clock polarity is selected by appropriately programming the CKP bit (SSPxCON1<4>). This, then, would give waveforms for SPI communication as shown in Figure 21-3, Figure 21-5 and Figure 21-6, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user-programmable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 • TCY)
- FOSC/64 (or 16 • TCY)
- Timer2 output/2

This allows a maximum data rate (at 40 MHz) of 10.00 Mbps.

Figure 21-3 shows the waveforms for Master mode. When the CKE bit is set, the SDOx data is valid before there is a clock edge on SCKx. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPxBUF is loaded with the received data is shown.

FIGURE 21-3: SPI MODE WAVEFORM (MASTER MODE)

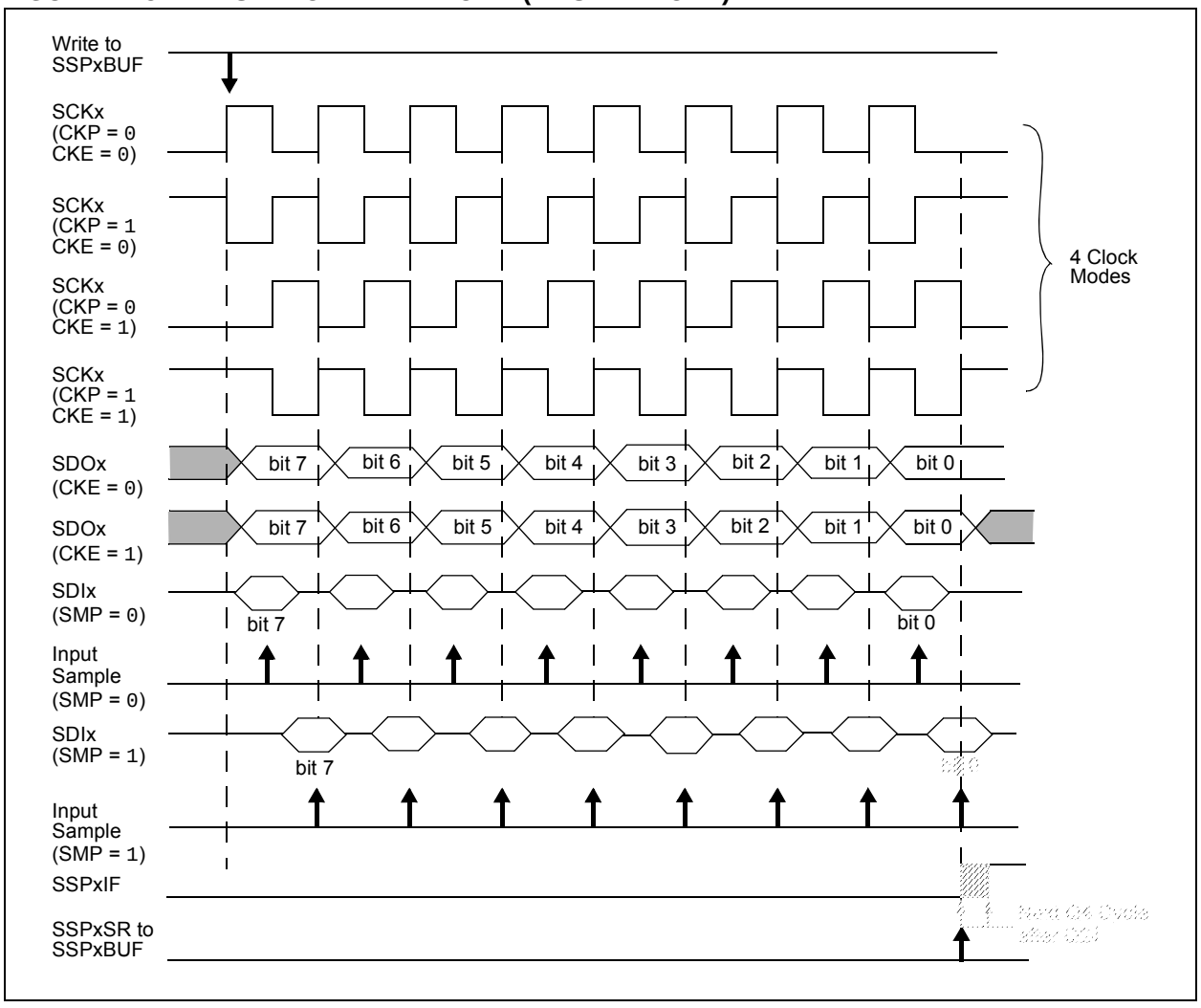


FIGURE 21-23: I²C™ MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)

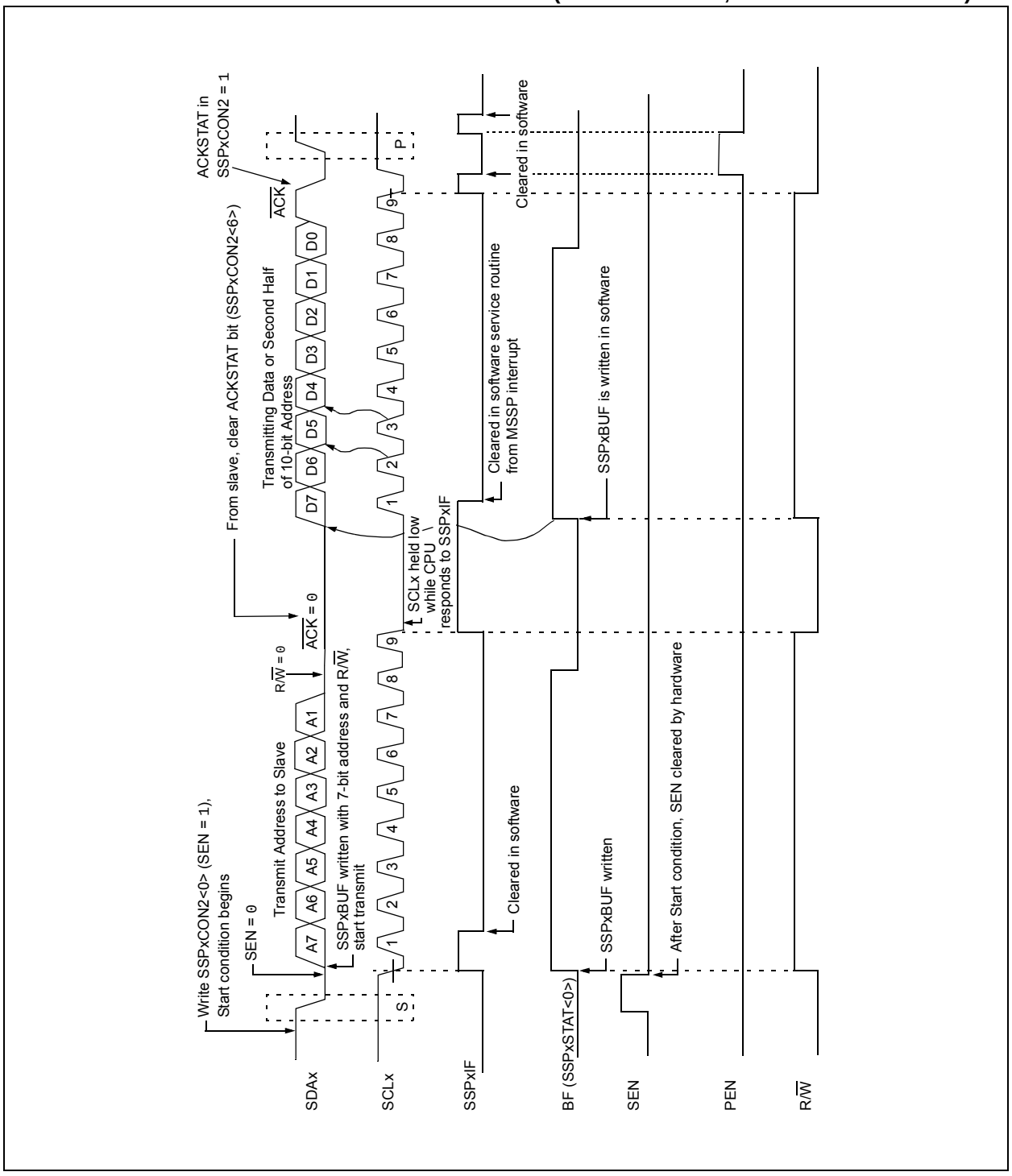


TABLE 21-4: REGISTERS ASSOCIATED WITH I²C™ OPERATION

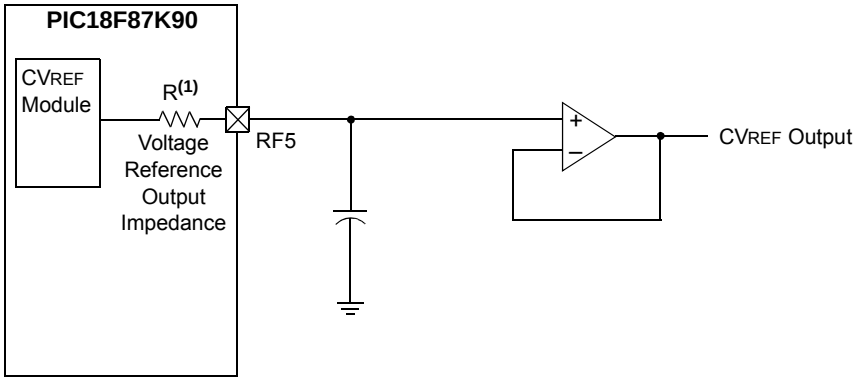
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	TMR1GIF	TMR2IF	TMR1IF	77
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	TMR1GIE	TMR2IE	TMR1IE	77
IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	TMR1GIP	TMR2IP	TMR1IP	77
PIR2	OSCFIF	—	SSP2IF	BLC2IF	BCL1IF	HLVDIF	TMR3IF	TMR3GIF	77
PIE2	OSCFIE	—	SSP2IE	BLC2IE	BCL1IE	HLVDIE	TMR3IE	TMR3GIE	77
IPR2	OSCFIP	—	SSP2IP	BLC2IP	BCL1IP	HLVDIP	TMR3IP	TMR3GIP	77
PIR3	TMR5GIF	LCDIF	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	RTCCIF	77
PIE3	TMR5GIE	LCDIE	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE	77
IPR3	TMR5GIP	LCDIP	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	RTCCIP	77
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	78
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	78
SSP1BUF	MSSP1 Receive Buffer/Transmit Register								76
SSP1ADD	MSSP1 Address Register (I²C™ Slave mode), MSSP1 Baud Rate Reload Register (I²C Master mode)								76
SSP1MSK(1)	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	—
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	76
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	76
	GCEN	ACKSTAT	ADMSK5(2)	ADMSK4(2)	ADMSK3(2)	ADMSK2(2)	ADMSK1(2)	SEN	
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	76
SSP2BUF	MSSP2 Receive Buffer/Transmit Register								82
SSP2ADD	MSSP2 Address Register (I²C Slave mode), MSSP2 Baud Rate Reload Register (I²C Master mode)								82
SSP2MSK(1)	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	—
SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	82
SSP2CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	83
	GCEN	ACKSTAT	ADMSK5(2)	ADMSK4(2)	ADMSK3(2)	ADMSK2(2)	ADMSK1(2)	SEN	
SSP2STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	82

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the MSSP module in I²C™ mode.

Note 1: SSPxMSK shares the same address in SFR space as SSPxADD, but is only accessible in certain I²C™ Slave operating modes in 7-Bit Masking mode. See **Section 21.4.3.4 "7-Bit Address Masking Mode"** for more details.

2: Alternate bit definitions for use in I²C Slave mode operations only.

FIGURE 25-2: COMPARATOR VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



Note 1: R is dependent upon the Voltage Reference Configuration bits, CVRCON<3:0> and CVRCON<5>.

TABLE 25-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
CVRCON	CVREN	CVROE	CVRSS	CVR4	CVR3	CVR2	CVR1	CVR0	77
CM1CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0	80
CM2CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0	81
CM3CON	CON	COE	CPOL	EVPOL1	EVPOL0	CREF	CCH1	CCH0	81
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—	78

Legend: — = unimplemented, read as '0'. Shaded cells are not used with the comparator voltage reference.

26.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The PIC18F87K90 family of devices has a High/Low-Voltage Detect module (HLVD). This is a programmable circuit that sets both a device voltage trip point and the direction of change from that point. If the device experiences an excursion past the trip point in that direction, an interrupt flag is set. If the interrupt is enabled, the program execution branches to the interrupt vector address and the software responds to the interrupt.

The High/Low-Voltage Detect Control register (Register 26-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

The module's block diagram is shown in Figure 26-1.

REGISTER 26-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL3(1)	HLVDL2(1)	HLVDL1(1)	HLVDL0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **VDIRMAG:** Voltage Direction Magnitude Select bit
1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 6 **BGVST:** Band Gap Reference Voltages Stable Status Flag bit
1 = Internal band gap voltage references are stable
0 = Internal band gap voltage references are not stable

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
1 = Indicates that the voltage detect logic will generate the interrupt flag at the specified voltage range
0 = Indicates that the voltage detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 4 **HLVDEN:** High/Low-Voltage Detect Power Enable bit
1 = HLVD is enabled
0 = HLVD is disabled

bit 3-0 **HLVDL<3:0>:** Voltage Detection Limit bits(1)
1111 = External analog input is used (input comes from the HLVDIN pin)
1110 = Maximum setting
.
.
.
0000 = Minimum setting

Note 1: For the electrical specifications, see Parameter D420.

REGISTER 28-11: CONFIG6H: CONFIGURATION REGISTER 6 HIGH (BYTE ADDRESS 30000Bh)(2)

R/C-1	R/C-1	R-1	U-0	U-0	U-0	U-0	U-0
WRTD	WRTB	WRTC(1)	—	—	—	—	—
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WRTD:** Data EEPROM Write Protection bit
1 = Data EEPROM is not write-protected
0 = Data EEPROM is write-protected

bit 6 **WRTB:** Boot Block Write Protection bit
1 = Boot block is not write-protected
0 = Boot block is write-protected

bit 5 **WRTC:** Configuration Register Write Protection bit(1)
1 = Configuration registers are not write-protected
0 = Configuration registers are write-protected

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is read-only in Normal Execution mode; it can be written only in Program mode.
2: For the memory size of the blocks, refer to Figure 28-6.

RLNCF **Rotate Left f (No Carry)**

Syntax: RLNCF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f<n>) → dest<n + 1>,
(f<7>) → dest<0>

Status Affected: N, Z

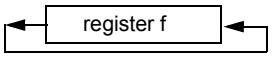
Encoding:

0100	01da	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the left. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example:
```
RLNCF   REG, 1, 0
```
Before Instruction
```
REG  =  1010 1011
```
After Instruction
```
REG  =  0101 0111
```

RRCF **Rotate Right f through Carry**

Syntax: RRCF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (f<n>) → dest<n – 1>,
(f<0>) → C,
(C) → dest<7>

Status Affected: C, N, Z

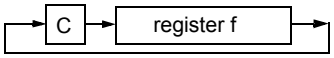
Encoding:

0011	00da	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example:
```
RRCF    REG, 0, 0
```
Before Instruction
```
REG  =  1110 0110
C    =  0
```
After Instruction
```
REG  =  1110 0110
W    =  0111 0011
C    =  0
```