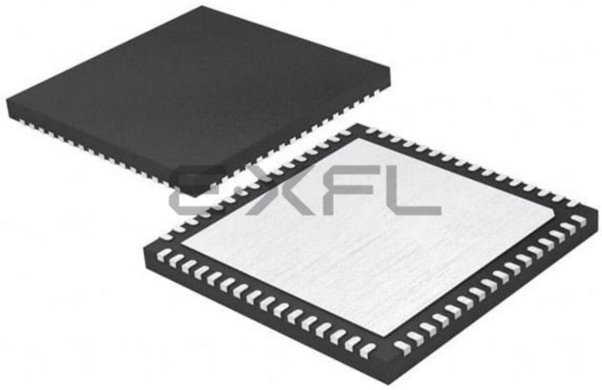

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f65k90t-i-mrrsl

Special Microcontroller Features:

- Operating Voltage Range: 1.8V to 5.5V
- On-Chip 3.3V Regulator
- Operating Speed up to 64 MHz
- Up to 128 Kbytes On-Chip Flash Program Memory
- Data EEPROM of 1,024 Bytes
- 4K x 8 General Purpose Registers (SRAM)
- 10,000 Erase/Write Cycle Flash Program Memory, Minimum
- 1,000,000 Erase/write Cycle Data EEPROM Memory, Typical
- Flash Retention 40 Years, Minimum
- Three Internal Oscillators: LF-INTRC (31 kHz), MF-INTOSC (500 kHz) and HF-INTOSC (16 MHz)
- Self-Programmable under Software Control
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  - Programmable period from 4 ms to 4,194s (about 70 minutes)
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  - BOR
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- Two Enhanced Addressable USART modules:
  - LIN/J2602 support
  - Auto-Baud Detect (ABD)
- 12-Bit A/D Converter with up to 24 Channels:
  - Auto-acquisition and Sleep operation
  - Differential Input mode of operation

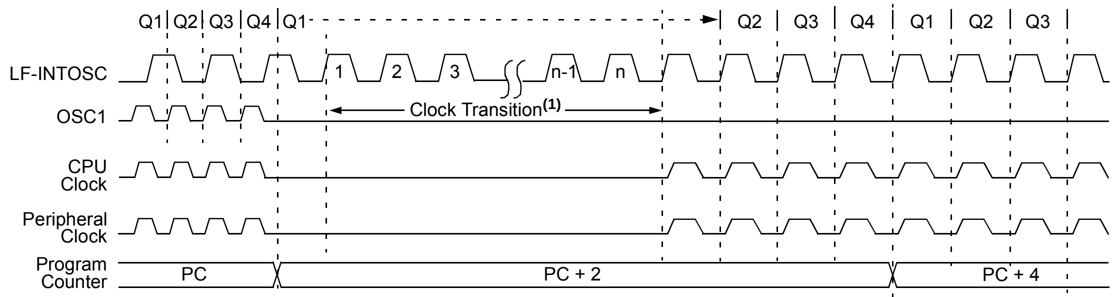
TABLE 1-4: PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTC is a bidirectional I/O port.
RC0/SOSCO/SCKLI	36			
RC0		I/O	ST	Digital I/O.
SOSCO		O	—	SOSC oscillator output.
SCKLI		I	ST	Digital SOSC input.
RC1/SOSCI/ECCP2/SEG32/P2A	35			
RC1		I/O	ST	Digital I/O.
SOSCI		I	CMOS	SOSC oscillator input.
ECCP2(1)		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
SEG32		O	Analog	SEG32 output for LCD.
P2A		O	—	Enhanced PWM2 Output A.
RC2/ECCP1/P1A/SEG13	43			
RC2		I/O	ST	Digital I/O.
ECCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
P1A		O	—	Enhanced PWM1 Output A.
SEG13		O	Analog	SEG13 output for LCD.
RC3/SCK1/SCL1/SEG17	44			
RC3		I/O	ST	Digital I/O.
SCK1		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL1		I/O	ST	Synchronous serial clock input/output for I^2C™ mode.
SEG17		O	Analog	SEG17 output for LCD.
RC4/SDI1/SDA1/SEG16	45			
RC4		I/O	ST	Digital I/O.
SDI1		I	ST	SPI data in.
SDA1		I/O	ST	I^2C data I/O.
SEG16		O	Analog	SEG16 output for LCD.
RC5/SDO1/SEG12	46			
RC5		I/O	ST	Digital I/O.
SDO1		O	—	SPI data out.
SEG12		O	Analog	SEG12 output for LCD.
RC6/TX1/CK1/SEG27	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART asynchronous transmit.
CK1		I/O	ST	EUSART synchronous clock (see related RX1/DT1).
SEG27		O	Analog	SEG27 output for LCD.
RC7/RX1/DT1/SEG28	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART asynchronous receive.
DT1		I/O	ST	EUSART synchronous data (see related TX1/CK1).
SEG28		O	Analog	SEG28 output for LCD.

Legend: TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I = Input; P = Power; I^2C™ = I^2C/SMBus; CMOS = CMOS compatible input or output; Analog = Analog input; O = Output; OD = Open-Drain (no P diode to V_{DD})

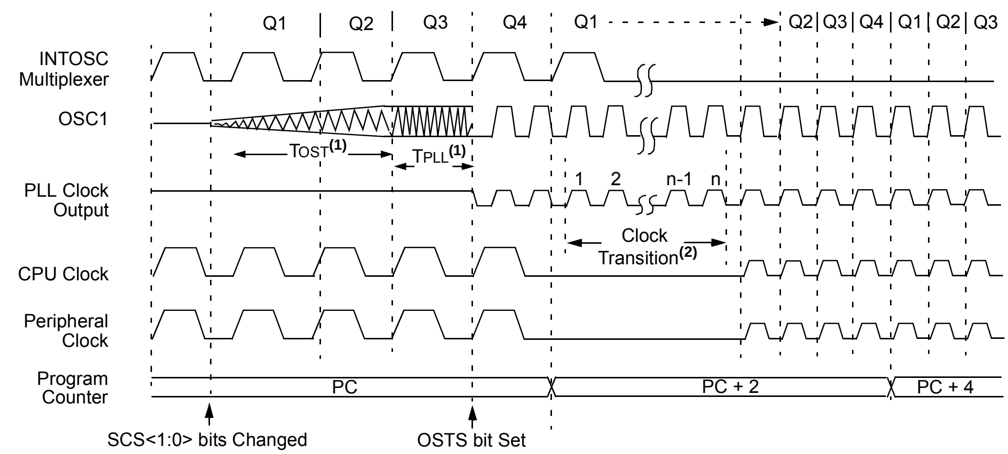
Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

FIGURE 4-3: TRANSITION TIMING TO RC_RUN MODE



Note 1: Clock transition typically occurs within 2-4 TOSC.

FIGURE 4-4: TRANSITION TIMING FROM RC_RUN MODE TO PRI_RUN MODE



Note 1: TOST = 1024 TOSC; TPLL = 2 ms (approx). These intervals are not shown to scale.

2: Clock transition typically occurs within 2-4 TOSC.

TABLE 5-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{MCLR}$ Resets, WDT Reset, RESET Instruction, Stack Resets, CM Resets	Wake-up via WDT or Interrupt
INDF2	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTINC2	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
POSTDEC2	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PREINC2	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
PLUSW2	PIC18F6XK90	PIC18F8XK90	N/A	N/A	N/A
FSR2H	PIC18F6XK90	PIC18F8XK90	---- 0000	---- 0000	---- uuuu
FSR2L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS(4)	PIC18F6XK90	PIC18F8XK90	---x xxxx	---u uuuu	---u uuuu
TMR0H	PIC18F6XK90	PIC18F8XK90	0000 0000	uuuu uuuu	uuuu uuuu
TMR0L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
SPBRGH1	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
OSCCON	PIC18F6XK90	PIC18F8XK90	0110 q000	0110 q000	uuuu quuu
IPR5	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
WDTCON	PIC18F6XK90	PIC18F8XK90	0-x0 -000	0-x0 -000	u-uu -uuu
RCON	PIC18F6XK90	PIC18F8XK90	0111 11qq	0uqq qquu	uuuu qquu
TMR1H	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	PIC18F6XK90	PIC18F8XK90	0000 0000	uuuu uuuu	uuuu uuuu
TMR2	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
PR2	PIC18F6XK90	PIC18F8XK90	1111 1111	1111 1111	uuuu uuuu
T2CON	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu
SSP1BUF	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSP1ADD	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
SSP1STAT	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
SSP1CON1	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
SSP1CON2	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
ADRESH	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADRESL	PIC18F6XK90	PIC18F8XK90	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	PIC18F6XK90	PIC18F8XK90	-000 0000	-000 0000	-uuu uuuu
ADCON1	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu
ADCON2	PIC18F6XK90	PIC18F8XK90	0-00 0000	0-00 0000	u-uu uuuu
ECCP1AS	PIC18F6XK90	PIC18F8XK90	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

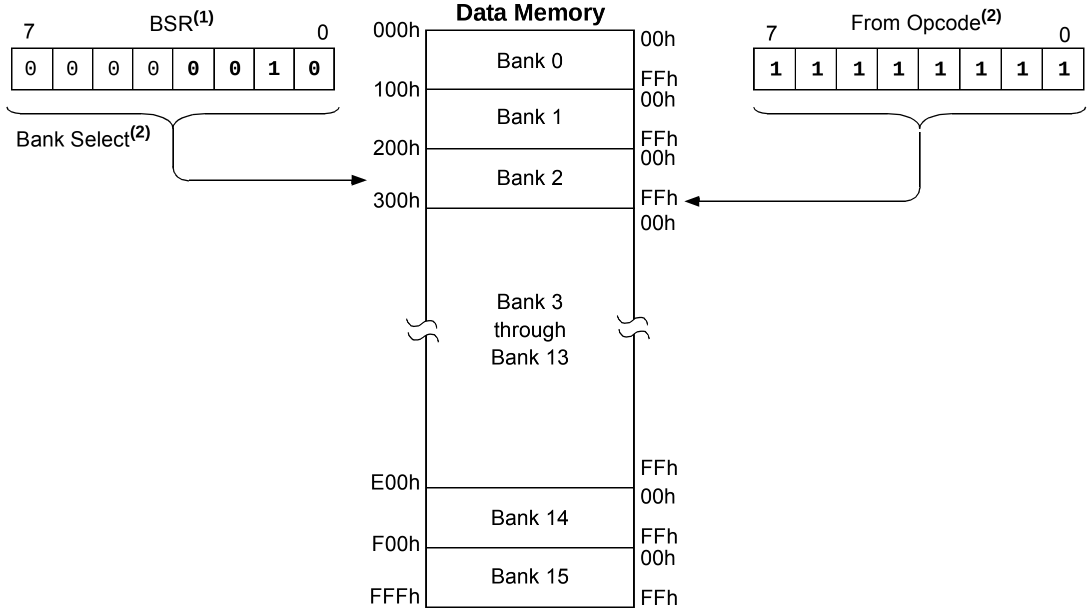
Note 1: When the wake-up is due to an interrupt, and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 5-1 for the Reset value for a specific condition.

FIGURE 6-7: USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)



Note 1: The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to the registers of the Access Bank.

2: The `MOVFF` instruction embeds the entire 12-bit address in the instruction.

6.3.2 ACCESS BANK

While the use of the BSR, with an embedded 8-bit address, allows users to address the entire range of data memory, it also means that the user must ensure that the correct bank is selected. If not, data may be read from, or written to, the wrong location. This can be disastrous if a GPR is the intended target of an operation, but an SFR is written to instead. But verifying and/or changing the BSR for each read or write to data memory can become very inefficient.

To streamline access for the most commonly used data memory locations, the data memory is configured with an Access Bank, which allows users to access a mapped block of memory without specifying a BSR. The Access Bank consists of the first 96 bytes of memory (00h-5Fh) in Bank 0 and the last 160 bytes of memory (60h-FFh) in Bank 15. The lower half is known as the "Access RAM" and is composed of GPRs. The upper half is where the device's SFRs are mapped. These two areas are mapped contiguously in the Access Bank and can be addressed in a linear fashion by an 8-bit address (Figure 6-6).

The Access Bank is used by core PIC18 instructions that include the Access RAM bit (the 'a' parameter in the instruction). When 'a' is equal to '`1`', the instruction uses the BSR and the 8-bit address included in the opcode for the data memory address. When 'a' is '`0`', however, the instruction is forced to use the Access Bank address map. In that case, the current value of the BSR is ignored entirely.

Using this "forced" addressing allows the instruction to operate on a data address in a single cycle without updating the BSR first. For 8-bit addresses of 60h and above, this means that users can evaluate and operate on SFRs more efficiently. The Access RAM below 60h is a good place for data values that the user might need to access rapidly, such as immediate computational results or common program variables.

Access RAM also allows for faster and more code efficient context saving and switching of variables.

The mapping of the Access Bank is slightly different when the extended instruction set is enabled (XINST Configuration bit = `1`). This is discussed in more detail in **Section 6.6.3 "Mapping the Access Bank in Indexed Literal Offset Mode"**.

6.3.3 GENERAL PURPOSE REGISTER FILE

PIC18 devices may have banked memory in the GPR area. This is data RAM which is available for use by all instructions. GPRs start at the bottom of Bank 0 (address 000h) and grow upwards towards the bottom of the SFR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other Resets.

REGISTER 10-7: PIR4: PERIPHERAL INTERRUPT FLAG REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP10IF(1)	CCP9IF(1)	CCP8IF	CCP7IF	CCP6IF	CCP5IF	CCP4IF	CCP3IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-1 **CCP10IF:CCP4IF:** CCP<10:4> Interrupt Flag bits(1)

Capture Mode
1 = A TMR register capture occurred (must be cleared in software)
0 = No TMR register capture occurred

Compare Mode
1 = A TMR register compare match occurred (must be cleared in software)
0 = No TMR register compare match occurred

PWM Mode
Not used in PWM mode.

bit 0 **CCP3IF:** ECCP3 Interrupt Flag bits

Capture Mode
1 = A TMR register capture occurred (must be cleared in software)
0 = No TMR register capture occurred

Compare Mode
1 = A TMR register compare match occurred (must be cleared in software)
0 = No TMR register compare match occurred

PWM Mode
Not used in PWM mode.

Note 1: Unimplemented in devices with a program memory of 32 Kbytes (PIC18FX5K90).

REGISTER 10-9: PIR6: PERIPHERAL INTERRUPT FLAG REGISTER 6

U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	EEIF	—	CMP3IF	CMP2IF	CMP1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **EEIF:** Data EEDATA/Flash Write Operation Interrupt Flag bit
1 = The write operation is complete (must be cleared in software)
0 = The write operation is not complete, or has not been started

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **CMP3IF:** CMP3 Interrupt Flag bit
1 = CMP3 interrupt occurred (must be cleared in software)
0 = No CMP3 interrupt occurred

bit 1 **CMP2IF:** CMP2 Interrupt Flag bit
1 = CMP2 interrupt occurred (must be cleared in software)
0 = No CMP2 interrupt occurred

bit 0 **CMP1IF:** CM1 Interrupt Flag bit
1 = CMP1 interrupt occurred (must be cleared in software)
0 = No CMP1 interrupt occurred

REGISTER 10-12: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TMR5GIE	LCDIE(1)	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **TMR5GIE:** Timer5 Gate Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 6 **LCDIE:** LCD Interrupt Enable bit(1)
1 = Enabled
0 = Disabled

bit 5 **RC2IE:** AUSART Receive Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 4 **TX2IE:** AUSART Transmit Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 3 **CTMUIE:** CTMU Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **CCP2IE:** ECCP2 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 **CCP1IE:** ECCP1 Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 **RTCCIE:** RTCC Interrupt Enable bit
1 = Enabled
0 = Disabled

Note 1: This bit is valid when the Type-B waveform with Non-Static mode is selected.

REGISTER 10-13: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCP10IE(1)	CCP9IE(1)	CCP8IE	CCP7IE	CCP6IE	CCP5IE	CCP4IE	CCP3IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CCP10IE:CCP3IE:** CCP<10:3> Interrupt Enable bits(1)
1 = Enabled
0 = Disabled

Note 1: CCP10IE and CCP9IE are unimplemented in devices with a program memory of 32 Kbytes (PIC18FX5K90).

15.0 TIMER3/5/7 MODULES

The Timer3/5/7 timer/counter modules incorporate these features:

- Software-selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMRxH and TMRxL)
- Selectable clock source (internal or external) with device clock or SOSC oscillator internal options
- Interrupt-on-overflow
- Module Reset on ECCP Special Event Trigger

Timer7 is unimplemented for devices with a program memory of 32 Kbytes (PIC18FX5K90).

Note:	Throughout this section, generic references are used for register and bit names that are the same, except for an ‘x’ variable that indicates the item’s association with the Timer3, Timer5 or Timer7 module. For example, the control register is named TxCON and refers to T3CON, T5CON and T7CON.

A simplified block diagram of the Timer3/5/7 module is shown in Figure 15-1.

The Timer3/5/7 module is controlled through the TxCON register (Register 15-1). It also selects the clock source options for the ECCP modules. (For more information, see **Section 19.1.1 “ECCP Module and Timer Resources”**.)

The FOSC clock source should not be used with the ECCP capture/compare features. If the timer will be used with the capture or compare features, always select one of the other timer clocking options.

REGISTER 17-11: HOUR: HOUR VALUE REGISTER(1)

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour’s Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour’s Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 17-12: MINUTE: MINUTE VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute’s Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **MINONE<3:0>:** Binary Coded Decimal Value of Minute’s Ones Digit bits
Contains a value from 0 to 9.

REGISTER 17-13: SECOND: SECOND VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second’s Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second’s Ones Digit bits
Contains a value from 0 to 9.

The LCDSE5:LCDSE0 registers configure the functions of the port pins. Setting the segment enable bit for a particular segment configures that pin as an LCD driver. There are six LCD Segment Enable registers, as shown in Table 20-1. The prototype LCDSEx register is shown in Register 20-5.

TABLE 20-1: LCDSE REGISTERS AND ASSOCIATED SEGMENTS

Register	Segments
LCDSE0	7:0 (RD<7:0>)
LCDSE1	15:8 (RA<5:4>, RC2, RC5, RB<4:1>)
LCDSE2	23:16 (RF<5:1>, RA1, RC<4:3>)
LCDSE3	31:24 (RE7, RB0, RB5, RC<7:6>, RG4, RF<7:6>)
LCDSE4	39:32 (RJ<4:7>, RJ<3:1>, RC1)
LCDSE5	47:40 (RH<0:3>, RH<7:4>)

> **Note:** The LCDSE5:LCDSE4 registers are not implemented in PIC18F6XK90 devices.

Once the module is initialized for the LCD panel, the individual bits of the LCDDATA23:LCDDATA0 registers are cleared or set to represent a clear or dark pixel, respectively.

Specific sets of LCDDATA registers are used with specific segments and common signals. Each bit represents a unique combination of a specific segment connected to a specific common.

Individual LCDDATA bits are named by the convention, "SxxCy", with "xx" as the segment number and "y" as the common number. The relationship is summarized in Table 20-2. The prototype LCDDATAx register is shown in Register 20-6.

> **Note:** In PIC18F6XK90 devices, writing into the registers, LCDDATA4, LCDDATA5, LCDDATA10, LCDDATA11, LCDDATA16, LCDDATA17, LCDDATA22 and LCDDATA23, will not affect the status of any pixel. These registers can be used as general purpose registers.

REGISTER 20-5: LCDSEx: LCD SEGMENTx ENABLE REGISTER

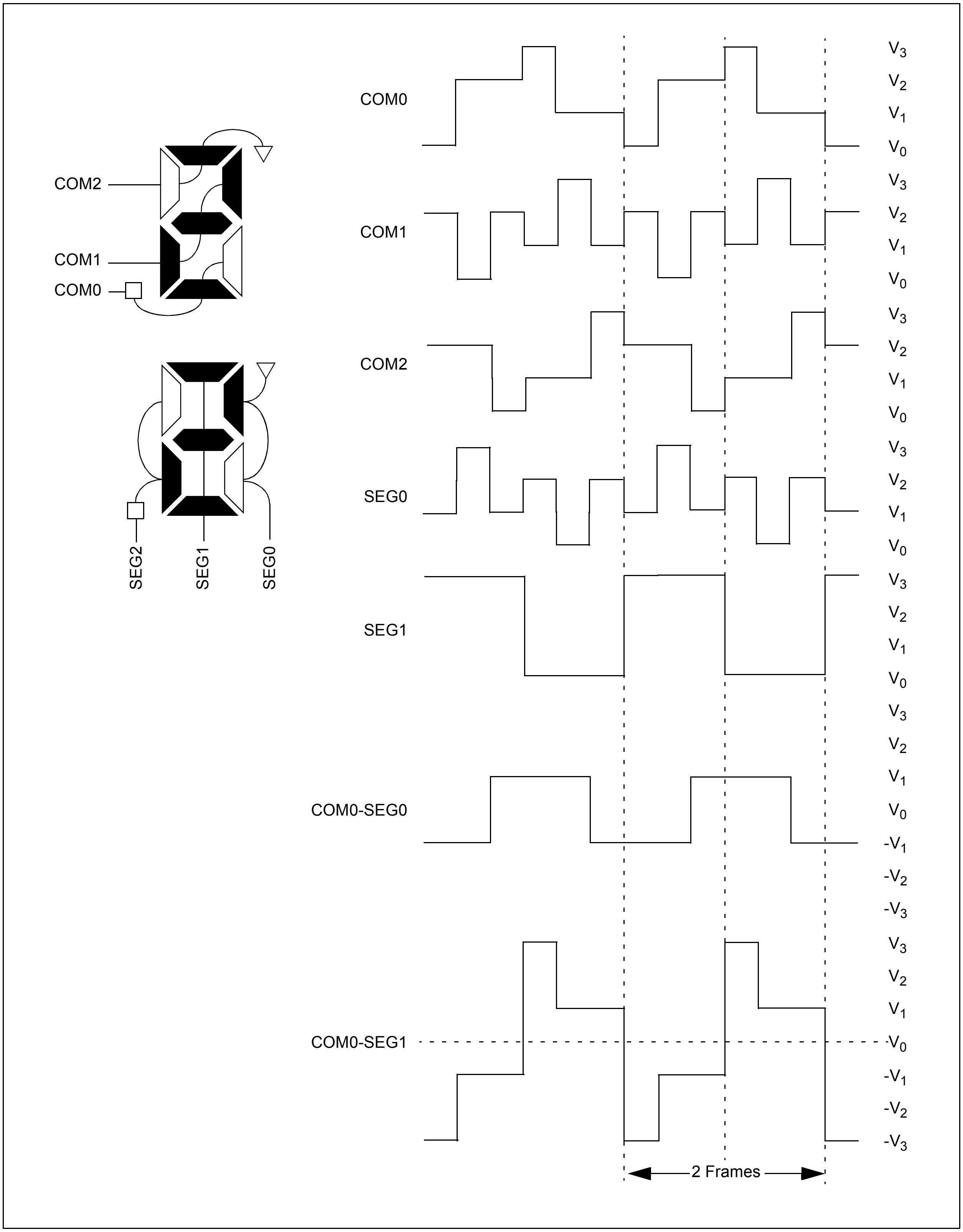
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SE(n + 7)	SE(n + 6)	SE(n + 5)	SE(n + 4)	SE(n + 3)	SE(n + 2)	SE(n + 1)	SE(n)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SE(n + 7):SE(n):** Segment Enable bits

For LCDSE0: n = 0
For LCDSE1: n = 8
For LCDSE2: n = 16
For LCDSE3: n = 24
For LCDSE4: n = 32
For LCDSE5: n = 40
1 = Segment function of the pin is enabled, digital I/O is disabled
0 = I/O function of the pin is enabled

FIGURE 20-15: TYPE-B WAVEFORMS IN 1/3 MUX, 1/3 BIAS DRIVE



21.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDAx when SCLx goes from a low level to a high level.

b) SCLx goes low before SDAx is asserted low, indicating that another master is attempting to transmit a data ‘1’.

When the user deasserts SDAx and the pin is allowed to float high, the BRG is loaded with SSPxADD<6:0> and counts down to 0. The SCLx pin is then deasserted and when sampled high, the SDAx pin is sampled.

If SDAx is low, a bus collision has occurred (i.e., another master is attempting to transmit a data ‘0’, Figure 21-31). If SDAx is sampled high, the BRG is reloaded and begins counting. If SDAx goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDAx at exactly the same time.

If SCLx goes from high-to-low before the BRG times out and SDAx has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data ‘1’ during the Repeated Start condition (see Figure 21-32).

If, at the end of the BRG time-out, both SCLx and SDAx are still high, the SDAx pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCLx pin, the SCLx pin is driven low and the Repeated Start condition is complete.

FIGURE 21-31: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

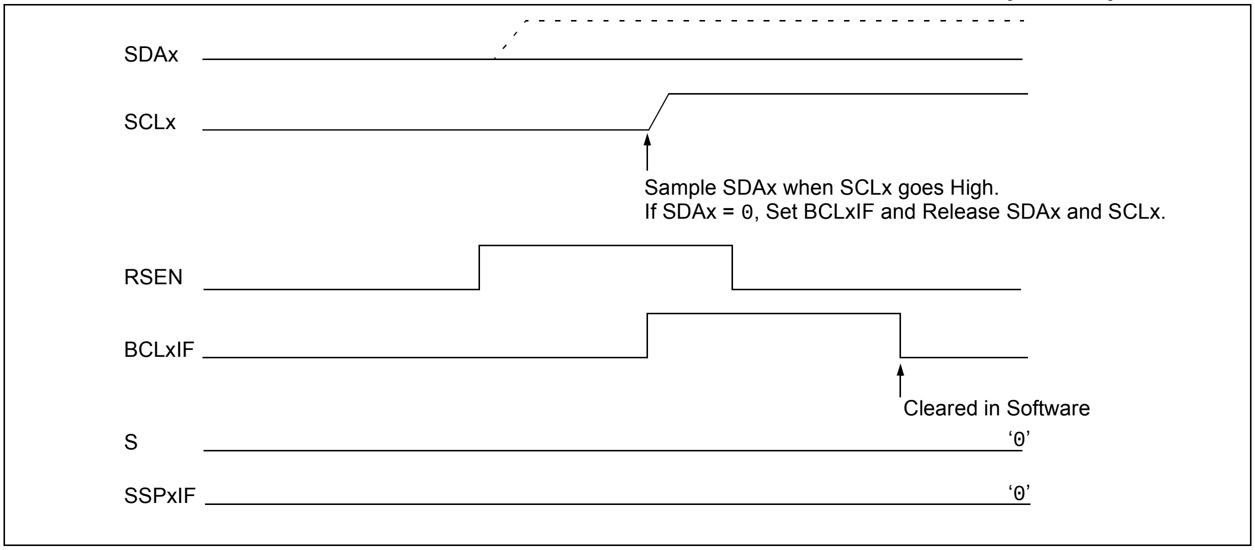
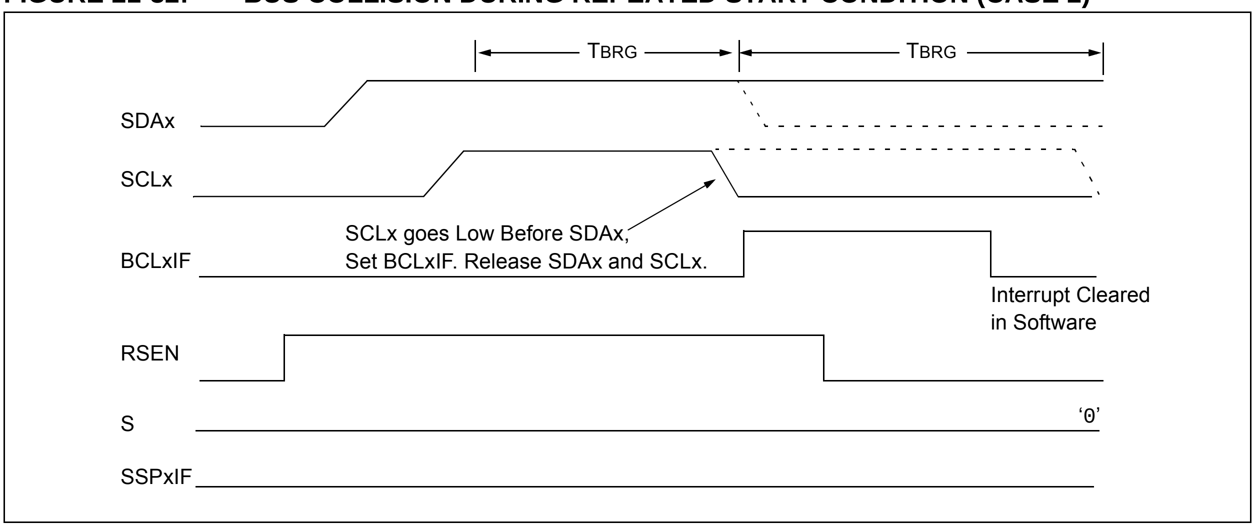


FIGURE 21-32: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



22.2.4 AUTO-WAKE-UP ON SYNC BREAK CHARACTER

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper byte reception cannot be performed. The auto-wake-up feature allows the controller to wake-up due to activity on the RXx/DTx line while the EUSART is operating in Asynchronous mode.

The auto-wake-up feature is enabled by setting the WUE bit (BAUDCONx<1>). Once set, the typical receive sequence on RXx/DTx is disabled and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RXx/DTx line. (This coincides with the start of a Sync Break or a Wake-up Signal character for the LIN/J2602 protocol.)

Following a wake-up event, the module generates an RCxIF interrupt. The interrupt is generated synchronously to the Q clocks in normal operating modes (Figure 22-8) and asynchronously if the device is in Sleep mode (Figure 22-9). The interrupt condition is cleared by reading the RCREGx register.

The WUE bit is automatically cleared once a low-to-high transition is observed on the RXx line following the wake-up event. At this point, the EUSART module is in Idle mode and returns to normal operation. This signals to the user that the Sync Break event is over.

22.2.4.1 Special Considerations Using Auto-Wake-up

Since auto-wake-up functions by sensing rising edge transitions on RXx/DTx, information with any state changes before the Stop bit may signal a false End-of-Character (EOC) and cause data or framing errors. To work properly, therefore, the initial character in the transmission must be all '0's. This can be 00h (8 bits) for standard RS-232 devices or 000h (12 bits) for LIN/J2602 bus.

Oscillator start-up time must also be considered, especially in applications using oscillators with longer start-up intervals (i.e., HS or HSPLL mode). The Sync Break (or Wake-up Signal) character must be of sufficient length and be followed by a sufficient interval to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

26.6 Operation During Sleep

When enabled, the HLVD circuitry continues to operate during Sleep. If the device voltage crosses the trip point, the HLVDIF bit will be set and the device will wake-up from Sleep. Device execution will continue from the interrupt vector address if interrupts have been globally enabled.

26.7 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the HLVD module to be turned off.

TABLE 26-1: REGISTERS ASSOCIATED WITH HIGH/LOW-VOLTAGE DETECT MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
HLVDCON	VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0	77
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75
PIR2	OSCFIF	—	SSP2IF	BLC2IF	BCL1IF	HLVDIF	TMR3IF	TMR3GIF	77
PIE2	OSCFIE	—	SSP2IE	BLC2IE	BCL1IE	HLVDIE	TMR3IE	TMR3GIE	77
IPR2	OSCFIP	—	SSP2IP	BLC2IP	BCL1IP	HLVDIP	TMR3IP	TMR3GIP	77
TRISA	TRISA7(1)	TRISA6(1)	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	78

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the HLVD module.

Note 1: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

27.1 CTMU Registers

The control registers for the CTMU are:

- CTMUCONH
- CTMUCONL
- CTMUICON

The CTMUCONH and CTMUCONL registers (Register 27-1 and Register 27-2) contain control bits for configuring the CTMU module edge source selection, edge source polarity selection, edge sequencing, A/D trigger, analog circuit capacitor discharge and enables. The CTMUICON register (Register 27-3) has bits for selecting the current source range and current source trim.

REGISTER 27-1: CTMUCONH: CTMU CONTROL HIGH REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **CTMUSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 4 **TGEN:** Time Generation Enable bit
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 3 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 2 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 1 **IDISSEN:** Analog Current Source Control bit
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 0 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

REGISTER 28-14: DEVID1: DEVICE ID REGISTER 1 FOR THE PIC18F87K90 FAMILY

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **DEV<2:0>:** Device ID bits

Devices with DEV<10:3> of `0101 0010` (see DEVID2):
`010` = PIC18F65K90
`000` = PIC18F66K90
`101` = PIC18F85K90
`011` = PIC18F86K90

Devices with DEV<10:3> of `0101 0001`:
`000` = PIC18F67K90
`010` = PIC18F87K90

bit 4-0 **REV<4:0>:** Revision ID bits

These bits are used to indicate the device revision.

REGISTER 28-15: DEVID2: DEVICE ID REGISTER 2 FOR THE PIC18F87K90 FAMILY

R	R	R	R	R	R	R	R
DEV10(1)	DEV9(1)	DEV8(1)	DEV7(1)	DEV6(1)	DEV5(1)	DEV4(1)	DEV3(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **DEV<10:3>:** Device ID bits(1)

These bits are used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number.

`0101 0010` = PIC18F65K90, PIC18F66K90, PIC18F85K90 and PIC18F86K90
`0101 0001` = PIC18F67K90 and PIC18F87K90

Note 1: These values for DEV<10:3> may be shared with other devices. The specific device is always identified by using the entire DEV<10:0> bit sequence.

RETURN — Return from Subroutine

Syntax:	RETURN {s}
Operands:	s ∈ [0,1]
Operation:	(TOS) → PC; if s = `1`, (WS) → W, (STATUSS) → STATUS, (BSRS) → BSR, PCLATU, PCLATH are unchanged
Status Affected:	None
Encoding:	`0000` `0000` `0001` `001s`
Description:	Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the Program Counter. If ‘s’= `1`, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers W, STATUS and BSR. If ‘s’ = `0`, no update of these registers occurs.
Words:	1
Cycles:	2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	POP PC from stack
No operation	No operation	No operation	No operation

Example: `RETURN`

After Instruction:
PC = TOS

RLCF — Rotate Left f through Carry

Syntax:	RLCF f {,d {,a}}
Operands:	0 ≤ f ≤ 255 d ∈ [`0`,`1`] a ∈ [`0`,`1`]
Operation:	(f<n>) → dest<n + 1>, (f<7>) → C, (C) → dest<0>
Status Affected:	C, N, Z
Encoding:	`0011` `01da` `ffff` `ffff`
Description:	The contents of register ‘f’ are rotated one bit to the left through the Carry flag. If ‘d’ is ‘`0`’, the result is placed in W. If ‘d’ is ‘`1`’, the result is stored back in register ‘f’. If ‘a’ is ‘`0`’, the Access Bank is selected. If ‘a’ is ‘`1`’, the BSR is used to select the GPR bank. If ‘a’ is ‘`0`’ and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See **Section 29.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode”** for details.

Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ‘f’	Process Data	Write to destination

Example: `RLCF REG, 0, 0`

Before Instruction
```
REG  =  1110 0110
C    =  0
```
After Instruction
```
REG  =  1110 0110
W    =  1100 1100
C    =  1
```

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K90 Family (Industrial/Extended) (Continued)

PIC18F87K90 Family		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD) Cont.[2,3]						
	All devices	2.1	5.5	μA	-40°C	VDD = 1.8V[4] Regulator Disabled	FOSC = 31 kHz (**RC_IDLE** mode, LF-INTOSC)
		2.1	5.7	μA	+25°C		
		2.2	6.0	μA	+85°C		
		10	20	μA	+125°C		
	All devices	3.7	7.5	μA	-40°C	VDD = 3.3V[4] Regulator Disabled	
		3.9	7.8	μA	+25°C		
		3.9	8.5	μA	+85°C		
		12	24	μA	+125°C		
	All devices	70	180	μA	-40°C	VDD = 5V[5] Regulator Enabled	
		80	190	μA	+25°C		
		80	200	μA	+85°C		
		200	420	μA	+125°C		
	All devices	330	650	μA	-40°C	VDD = 1.8V[4] Regulator Disabled	FOSC = 1 MHz (**RC_IDLE** mode, HF-INTOSC)
		330	640	μA	+25°C		
		330	630	μA	+85°C		
		500	850	μA	+125°C		
	All devices	520	850	μA	-40°C	VDD = 3.3V[4] Regulator Disabled	
		520	900	μA	+25°C		
		520	850	μA	+85°C		
		800	1200	μA	+125°C		
	All devices	590	940	μA	-40°C	VDD = 5V[5] Regulator Enabled	
		600	960	μA	+25°C		
		620	990	μA	+85°C		
		1000	1400	μA	+125°C		
	All devices	470	770	μA	-40°C	VDD = 1.8V[4] Regulator Disabled	FOSC = 4 MHz (**RC_IDLE** mode, internal HF-INTOSC)
		470	770	μA	+25°C		
		460	760	μA	+85°C		
		700	1000	μA	+125°C		
	All devices	800	1400	μA	-40°C	VDD = 3.3V[4] Regulator Disabled	
		800	1350	μA	+25°C		
		790	1300	μA	+85°C		
		1100	1400	μA	+125°C		
	All devices	880	1600	μA	-40°C	VDD = 5V[5] Regulator Enabled	
		890	1700	μA	+25°C		
		910	1800	μA	+85°C		
		1200	2200	μA	+125°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
$\overline{\text{OSC1}}$ = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0).

6: LCD glass is not connected; resistor current is not included.

7: 48 MHz maximum frequency at 125°C.

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K90 Family (Industrial/Extended) (Continued)

PIC18F87K90 Family		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Supply Current (IDD) Cont.[2,3]						
	All devices	3.3	5.6	mA	-40°C	VDD = 3.3V[4] Regulator Disabled	FOSC = 16 MHz, (**PRI_RUN** mode, 4 MHz EC oscillator with PLL)
		3.3	5.5	mA	+25°C		
		3.3	5.5	mA	+85°C		
		3.6	6.0	mA	+125°C		
	All devices	3.5	5.9	mA	-40°C	VDD = 5V[5] Regulator Enabled	
		3.5	5.8	mA	+25°C		
		3.5	5.8	mA	+85°C		
		3.8	7.0	mA	+125°C		
	All devices	12	18	mA	-40°C	VDD = 3.3V[4] Regulator Disabled	FOSC = 64 MHz, (**PRI_RUN** mode, 16 MHz EC oscillator with PLL)
		12	18	mA	+25°C		
		12	18	mA	+85°C		
		13	22	mA	+125°C[7]		
	All devices	13	20	mA	-40°C	VDD = 5V[5] Regulator Enabled	
		13	20	mA	+25°C		
		13	20	mA	+85°C		
		14	24	mA	+125°C[7]		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0).

6: LCD glass is not connected; resistor current is not included.

7: 48 MHz maximum frequency at 125°C.