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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f66k90-e-pt

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5.0 RESET

The PIC18F87K90 family of devices differentiates between various kinds of Reset:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during power-managed modes
- d) Watchdog Timer (WDT) Reset (during execution)
- e) Configuration Mismatch (CM) Reset
- f) Brown-out Reset (BOR)
- g) RESET Instruction
- h) Stack Full Reset
- i) Stack Underflow Reset

This section discusses Resets generated by MCLR, POR and BOR, and covers the operation of the various start-up timers. Stack Reset events are covered in Section 6.1.3.4 "Stack Full and Underflow Resets". WDT Resets are covered in Section 28.2 "Watchdog Timer (WDT)". A simplified block diagram of the on-chip Reset circuit is shown in Figure 5-1.

5.1 RCON Register

Device Reset events are tracked through the RCON register (Register 5-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be set by the event and must be cleared by the application after the event.

The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 5.7** "**Reset State of Registers**".

The RCON register also has a control bit for setting interrupt priority (IPEN). Interrupt priority is discussed in **Section 10.0 "Interrupts"**.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:	
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75	
PIR5	TMR7GIF ⁽¹⁾	TMR12IF ⁽¹⁾	TMR10IF ⁽¹⁾	TMR8IF	TMR7IF ⁽¹⁾	TMR6IF	TMR5IF	TMR4IF	77	
PIE5	TMR7GIE ⁽¹⁾	TMR12IE ⁽¹⁾	TMR10IE ⁽¹⁾	TMR8IE	TMR7IE ⁽¹⁾	TMR6IE	TMR5IE	TMR4IE	77	
PIR2	OSCFIF	_	SSP2IF	BCL2IF	BCL1IF	HLVDIF	TMR3IF	TMR3GIF	77	
PIE2	OSCFIE	_	SSP2IE	BCL2IE	BCL1IE	HLVDIE	TMR3IE	TMR3GIE	77	
PIR3	TMR5GIF ⁽¹⁾	LCDIF	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	RTCCIF	77	
PIE3	TMR5GIE ⁽¹⁾	LCDIE	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE	77	
TMR3H	Timer3 Regi	ster High Byt	e						77	
TMR3L	Timer3 Register Low Byte									
T3GCON	TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/ T3DONE	T3GVAL	T3GSS1	T3GSS0	77	
T3CON	TMR3CS1	TMR3CS0	T3CKPS1	T3CKPS0	SOSCEN	T3SYNC	RD16	TMR3ON	77	
TMR5H	Timer5 Register High Byte									
TMR5L	Timer5 Register Low Byte									
T5GCON	TMR5GE	T5GPOL	T5GTM	T5GSPM	T5GGO/ T5DONE	T5GVAL	T5GSS1	T5GSS0	82	
T5CON	TMR5CS1	TMR5CS0	T5CKPS1	T5CKPS0	SOSCEN	T5SYNC	RD16	TMR5ON	82	
TMR7H ⁽¹⁾	Timer7 Regi	ster High Byt	e						81	
TMR7L ⁽¹⁾	Timer7 Regi	ster Low Byte	e						81	
T7GCON ⁽¹⁾	TMR7GE	T7GPOL	T7GTM	T7GSPM	T7GGO/ T7DONE	T7GVAL	T7GSS1	T7GSS0	81	
T7CON ⁽¹⁾	TMR7CS1	TMR7CS0	T7CKPS1	T7CKPS0	SOSCEN	T7SYNC	RD16	TMR7ON	81	
OSCCON2	_	SOSCRUN	_	_	SOSCGO	_	MFIOFS	MFIOSEL	79	
CCPTMRS0	C3TSEL1	C3TSEL0	C2TSEL2	C2TSEL1	C2TSEL0	C1TSEL2	C1TSEL1	C1TSEL0	81	
CCPTMRS1	C7TSEL1	C7TSEL0	—	C6TSEL0	—	C5TSEL0	C4TSEL1	C4TSEL0	81	
CCPTMRS1	_	_	_	C10TSEL0	_	C9TSEL0	C8TSEL1	C8TSEL0	81	

TABLE 15-5:	REGISTERS ASSOCIATED WITH TIMER3/5/7 AS A TIMER/COUNTER

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Timer3/5/7 modules.

Note 1: Unimplemented in devices with a program memory of 32 Kbytes (PIC18FX5K90).

The outputs of TMRx (before the postscaler) are used

only as a PWM time base for the ECCP modules. They

are not used as baud rate clocks for the MSSP

Output of TMRx

modules as is the Timer2 output.

16.2 Timer4/6/8/10/12 Interrupt

The Timer4/6/8/10/12 modules have 8-bit Period registers, PRx, that are both readable and writable. Timer4/6/8/10/12 increment from 00h until they match PR4/6/8/10/12 and then reset to 00h on the next increment cycle. The PRx registers are initialized to FFh upon Reset.

FIGURE 16-1: TIMER4/6/8/10/12 BLOCK DIAGRAM



16.3

TABLE 16-3: REGISTERS ASSOCIATED WITH TIMER4/6/8/10/12 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:		
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	75		
IPR5	TMR7GIP ⁽¹⁾	TMR12IP ⁽¹⁾	TMR10IP ⁽¹⁾	TMR8IP	TMR7IP ⁽¹⁾	TMR6IP	TMR5IP	TMR4IP	76		
PIR5	TMR7GIF ⁽¹⁾	TMR12IF ⁽¹⁾	TMR10IF ⁽¹⁾	TMR8IF	TMR7IF ⁽¹⁾	TMR6IF	TMR5IF	TMR4IF	77		
PIE5	TMR7GIE ⁽¹⁾	TMR12IE ⁽¹⁾	TMR10IE ⁽¹⁾	TMR8IE	TMR7IE ⁽¹⁾	TMR6IE	TMR5IE	TMR4IE	77		
TMR4	Timer4 Register										
T4CON	_	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	82		
PR4	Timer4 Period	d Register							82		
TMR6	Timer6 Register										
T6CON	_	T6OUTPS3	T6OUTPS2	T6OUTPS1	T6OUTPS0	TMR6ON	T6CKPS1	T6CKPS0	81		
PR6	Timer6 Period Register										
TMR8	Timer8 Register										
T8CON		T8OUTPS3	T8OUTPS2	T8OUTPS1	T8OUTPS0	TMR8ON	T8CKPS1	T8CKPS0	81		
PR8	Timer8 Period	d Register							81		
TMR10	Timer10 Regi	ster							81		
T10CON	_	T10OUTPS3	T10OUTPS2	T10OUTPS1	T10OUTPS0	TMR100N	T10CKPS1	T10CKPS0	81		
PR10	Timer10 Perio	od Register							81		
TMR12	Timer12 Regi	ster							81		
T12CON	_	T12OUTPS3	T12OUTPS2	T12OUTPS1	T12OUTPS0	TMR12ON	T12CKPS1	T12CKPS0	81		
PR12	Timer12 Perio	od Register							81		
CCPTMRS0	C3TSEL1	C3TSEL0	C2TSEL2	C2TSEL1	C2TSEL0	C1TSEL2	C1TSEL1	C1TSEL0	81		
CCPTMRS1	C7TSEL1	C7TSEL0	_	C6TSEL0	_	C5TSEL0	C4TSEL1	C4TSEL0	81		
CCPTMRS2	_	_	_	C10TSEL0 ⁽¹⁾	_	C9TSEL0 ⁽¹⁾	C8TSEL1	C8TSEL0	81		

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Timer4/6/8/10/12 module.

Note 1: Unimplemented in devices with a program memory of 32 Kbytes (PIC18FX5K22).

17.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

The key features of the Real-Time Clock and Calendar (RTCC) module are:

- Time: hours, minutes and seconds
- Twenty-four hour format (military time)
- Calendar: weekday, date, month and year
- · Alarm configurable
- Year range: 2000 to 2099
- · Leap year correction
- · BCD format for compact firmware
- Optimized for low-power operation
- · User calibration with auto-adjust
- Calibration range: ±2.64 seconds error per month
- Requirements: external 32.768 kHz clock crystal
- · Alarm pulse or seconds clock output on RTCC pin

The RTCC module is intended for applications where accurate time must be maintained for an extended period with minimum to no intervention from the CPU. The module is optimized for low-power usage in order to provide extended battery life while keeping track of time.

The module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

Hours are measured in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.



FIGURE 17-1: RTCC BLOCK DIAGRAM

17.6 Register Maps

Table 17-5, Table 17-6 and Table 17-7 summarize the registers associated with the RTCC module.

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets on Page:
RTCCFG	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTR1	RTCPTR0	80
RTCCAL	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	80
PADCFG1	RDPU	REPU	RJPU ⁽¹⁾	_	-	RTSECSEL1	RTSECSEL0	_	80
ALRMCFG	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	80
ALRMRPT	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	80

TABLE 17-5:RTCC CONTROL REGISTERS

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for 80-pin devices.

Note 1: Not available on 64-pin devices.

TABLE 17-6: RTCC VALUE REGISTERS

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets on Page:	
RTCVALH	RTCC Value High Register Window Based on RTCPTR<1:0>									
RTCVALL	RTCC Value Low Register Window Based on RTCPTR<1:0>									

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for 80-pin devices.

TABLE 17-7: ALARM VALUE REGISTERS

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets on Page:	
ALRMVALH	Alarm Value High Register Window Based on ALRMPTR<1:0>									
ALRMVALL	Alarm Value Low Register Window Based on ALRMPTR<1:0>									

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for 80-pin devices.

In addition to the expanded range of modes available through the CCPxCON and ECCPxAS registers, the ECCP modules have two additional registers associated with Enhanced PWM operation and auto-shutdown features. They are:

- ECCPxDEL Enhanced PWM Control
- PSTRxCON Pulse Steering Control

19.1 ECCP Outputs and Configuration

The Enhanced CCP module may have up to four PWM outputs, depending on the selected operating mode. The CCPxCON register is modified to allow control over four PWM outputs: ECCPx/PxA, PxB, PxC and PxD. Applications can use one, two or four of these outputs.

The outputs that are active depend on the selected ECCP operating mode. The pin assignments are summarized in Table 19-3.

To configure the I/O pins as PWM outputs, the proper PWM mode must be selected by setting the PxM<1:0> and CCPxM<3:0> bits. The appropriate TRIS direction bits for the PORT pins must also be set as outputs.

19.1.1 ECCP MODULE AND TIMER RESOURCES

The ECCP modules use Timers, 1, 2, 3, 4, 6, 8, 10 or 12, depending on the mode selected. These timers are available to CCP modules in Capture, Compare or PWM modes, as shown in Table 19-1.

TABLE 19-1: ECCP MODE – TIMER RESOURCE

ECCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2, Timer4, Timer6, Timer8, Timer10 or Timer12

The assignment of a particular timer to a module is determined by the timer to ECCP enable bits in the CCPTMRSx register (Register 19-2). The interactions between the two modules are depicted in Figure 19-1. Capture operations are designed to be used when the timer is configured for Synchronous Counter mode. Capture operations may not work as expected if the associated timer is configured for Asynchronous Counter mode.

19.1.2 ECCP PIN ASSIGNMENT

The pin assignment for ECCPx (capture input, compare and PWM output) can change, based on device configuration. The ECCPMX (CONFIG3H<1>) Configuration bit determines which pins, ECCP1 and ECCP3, are multiplexed to.

- Default/ECCPMX = 1:
 - ECCP1 (P1B/P1C) is multiplexed onto RE6 and RE5
 - ECCP3 (P3B/P3C) is multiplexed onto RE4 and RE3
- ECCPMX = 0:
 - ECCP1 (P1B/P1C) is multiplexed onto RH7 and RH6
 - ECCP3 (P3B/P3C) is multiplexed onto RH5 and RH4.

The pin assignment for ECCP2 (capture input, compare and PWM output) can change, based on device configuration.

The CCP2MX Configuration bit (CONFIG3H<0>) determines which pin, ECCP2, is multiplexed to.

- If CCP2MX = 1 (default) ECCP2 is multiplexed to RC1
- If CCP2MX = 0 ECCP2 is multiplexed to:
- RE7 is the ECCP2 pin with CCP2MX = 0



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FIGURE 21-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)





REGISTER 2	21-6: SSPx	CON2: MSSI	YX CONTRO	L REGISTER	2 (I ² C™ SLA	VE MODE)				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
GCEN	ACKSTAT	ADMSK5	ADMSK4	ADMSK3	ADMSK2	ADMSK1	SEN ⁽¹⁾			
bit 7							bit 0			
Legend:										
R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'										
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own			
bit 7	GCEN: Gene	ral Call Enable	bit							
1 = Enables interrupt when a general call address (0000h) is received in the SSPxSR										
	0 = General call address is disabled									
bit 6	ACKSTAT: A	cknowledge Sta	atus bit							
	Unused in Sla	ave mode.								
bit 5-2	ADMSK<5:2>	Slave Addres	ss Mask Selec	ct bits (5-Bit Add	ress Masking i	mode)				
	1 = Masking o 0 = Masking o	of correspondir of correspondir	ig bits of SSP ig bits of SSP	ADD is enabled ADD is disable	d d					
bit 1	ADMSK1: Sla	ave Address Le	ast Significan	t bit(s) Mask Se	lect bit					
	In 7-Bit Addre	essing mode:								
	1 = Masking o	of SSPxADD<1	> only is enab	bled						
	0 = Masking o	of SSPxADD<1	> only is disal	bled						
	In 10-Bit Addr	ressing mode:	102 is enabled	4						
	1 = Masking 0 0 = Masking 0	of SSPxADD<1	:0> is disable	d						
bit 0	SEN: Stretch	Enable bit ⁽¹⁾		-						
	1 = Clock stre	etching is enabl	ed for both sla	ave transmit and	I slave receive	(stretch enable	d)			
	0 = Clock stre	etching is disab	led							

Note 1: If the I²C module is active, this bit may not be set (no spooling) and the SSPxBUF may not be written to (or writes to the SSPxBUF are disabled).

REGISTER 21-7: SSPxMSK: I ⁺ C [™] SLAVE ADDRESS MASK REGISTER (7-BIT MASKING MODE) ^V	EGISTER 21-7:
---	---------------

| R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|---------------------|
| MSK7 | MSK6 | MSK5 | MSK4 | MSK3 | MSK2 | MSK1 | MSK0 ⁽²⁾ |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 MSK<7:0>: Slave Address Mask Select bit

1 = Masking of the corresponding bit of SSPxADD is enabled

0 = Masking of the corresponding bit of SSPxADD is disabled

Note 1: This register shares the same SFR address as SSPxADD and is only addressable in select MSSPx operating modes. See Section 21.4.3.4 "7-Bit Address Masking Mode" for more details.

2: MSK0 is not used as a mask bit in 7-bit addressing.



				SYNC = 0, BRGH = 0, BRG16 = 0								
BAUD	Fosc = 40.000 MHz			Fosc = 20.000 MHz		Fosc = 10.000 MHz			Fosc = 8.000 MHz			
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	_								_		_	
1.2	—	—	—	1.221	1.73	255	1.202	0.16	129	1.201	-0.16	103
2.4	2.441	1.73	255	2.404	0.16	129	2.404	0.16	64	2.403	-0.16	51
9.6	9.615	0.16	64	9.766	1.73	31	9.766	1.73	15	9.615	-0.16	12
19.2	19.531	1.73	31	19.531	1.73	15	19.531	1.73	7	_	_	_
57.6	56.818	-1.36	10	62.500	8.51	4	52.083	-9.58	2	—	_	_
115.2	125.000	8.51	4	104.167	-9.58	2	78.125	-32.18	1	_	_	_

TABLE 22-3	BAUD RATES	FOR ASYNCHRON	OUS MODES
IADLL 22-J.			

		SYNC = 0, BRGH = 0, BRG16 = 0										
BAUD RATE (K)	Fosc = 4.000 MHz			Fos	c = 2.000	MHz	Fosc = 1.000 MHz					
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)			
0.3	0.300	0.16	207	0.300	-0.16	103	0.300	-0.16	51			
1.2	1.202	0.16	51	1.201	-0.16	25	1.201	-0.16	12			
2.4	2.404	0.16	25	2.403	-0.16	12	—	—	—			
9.6	8.929	-6.99	6	—	_	_	—	_	_			
19.2	20.833	8.51	2	—	_	_	—	_	_			
57.6	62.500	8.51	0	—	_	_	—	_	_			
115.2	62.500	-45.75	0		—		_	—	—			

					SYNC = 0, BRGH = 1, BRG16 = 0							
BAUD	Fosc = 40.000 MHz			Fosc	Fosc = 20.000 MHz		Fosc = 10.000 MHz			Fosc = 8.000 MHz		
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	_	_	_	_	_	_	_	_	_	_	_	_
1.2	—	—	—	—	—	—	—	—	—	—	—	—
2.4	—	—	—	—	—	—	2.441	1.73	255	2.403	-0.16	207
9.6	9.766	1.73	255	9.615	0.16	129	9.615	0.16	64	9.615	-0.16	51
19.2	19.231	0.16	129	19.231	0.16	64	19.531	1.73	31	19.230	-0.16	25
57.6	58.140	0.94	42	56.818	-1.36	21	56.818	-1.36	10	55.555	3.55	8
115.2	113.636	-1.36	21	113.636	-1.36	10	125.000	8.51	4	—	_	_

		SYNC = 0, BRGH = 1, BRG16 = 0									
BAUD	Fosc = 4.000 MHz			Fos	c = 2.000	MHz	Fosc = 1.000 MHz				
(K)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)		
0.3		_	_	_	_	_	0.300	-0.16	207		
1.2	1.202	0.16	207	1.201	-0.16	103	1.201	-0.16	51		
2.4	2.404	0.16	103	2.403	-0.16	51	2.403	-0.16	25		
9.6	9.615	0.16	25	9.615	-0.16	12	_	_	_		
19.2	19.231	0.16	12	_	_	_	_	_	_		
57.6	62.500	8.51	3	—	_	_	—	_	_		
115.2	125.000	8.51	1	—	—	—	—	—	_		

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24.5 Comparator Control and Configuration

Each comparator has up to eight possible combinations of inputs: up to four external analog inputs and one of two internal voltage references.

All of the comparators allow a selection of the signal from pin, CxINA, or the voltage from the Comparator Voltage Reference (CVREF) on the non-inverting channel. This is compared to either CxINB, CxINC, C2INB/C2IND or the microcontroller's fixed internal reference voltage (VBG, 1.024V nominal) on the inverting channel. The comparator inputs and outputs are tied to fixed I/O pins, defined in Table 24-1. The available comparator configurations and their corresponding bit settings are shown in Figure 24-4.

TABLE 24-1:	COMPARATOR INPUTS AND
	OUTPUTS

Comparator	Input or Output	I/O Pin
	C1INA (VIN+)	RF6
	C1INB (VIN-)	RF5
1	C1INC ⁽¹⁾ (VIN-)	RH6
	C2INB (VIN-)	RF3
	C1OUT	RF2
	C2INA (VIN+)	RF4
	C2INB (VIN-)	RF3
2	C2INC ⁽¹⁾ (VIN-)	RH4
	C2IND ⁽¹⁾ (VIN-)	RH5
	C2OUT	RF1
	C3INA (VIN+)	RG2
	C3INB (VIN-)	RG3
3	C3INC (VIN-)	RG4
	C2INB (VIN-)	RF3
	C3OUT	RG1

Note 1: C1INC, C2INC and C2IND are all unavailable for 64-pin devices (PIC18F6XK90).

24.5.1 COMPARATOR ENABLE AND INPUT SELECTION

Setting the CON bit of the CMxCON register (CMxCON<7>) enables the comparator for operation. Clearing the CON bit disables the comparator, resulting in minimum current consumption.

The CCH<1:0> bits in the CMxCON register (CMxCON<1:0>) direct either one of three analog input pins, or the Internal Reference Voltage (VBG), to the comparator, VIN-. Depending on the comparator

operating mode, either an external or internal voltage reference may be used. For external analog pins that are unavailable in 64-pin devices (C1INC, C2INC and C2IND), the corresponding configurations that use them as inputs are unavailable.

The analog signal present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is adjusted accordingly.

The external reference is used when CREF = 0 (CMxCON<2>) and VIN+ is connected to the CxINA pin. When external voltage references are used, the comparator module can be configured to have the reference sources externally. The reference signal must be between Vss and VDD, and can be applied to either pin of the comparator.

The comparator module also allows the selection of an internally generated voltage reference from the Comparator Voltage Reference (CVREF) module. This module is described in more detail in **Section 25.0 "Comparator Voltage Reference Module**". The reference from the comparator voltage reference module is only available when CREF = 1. In this mode, the internal voltage reference is applied to the comparator's VIN+ pin.

Note:	The comparator input pin, selected by
	CCH<1:0>, must be configured as an input
	by setting both the corresponding TRISF,
	TRISG or TRISH bit and the corresponding
	ANSELx bit in the ANCONx register.

24.5.2 COMPARATOR ENABLE AND OUTPUT SELECTION

The comparator outputs are read through the CMSTAT register. The CMSTAT<5> bit reads the Comparator 1 output, CMSTAT<6> reads Comparator 2 output and CMSTAT<7> reads Comparator 3 output. These bits are read-only.

The comparator outputs may also be directly output to the RF2, RF1 and RG1 I/O pins by setting the COE bit (CMxCON<6>). When enabled, multiplexers in the output path of the pins switch to the output of the comparator. While in this mode, the TRISF<2:1> and TRISG<1> bits still function as the digital output enable bits for the RF2, RF1 and RG1 pins.

By default, the comparator's output is at logic high whenever the voltage on VIN+ is greater than on VIN-. The polarity of the comparator outputs can be inverted using the CPOL bit (CMxCON<5>).

The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications, as discussed in **Section 24.2 "Comparator Operation"**.

26.2 HLVD Setup

To set up the HLVD module:

- 1. Select the desired HLVD trip point by writing the value to the HLVDL<3:0> bits.
- Set the VDIRMAG bit to detect high voltage (VDIRMAG = 1) or low voltage (VDIRMAG = 0).
- 3. Enable the HLVD module by setting the HLVDEN bit.
- 4. Clear the HLVD interrupt flag (PIR2<2>), which may have been set from a previous interrupt.
- If interrupts are desired, enable the HLVD interrupt by setting the HLVDIE and GIE bits (PIE2<2> and INTCON<7>, respectively).

An interrupt will not be generated until the IRVST bit is set.

Note: Before changing any module settings (VDIRMAG, HLVDL<3:0>), first disable the module (HLVDEN = 0), make the changes and re-enable the module. This prevents the generation of false HLVD events.

26.3 Current Consumption

When the module is enabled, the HLVD comparator and voltage divider are enabled and consume static current. The total current consumption, when enabled, is specified in electrical specification Parameter D022B (Table 31-10). Depending on the application, the HLVD module does not need to operate constantly. To reduce current requirements, the HLVD circuitry may only need to be enabled for short periods where the voltage is checked. After such a check, the module could be disabled.

26.4 HLVD Start-up Time

The internal reference voltage of the HLVD module, specified in electrical specification Parameter 37 (Section 31.0 "Electrical Characteristics"), may be used by other internal circuitry, such as the programmable Brown-out Reset. If the HLVD or other circuits using the voltage reference are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification Parameter 36 (Table 31-10).

The HLVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval (see Figure 26-2 or Figure 26-3).





27.2 CTMU Operation

The CTMU works by using a fixed current source to charge a circuit. The type of circuit depends on the type of measurement being made.

In the case of charge measurement, the current is fixed and the amount of time the current is applied to the circuit is fixed. The amount of voltage read by the A/D becomes a measurement of the circuit's capacitance.

In the case of time measurement, the current, as well as the capacitance of the circuit, is fixed. In this case, the voltage read by the A/D is representative of the amount of time elapsed from the time the current source starts and stops charging the circuit.

If the CTMU is being used as a time delay, both capacitance and current source are fixed, as well as the voltage supplied to the comparator circuit. The delay of a signal is determined by the amount of time it takes the voltage to charge to the comparator threshold voltage.

27.2.1 THEORY OF OPERATION

The operation of the CTMU is based on the equation for charge:

 $C = I \bullet \frac{dV}{dT}$

More simply, the amount of charge measured in coulombs in a circuit is defined as current in amperes (I) multiplied by the amount of time in seconds that the current flows (t). Charge is also defined as the capacitance in farads (C) multiplied by the voltage of the circuit (V). It follows that:

 $I \bullet t = C \bullet V$

The CTMU module provides a constant, known current source. The A/D Converter is used to measure (V) in the equation, leaving two unknowns: capacitance (C) and time (t). The above equation can be used to calculate capacitance or time, by either the relationship using the known fixed capacitance of the circuit:

 $t = (C \bullet V)/I$

or by:

 $\mathbf{C} = (\mathbf{I} \bullet \mathbf{t}) / \mathbf{V}$

using a fixed time that the current source is applied to the circuit.

27.2.2 CURRENT SOURCE

At the heart of the CTMU is a precision current source, designed to provide a constant reference for measurements. The level of current is user-selectable across three ranges or a total of two orders of magnitude, with the ability to trim the output in $\pm 2\%$ increments (nominal). The current range is selected by the IRNG<1:0> bits (CTMUICON<1:0>), with a value of '00' representing the lowest range.

Current trim is provided by the ITRIM<5:0> bits (CTMUICON<7:2>). These six bits allow trimming of the current source in steps of approximately 2% per step. Half of the range adjusts the current source positively and the other half reduces the current source. A value of '000000' is the neutral position (no change). A value of '100000' is the maximum negative adjustment (approximately -62%) and '011111' is the maximum positive adjustment (approximately +62%).

27.2.3 EDGE SELECTION AND CONTROL

CTMU measurements are controlled by edge events occurring on the module's two input channels. Each channel, referred to as Edge 1 and Edge 2, can be configured to receive input pulses from one of the edge input pins (CTED1 and CTED2) or CCPx Special Event Triggers. The input channels are level-sensitive, responding to the instantaneous level on the channel rather than a transition between levels. The inputs are selected using the EDG1SEL and EDG2SEL bit pairs (CTMUCONL<3:2, 6:5>).

In addition to source, each channel can be configured for event polarity using the EDGE2POL and EDGE1POL bits (CTMUCONL<7,4>). The input channels can also be filtered for an edge event sequence (Edge 1 occurring before Edge 2) by setting the EDGSEQEN bit (CTMUCONH<2>).

27.2.4 EDGE STATUS

The CTMUCON register also contains two status bits, EDG2STAT and EDG1STAT (CTMUCONL<1:0>). Their primary function is to show if an edge response has occurred on the corresponding channel. The CTMU automatically sets a particular bit when an edge response is detected on its channel. The level-sensitive nature of the input channels also means that the status bits become set immediately if the channel's configuration is changed and matches the channel's current state.

The module uses the edge status bits to control the current source output to external analog modules (such as the A/D Converter). Current is only supplied to external modules when only one (not both) of the status bits is set. Current is shut off when both bits are either set or cleared. This allows the CTMU to measure current only during the interval between edges. After both status bits are set, it is necessary to clear them before another measurement is taken. Both bits should be cleared simultaneously, if possible, to avoid re-enabling the CTMU current source.

In addition to being set by the CTMU hardware, the edge status bits can also be set by software. This permits a user application to manually enable or disable the current source. Setting either (but not both) of the bits enables the current source. Setting or clearing both bits at once disables the source.

27.8 Measuring Temperature Using the CTMU Module

The CTMU, along with an internal diode, can be used to measure the temperature. The ADC can be connected to the internal diode and the CTMU module can

source the current to the diode. The ADC reading will reflect the temperature. With the increase, the ADC readings will go low. This can be used for low-cost temperature measurement applications.

EXAMPLE 27-5: ROUTINE FOR TEMPERATURE MEASUREMENT USING INTERNAL DIODE

//Initialize CTMU CTMUICON=0x03; CTMUCONHbits.CTMUEN=1; CTMUCONLbits.EDGISTAT=1; //Initialize ADC ADCON0=0xE5; //ADCON and connect to Internal diode ADCON1=0; ADCON2=0xBE; //Right justified ADCON0bits.GO=1; while(ADCON0bits.GO=1); Temp=ADRES; ;//read ADC results (inversely proportional to temperature)

Note: The temperature diode is not calibrated; the user will have to calibrate the diode to their application.

28.0 SPECIAL FEATURES OF THE CPU

The PIC18F87K90 family of devices includes several features intended to maximize reliability and minimize cost through elimination of external components. These include:

- Oscillator Selection
- Resets:
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT) and On-Chip Regulator
- · Fail-Safe Clock Monitor
- Two-Speed Start-up
- Code Protection
- ID Locations
- In-Circuit Serial Programming[™] (ICSP[™])

The oscillator can be configured for the application depending on frequency, power, accuracy and cost. All of the options are discussed in detail in **Section 3.0 "Oscillator Configurations"**.

A complete discussion of device Resets and interrupts is available in previous sections of this data sheet.

In addition to their Power-up and Oscillator Start-up Timers provided for Resets, the PIC18F87K90 family of devices has a Watchdog Timer, which is either permanently enabled via the Configuration bits or software controlled (if configured as disabled).

The inclusion of an internal RC (LF-INTOSC) oscillator also provides the additional benefits of a Fail-Safe Clock Monitor (FSCM) and Two-Speed Start-up. FSCM provides for background monitoring of the peripheral clock and automatic switchover in the event of its failure. Two-Speed Start-up enables code to be executed almost immediately on start-up, while the primary clock source completes its start-up delays.

All of these features are enabled and configured by setting the appropriate Configuration register bits.

28.1 Configuration Bits

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped starting at program memory location, 300000h.

The user will note that address, 300000h, is beyond the user program memory space. In fact, it belongs to the configuration memory space (300000h-3FFFFFh), which can only be accessed using table reads and table writes.

Software programming the Configuration registers is done in a manner similar to programming the Flash memory. The WR bit in the EECON1 register starts a self-timed write to the Configuration register. In normal operation mode, a TBLWT instruction, with the TBLPTR pointing to the Configuration register, sets up the address and the data for the Configuration register write. Setting the WR bit starts a long write to the Configuration register. The Configuration registers are written a byte at a time. To write or erase a configuration cell, a TBLWT instruction can write a '1' or a '0' into the cell. For additional details on Flash programming, refer to Section 7.5 "Writing to Flash Program Memory".

28.5 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the microcontroller to continue operation in the event of an external oscillator failure by automatically switching the device clock to the internal oscillator block. The FSCM function is enabled by setting the FCMEN Configuration bit.

When FSCM is enabled, the LF-INTOSC oscillator runs at all times to monitor clocks to peripherals and provide a backup clock in the event of a clock failure. Clock monitoring (shown in Figure 28-4) is accomplished by creating a sample clock signal, which is the output from the LF-INTOSC, divided by 64. This allows ample time between FSCM sample clocks for a peripheral clock edge to occur. The peripheral device clock and the sample clock are presented as inputs to the Clock Monitor (CM) latch. The CM is set on the falling edge of the device clock source, but cleared on the rising edge of the sample clock.



Clock failure is tested for on the falling edge of the sample clock. If a sample clock falling edge occurs while CM is still set, a clock failure has been detected (Figure 28-5). This causes the following:

- The FSCM generates an oscillator fail interrupt by setting bit, OSCFIF (PIR2<7>)
- The device clock source switches to the internal oscillator block (OSCCON is not updated to show the current clock source – this is the Fail-Safe condition)
- The WDT is reset

During switchover, the postscaler frequency from the internal oscillator block may not be sufficiently stable for timing-sensitive applications. In these cases, it may be desirable to select another clock configuration and enter an alternate power-managed mode. This can be done to attempt a partial recovery or execute a controlled shutdown. See Section 4.1.4 "Multiple Sleep Commands" and Section 28.4.1 "Special Considerations for Using Two-Speed Start-up" for more details.

To use a higher clock speed on wake-up, the INTOSC or postscaler clock sources can be selected to provide a higher clock speed by setting bits, IRCF<2:0>, immediately after Reset. For wake-ups from Sleep, the INTOSC or postscaler clock sources can be selected by setting the IRCF<2:0> bits prior to entering Sleep mode.

The FSCM will detect only failures of the primary or secondary clock sources. If the internal oscillator block fails, no failure would be detected nor would any action be possible.

28.5.1 FSCM AND THE WATCHDOG TIMER

Both the FSCM and the WDT are clocked by the INTOSC oscillator. Since the WDT operates with a separate divider and counter, disabling the WDT has no effect on the operation of the INTOSC oscillator when the FSCM is enabled.

As already noted, the clock source is switched to the INTOSC clock when a clock failure is detected. Depending on the frequency selected by the IRCF<2:0> bits, this may mean a substantial change in the speed of code execution. If the WDT is enabled with a small prescale value, a decrease in clock speed allows a WDT time-out to occur and a subsequent device Reset. For this reason, Fail-Safe Clock events also reset the WDT and postscaler, allowing it to start timing from when execution speed was changed, and decreasing the likelihood of an erroneous time-out.

28.5.2 EXITING FAIL-SAFE OPERATION

The Fail-Safe condition is terminated by either a device Reset or by entering a power-managed mode. On Reset, the controller starts the primary clock source specified in Configuration Register 1H (with any required start-up delays that are required for the oscillator mode, such as the OST or PLL timer). The INTOSC multiplexer provides the device clock until the primary clock source becomes ready (similar to a Two-Speed Start-up). The clock source is then switched to the primary clock (indicated by the OSTS bit in the OSCCON register becoming set). The Fail-Safe Clock Monitor then resumes monitoring the peripheral clock.

The primary clock source may never become ready during start-up. In this case, operation is clocked by the INTOSC multiplexer. The OSCCON register will remain in its Reset state until a power-managed mode is entered.

LFSF	R	Load FSR								
Synta	ax:	LFSR f, k	LFSR f, k							
Oper	ands:	$\begin{array}{l} 0 \leq f \leq 2 \\ 0 \leq k \leq 409 \end{array}$	$\begin{array}{l} 0 \leq f \leq 2 \\ 0 \leq k \leq 4095 \end{array}$							
Oper	ation:	$k\toFSRf$								
Statu	s Affected:	None								
Enco	ding:	1110 1111	1110 0000	00ff k ₇ kkk	k ₁₁ kkk kkkk					
Desc	ription:	The 12-bit file select r	literal 'k' egister p	is loaded ointed to	into the by 'f'.					
Word	ls:	2								
Cycle	es:	2	2							
QC	ycle Activity:									
	Q1	Q2	Q3		Q4					
	Decode	Read literal 'k' MSB	Proce Data	ss a li	Write teral 'k' MSB to FSRfH					
	Decode	Read literal 'k' LSB	ead literal Process Write lite 'k' LSB Data 'k' to FSF							
<u>Exan</u>	nple: After Instructi FSR2H FSR2L	LFSR 2, on = 03 = AE	3ABh bh 3h							

MOVE	Move f						
Svotav:	MOVE f	d (a)]					
Operande:		,u (,ajj					
Operands:	$0 \le 1 \le 255$ $d \in [0, 1]$	$0 \le 1 \le 255$					
	$a \in [0, 1]$ $a \in [0, 1]$						
Operation:	$f \to dest$						
Status Affected:	N, Z						
Encoding:	0101	00da	ffff	ffff			
Description:	The conten a destination status of 'd placed in V placed bac can be any 256-byte bac	The contents of register 'f' are moved to a destination dependent upon the status of 'd'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f'. Location 'f' can be anywhere in the 256 byte bank					
	lf 'a' is '0', t If 'a' is '1', t GPR bank.	he Acces he BSR i	s Bank is used to	selected. select the			
	If 'a' is '0' a set is enab in Indexed mode wher Section 29 Bit-Oriente Literal Offs	nd the e> led, this in Literal Of never f ≤ 9 .2.3 "Byt ed Instru set Mode	Atended in Instruction Ifset Addre 95 (5Fh). Ate-Oriente Ctions in 9" for deta	struction operates essing See ed and Indexed ils.			
Words:	1						
Cycles:	1						
Q Cycle Activity:							
Q1	Q2	Q3		Q4			
Decode	ReadProcessWriteregister 'f'DataW						
Example:	MOVF R	EG, 0,	0				
Before Instruction REG = 22h W = FFh							
REG W	= 22 = 22	h h					

NOTES:

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Type-A in 1/4 MUX, 1/3 Bias Drive	
Type-A/Type-B in Static Drive	
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Type-B in 1/2 MUX, 1/3 Bias Drive	
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