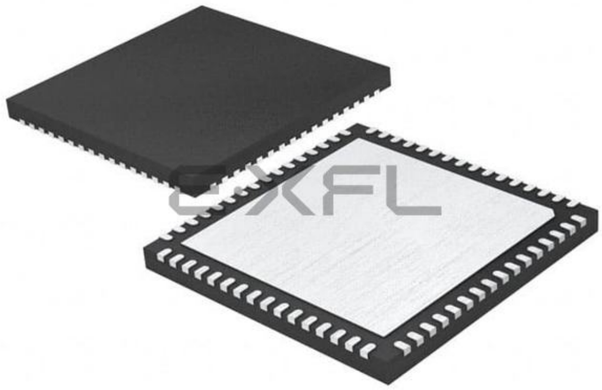

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f66k90-i-mrrsl

The PIC18F87K90 family is also largely pin-compatible with other PIC18 families, such as the PIC18F8720, PIC18F8722, PIC18F85J11, PIC18F8490, PIC18F85J90, PIC18F87J90 and PIC18F87J93 families of microcontrollers with LCD drivers. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining a similar feature set.

1.2 LCD Driver

The on-chip LCD driver includes many features that ease the integration of displays in low-power applications. These include an integrated internal resistor ladder, so bias voltages can be generated internally. This enables software-controlled contrast control and eliminates the need for external bias voltage resistors.

1.3 Other Special Features

- **Communications:** The PIC18F87K90 family incorporates a range of serial communication peripherals including two Enhanced USART, that support LIN/J2602, and two Master SSP modules capable of both SPI and I^2C™ (Master and Slave) modes of operation.
- **CCP Modules:** PIC18F87K90 family devices incorporate up to seven or five Capture/ Compare/PWM (CCP) modules. Up to six different time bases can be used to perform several different operations at once.
- **ECCP Modules:** The PIC18F87K90 family has three Enhanced CCP (ECCP) modules to maximize flexibility in control applications:
  - Up to eight different time bases for performing several different operations at once
  - Up to four PWM outputs for each module, for a total of 12 PWMs
  - Other beneficial features, such as polarity selection, programmable dead time, auto-shutdown and restart, and Half-Bridge and Full-Bridge Output modes
- **12-Bit A/D Converter:** The PIC18F87K90 family has differential ADC. It incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and thus, reducing code overhead.
- **Charge Time Measurement Unit (CTMU):** The CTMU is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation.

  Together with other on-chip analog modules, the CTMU can precisely measure time, measure capacitance or relative changes in capacitance, or generate output pulses that are independent of the system clock.
- **LP Watchdog Timer (WDT):** This enhanced version incorporates a 22-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 31.0 "Electrical Characteristics"** for time-out periods.
- **Real-Time Clock and Calendar Module (RTCC):** The RTCC module is intended for applications requiring that accurate time be maintained for extended periods of time with minimum to no intervention from the CPU.

  The module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

1.4 Details on Individual Family Members

Devices in the PIC18F87K90 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in these ways:

- Flash Program Memory:
  - PIC18FX5K90 (PIC18F65K90 and PIC18F85K90) – 32 Kbytes
  - PIC18FX6K90 (PIC18F66K90 and PIC18F86K90) – 64 Kbytes
  - PIC18FX7K90 (PIC18F67K90 and PIC18F87K90) – 128 Kbytes
- Data RAM:
  - All devices except PIC18FX5K90 – 4 Kbytes
  - PIC18FX5K90 – 2 Kbytes
- I/O Ports:
  - PIC18F6XK90 (64-pin devices) – 7 bidirectional ports
  - PIC18F8XK90 (80-pin devices) – 9 bidirectional ports
- LCD Pixels:
  - PIC18F6XK90 – 132 pixels (33 SEGs x 4 COMs)
  - PIC18F8XK90 – 192 pixels (48 SEGs x 4 COMs)
- CCP Module:
  - All devices except PIC18FX5K90 have seven CCP modules, PIC18FX5K90 has only five CCP modules
- Timers:
  - All devices except 18FX5K90 have six 8-bit timers and five 16-bit timers, PIC18FX5K90 has only four 8-bit timers and four 16-bit timers.
- A/D Channels:
  - All PIC18F8XK90 devices have 24 A/D channels, all PIC18F6XK90 devices have 16 A/D channels

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

TABLE 1-4: PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
				PORTH is a bidirectional I/O port.
RH0/SEG47/AN23	79			
RH0		I/O	ST	Digital I/O.
SEG47		O	Analog	SEG47 output for LCD.
AN23		I	Analog	Analog Input 23.
RH1/SEG46/AN22	80			
RH1		I/O	ST	Digital I/O.
SEG46		O	Analog	SEG46 output for LCD.
AN22		I	Analog	Analog Input 22.
RH2/SEG45/AN21	1			
RH2		I/O	ST	Digital I/O.
SEG45		O	Analog	SEG45 output for LCD.
AN21		I	Analog	Analog Input 21.
RH3/SEG44/AN20	2			
RH3		I/O	ST	Digital I/O.
SEG44		O	Analog	SEG44 output for LCD.
AN20		I	Analog	Analog Input 20.
RH4/SEG40/CCP9/P3C/ AN12/C2INC	22			
RH4		I/O	ST	Digital I/O.
SEG40		O	Analog	SEG40 output for LCD.
CCP9(3,4)		I/O	ST	Capture 9 input/Compare 9 output/PWM9 output.
P3C		O	—	ECCP3 PWM Output C.
AN12		I	Analog	Analog Input 12.
C2INC		I	Analog	Comparator 2 Input C.
RH5/SEG41/CCP8/P3B/ AN13/C2IND	21			
RH5		I/O	ST	Digital I/O.
SEG41		O	Analog	SEG41 output for LCD.
CCP8(4)		I/O	ST	Capture 8 input/Compare 8 output/PWM8 output.
P3B		O	—	ECCP3 PWM Output B.
AN13		I	Analog	Analog Input 13.
C2IND		I	Analog	Comparator 1 Input D.
RH6/SEG42/CCP7/P1C/ AN14/C1INC	20			
RH6		I/O	ST	Digital I/O.
SEG42		O	Analog	SEG42 output for LCD.
CCP7(4)		I/O	ST	Capture 7 input/Compare 7 output/PWM7 output.
P1C		O	—	ECCP1 PWM Output C.
AN14		I	Analog	Analog Input 14.
C1INC		I	Analog	Comparator 1 Input C.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; OD = Open-Drain (no P diode to VDD); I^2C™ = I^2C/SMBus

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

TABLE 1-4: PIC18F8XK90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RH7/SEG43/CCP6/P1B/AN15	19			
RH7		I/O	ST	Digital I/O.
SEG43		O	Analog	SEG43 output for LCD.
CCP6(4)		I/O	ST	Capture 6 input/Compare 6 output/PWM6 output.
P1B		O	—	ECCP1 PWM Output B.
AN15		I	Analog	Analog Input 15.

Legend:
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
I^2C™ = I^2C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to V_{DD})

Note 1: Default assignment for ECCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.
3: Not available on PIC18F65K90 and PIC18F85K90 devices.
4: The CCP6, CCP7, CCP8 and CCP9 pin placement depends on the ECCPMX Configuration bit setting.

2.6 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 3.0 "Oscillator Configurations"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-4. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins, and other signals in close proximity to the oscillator, are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

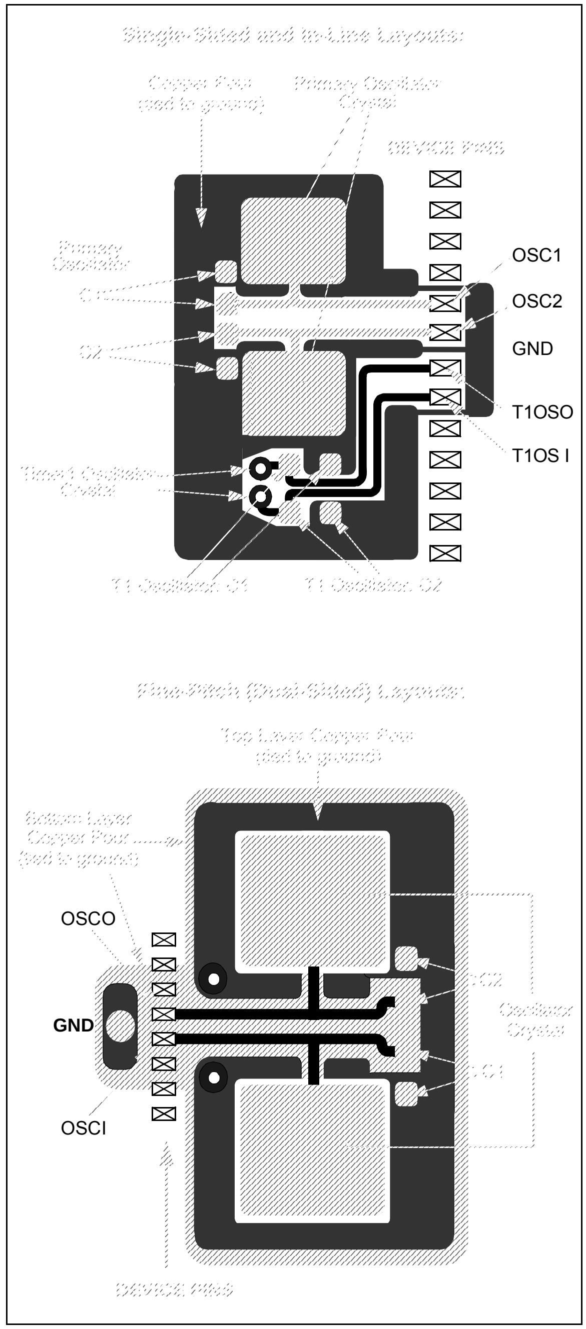
For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- *AN849, "Basic PICmicro® Oscillator Design"*
- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*

2.7 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to VSS on unused pins and drive the output to logic low.

FIGURE 2-5: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



6.3 Data Memory Organization

Note:	The operation of some aspects of data memory are changed when the PIC18 extended instruction set is enabled. See **Section 6.6 “Data Memory and the Extended Instruction Set”** for more information.

The data memory in PIC18 devices is implemented as static RAM. Each register in the data memory has a 12-bit address, allowing up to 4,096 bytes of data memory. The memory space is divided into as many as 16 banks that contain 256 bytes each. PIC18FX6K90 and PIC18FX7K90 devices implement all 16 complete banks, for a total of 4 Kbytes. PIC18FX5K90 devices implement only the first eight complete banks, for a total of 2 Kbytes.

Figure 6-6 and Figure 6-7 show the data memory organization for the devices.

The data memory contains Special Function Registers (SFRs) and General Purpose Registers (GPRs). The SFRs are used for control and status of the controller and peripheral functions, while GPRs are used for data storage and scratchpad operations in the user’s application. Any read of an unimplemented location will read as ‘0’s.

The instruction set and architecture allow operations across all banks. The entire data memory may be accessed by Direct, Indirect or Indexed Addressing modes. Addressing modes are discussed later in this section.

To ensure that commonly used registers (select SFRs and select GPRs) can be accessed in a single cycle, PIC18 devices implement an Access Bank. This is a 256-byte memory space that provides fast access to select SFRs and the lower portion of GPR Bank 0 without using the Bank Select Register. For details on the Access RAM, see **Section 6.3.2 “Access Bank”**.

6.3.1 BANK SELECT REGISTER

Large areas of data memory require an efficient addressing scheme to make possible rapid access to any address. Ideally, this means that an entire address does not need to be provided for each read or write operation. For PIC18 devices, this is accomplished with a RAM banking scheme. This divides the memory space into 16 contiguous banks of 256 bytes. Depending on the instruction, each location can be addressed directly by its full 12-bit address, or an 8-bit, low-order address and a 4-bit Bank Pointer.

Most instructions in the PIC18 instruction set make use of the Bank Pointer, known as the Bank Select Register (BSR). This SFR holds the four Most Significant bits of a location’s address. The instruction itself includes the eight Least Significant bits. Only the four lower bits of the BSR are implemented (BSR<3:0>). The upper four bits are unused, always read as ‘0’ and cannot be written to. The BSR can be loaded directly by using the `MOVLB` instruction.

The value of the BSR indicates the bank in data memory. The eight bits in the instruction show the location in the bank and can be thought of as an offset from the bank’s lower boundary. The relationship between the BSR’s value and the bank division in data memory is shown in Figure 6-7.

Since up to 16 registers may share the same low-order address, the user must always be careful to ensure that the proper bank is selected before performing a data read or write. For example, writing what should be program data to an 8-bit address of F9h while the BSR is 0Fh, will end up resetting the Program Counter.

While any bank can be selected, only those banks that are actually implemented can be read or written to. Writes to unimplemented banks are ignored, while reads from unimplemented banks will return ‘0’s. Even so, the STATUS register will still be affected as if the operation was successful. The data memory map in Figure 6-6 indicates which banks are implemented.

In the core PIC18 instruction set, only the `MOVFF` instruction fully specifies the 12-bit address of the source and target registers. When this instruction executes, it ignores the BSR completely. All other instructions include only the low-order address as an operand and must use either the BSR or the Access Bank to locate their target registers.

TABLE 11-1: PORTA FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0/ULPWU	RA0	0	O	DIG	LATA<0> data output; not affected by analog input.
		1	I	TTL	PORTA<0> data input; disabled when analog input is enabled.
	AN0	1	I	ANA	A/D Input Channel 0. Default input configuration on POR; does not affect digital output.
	ULPWU	1	I	ANA	Ultra Low-Power Wake-up (ULPWU) input.
RA1/AN1/SEG18	RA1	0	O	DIG	LATA<1> data output; not affected by analog input.
		1	I	TTL	PORTA<1> data input; disabled when analog input is enabled.
	AN1	1	I	ANA	A/D Input Channel 1. Default input configuration on POR; does not affect digital output.
	SEG18	1	O	ANA	LCD Segment 18 output; disables all other pin functions.
RA2/AN2/VREF-	RA2	0	O	DIG	LATA<2> data output; not affected by analog input.
		1	I	TTL	PORTA<2> data input; disabled when analog functions are enabled.
	AN2	1	I	ANA	A/D Input Channel 2. Default input configuration on POR.
	VREF-	1	I	ANA	A/D and comparator low reference voltage input.
RA3/AN3/VREF+	RA3	0	O	DIG	LATA<3> data output; not affected by analog input.
		1	I	TTL	PORTA<3> data input; disabled when analog input is enabled.
	AN3	1	I	ANA	A/D Input Channel 3. Default input configuration on POR.
	VREF+	1	I	ANA	A/D and comparator high reference voltage input.
RA4/T0CKI/SEG14	RA4	0	O	DIG	LATA<4> data output.
		1	I	ST	PORTA<4> data input. Default configuration on POR.
	T0CKI	x	I	ST	Timer0 clock input.
	SEG14	1	O	ANA	LCD Segment 14 output; disables all other pin functions.
RA5/AN4/SEG15/T1CKI/T3G/HLVDIN	RA5	0	O	DIG	LATA<5> data output; not affected by analog input.
		1	I	TTL	PORTA<5> data input; disabled when analog input is enabled.
	AN4	1	I	ANA	A/D Input Channel 4. Default configuration on POR.
	SEG15	1	O	ANA	LCD Segment 15 output; disables all other pin functions.
	T1CKI	x	I	ST	Timer1 clock input.
	T3G	x	I	ST	Timer3 external clock gate input.
	HLVDIN	1	I	ANA	High/Low-Voltage Detect (HLVD) external trip point input.
OSC2/CLKO/RA6	OSC2	x	O	ANA	Main oscillator feedback output connection (HS, XT and LP modes).
	CLKO	x	O	DIG	System cycle clock output (FOSC/4, EC and INTOSC modes).
	RA6	0	O	DIG	LATA<6> data output; disabled when OSC2 Configuration bit is set.
		1	I	TTL	PORTA<6> data input; disabled when OSC2 Configuration bit is set.
OSC1/CLKI/RA7	OSC1	x	I	ANA	Main oscillator input connection (HS, XT and LP modes).
	CLKI	x	I	ANA	Main external clock source input (EC modes).
	RA7	0	O	DIG	LATA<7> data output; disabled when OSC2 Configuration bit is set.
		1	I	TTL	PORTA<7> data input; disabled when OSC2 Configuration bit is set.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

TABLE 11-10: PORTE FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RE0/LCDBIAS1/ P2D	RE0	0	O	DIG	LATE<0> data output.
		1	I	ST	PORTE<0> data input.
	LCDBIAS1	—	I	ANA	LCD module bias voltage input.
	P2D	0	O	—	ECCP2 PWM Output D. May be configured for tri-state during Enhanced PWM shutdown events.
RE1/LCDBIAS2/ P2C	RE1	0	O	DIG	LATE<1> data output.
		1	I	ST	PORTE<1> data input.
	LCDBIAS2	—	I	ANA	LCD module bias voltage input.
	P2C	0	O	—	ECCP2 PWM Output C. May be configured for tri-state during Enhanced PWM shutdown events.
RE2/LCDBIAS3/ P2B	RE2	0	O	DIG	LATE<2> data output.
		1	I	ST	PORTE<2> data input.
	LCDBIAS3	x	I	ANA	LCD module bias voltage input.
	P2B	0	O	—	ECCP2 PWM Output B. May be configured for tri-state during Enhanced PWM shutdown events.
RE3/COM0/ P3C/CCP9/ REFO	RE3	0	O	DIG	LATE<3> data output.
		1	I	ST	PORTE<3> data input.
	COM0	x	O	ANA	LCD Common 0 output; disables all other outputs.
	P3C	0	O	—	ECCP3 PWM Output C. May be configured for tri-state during Enhanced PWM shutdown events.
	CCP9(2)	0	O	DIG	CCP9 compare/PWM output; takes priority over port data.
		1	I	ST	CCP9 capture input.
	REFO	x	O	DIG	Reference output clock.
RE4/COM1/ P3B/CCP8	RE4	0	O	DIG	LATE<4> data output.
		1	I	ST	PORTE<4> data input.
	COM1	x	O	ANA	LCD Common 1 output; disables all other outputs.
	P3B	0	O	—	ECCP3 PWM Output B. May be configured for tri-state during Enhanced PWM shutdown events.
	CCP8	0	O	DIG	CCP8 Compare/PWM output; takes priority over port data.
		1	I	ST	CCP8 capture input.
RE5/COM2/ P1C/CCP7	RE5	0	O	DIG	LATE<5> data output.
		1	I	ST	PORTE<5> data input.
	COM2	x	O	ANA	LCD Common 2 output; disables all other outputs.
	P1C	0	O	—	ECCP1 PWM Output C. May be configured for tri-state during Enhanced PWM shutdown events.
	CCP7	0	O	DIG	CCP7 Compare/PWM output; takes priority over port data.
		1	I	ST	CCP7 capture input.
RE6/COM3/ P1B/CCP6	RE6	0	O	DIG	LATE<6> data output.
		1	I	ST	PORTE<6> data input.
	COM3	x	O	ANA	LCD Common 3 output; disables all other outputs.
	P1B	0	O	—	ECCP1 PWM Output B. May be configured for tri-state during Enhanced PWM shutdown events.
	CCP6	0	O	DIG	CCP6 Compare/PWM output; takes priority over port data.
		1	I	ST	CCP6 capture input.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: Alternate assignment for ECCP2 when the CCP2MX Configuration bit is cleared.

2: This bit is unimplemented in PIC18FX5K90 devices.

17.2.4 LEAP YEAR

Since the year range on the RTCC module is 2000 to 2099, the leap year calculation is determined by any year divisible by four in the above range. Only February is affected in a leap year.

February will have 29 days in a leap year and 28 days in any other year.

17.2.5 GENERAL FUNCTIONALITY

All Timer registers containing a time value of seconds or greater are writable. The user configures the time by writing the required year, month, day, hour, minutes and seconds to the Timer registers, via Register Pointers. (See **Section 17.2.8 "Register Mapping"**.)

The timer uses the newly written values and proceeds with the count from the required starting point.

The RTCC is enabled by setting the RTCEN bit (RTCCFG<7>). If enabled, while adjusting these registers, the timer still continues to increment. However, any time the MINSEC register is written to, both of the timer prescalers are reset to '0'. This allows fraction of a second synchronization.

The Timer registers are updated in the same cycle as the write instruction's execution by the CPU. The user must ensure that when RTCEN = 1, the updated registers will not be incremented at the same time. This can be accomplished in several ways:

- By checking the RTCSYNC bit (RTCCFG<4>)
- By checking the preceding digits from which a carry can occur
- By updating the registers immediately following the seconds pulse (or an alarm interrupt)

The user has visibility to the half-second field of the counter. This value is read-only and can be reset only by writing to the lower half of the SECONDS register.

17.2.6 SAFETY WINDOW FOR REGISTER READS AND WRITES

The RTCSYNC bit indicates a time window during which the RTCC Clock Domain registers can be safely read and written without concern about a rollover. When RTCSYNC = 0, the registers can be safely accessed by the CPU.

Whether RTCSYNC = 1 or 0, the user should employ a firmware solution to ensure that the data read did not fall on a rollover boundary, resulting in an invalid or partial read. This firmware solution would consist of reading each register twice and then comparing the two values. If the two values matched, then a rollover did not occur.

17.2.7 WRITE LOCK

In order to perform a write to any of the RTCC Timer registers, the RTCWREN bit (RTCCFG<5>) must be set.

To avoid accidental writes to the RTCC Timer register, it is recommended that the RTCWREN bit (RTCCFG<5>) be kept clear when not writing to the register. For the RTCWREN bit to be set, there is only one instruction cycle time window allowed between the 55h/AA sequence and the setting of RTCWREN. For that reason, it is recommended that users follow the code example in Example 17-1.

EXAMPLE 17-1: SETTING THE RTCWREN BIT

```
movlw    0x55
movwf    EECON2
movlw    0xAA
movwf    EECON2
bsf      RTCCFG,RTCWREN
```

17.2.8 REGISTER MAPPING

To limit the register interface, the RTCC Timer and Alarm Timer registers are accessed through corresponding Register Pointers. The RTCC Value register window (RTCVALH and RTCVALL) uses the RTCPTRx bits (RTCCFG<1:0>) to select the required Timer register pair.

By reading or writing to the RTCVALH register, the RTCC Pointer value (RTCPTR<1:0>) decrements by '1' until it reaches '00'. When '00' is reached, the MINUTES and SECONDS value is accessible through RTCVALH and RTCVALL until the pointer value is manually changed.

TABLE 17-3: RTCVALH AND RTCVALL REGISTER MAPPING

RTCPTR<1:0>	RTCC Value Register Window	
	RTCVALH	RTCVALL
00	MINUTES	SECONDS
01	WEEKDAY	HOURS
10	MONTH	DAY
11	—	YEAR

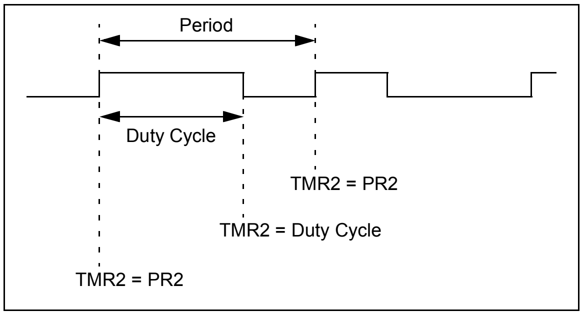
The Alarm Value register windows (ALRMVALH and ALRMVALL) use the ALRMPTR bits (ALRMCFG<1:0>) to select the desired alarm register pair.

By reading or writing to the ALRMVALH register, the Alarm Pointer value, ALRMPTR<1:0>, decrements by one until it reaches '00'. When it reaches '00', the ALRMMIN and ALRMSEC value is accessible through ALRMVALH and ALRMVALL until the pointer value is manually changed.

NOTES:

A PWM output (Figure 18-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 18-4: PWM OUTPUT



18.4.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

EQUATION 18-1:

$$\text{PWM Period} = [(\text{PR2}) + 1] \bullet 4 \bullet \text{TOSC} \bullet (\text{TMR2 Prescale Value})$$

PWM frequency is defined as 1/[PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP4 pin is set
  (An exception: If PWM duty cycle = 0%, the CCP4 pin will not be set)
- The PWM duty cycle is latched from CCPR4L into CCPR4H

Note:	The Timer2 postscalers (see **Section 14.0 “Timer2 Module”**) are not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

18.4.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR4L register (using CCP4 as an example) and to the CCP4CON<5:4> bits. Up to 10-bit resolution is available. The CCPR4L contains the eight MSbs and the CCP4CON<5:4> bits contain the two LSbs. This 10-bit value is represented by CCPR4L:CCP4CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

EQUATION 18-2:

$$\text{PWM Duty Cycle} = (\text{CCPR4L:CCP4CON<5:4>}) \bullet \text{TOSC} \bullet (\text{TMR2 Prescale Value})$$

CCPR4L and CCP4CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR4H until after a match between PR2 and TMR2 occurs (that is, the period is complete). In PWM mode, CCPR4H is a read-only register.

The CCPR4H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPR4H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or two bits of the TMR2 prescaler, the CCP4 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by Equation 18-3:

EQUATION 18-3:

$$\text{PWM Resolution (max)} = \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the CCP4 pin will not be cleared.

TABLE 18-6: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	14	12	10	8	7	6.58

19.2 Capture Mode

In Capture mode, the CCPRxH:CCPRxL register pair captures the 16-bit value of the TMR1 or TMR3 registers when an event occurs on the corresponding ECCPx pin. An event is defined as one of the following:

- Every falling edge
- Every rising edge
- Every fourth rising edge
- Every 16^{th} rising edge

The event is selected by the mode select bits, CCPxM<3:0> (CCPxCON register<3:0>). When a capture is made, the interrupt request flag bit, CCPxIF, is set (see Table 19-2). The flag must be cleared by software. If another capture occurs before the value in the CCPRxH/L register is read, the old captured value is overwritten by the new captured value.

TABLE 19-2: ECCP1/2/3 INTERRUPT FLAG BITS

ECCP Module	Flag Bit
1	PIR3<1>
2	PIR3<2>
3	PIR4<0>

19.2.1 ECCP PIN CONFIGURATION

In Capture mode, the appropriate ECCPx pin should be configured as an input by setting the corresponding TRIS direction bit.

Note:	If the ECCPx pin is configured as an output, a write to the PORT can cause a capture condition.

19.2.2 TIMER1/TIMER3 MODE SELECTION

The timers that are to be used with the capture feature (Timer1 and/or Timer3) must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work. The timer to be used with each ECCP module is selected in the CCPTMRS0 register (Register 19-2).

19.2.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit clear to avoid false interrupts. The interrupt flag bit, CCPxIF, should also be cleared following any such change in operating mode.

19.2.4 ECCP PRESCALER

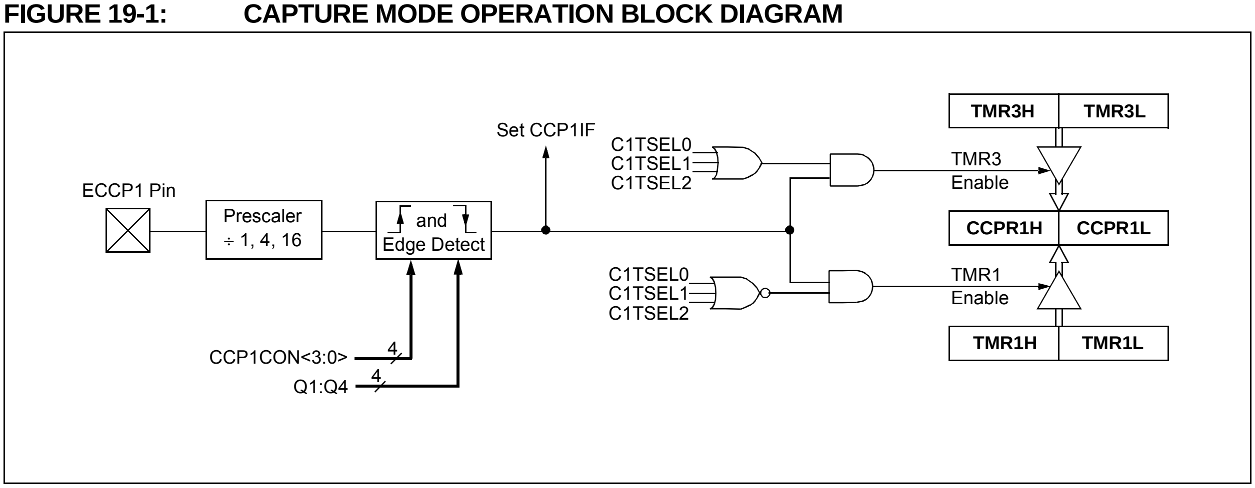
There are four prescaler settings in Capture mode; they are specified as part of the operating mode selected by the mode select bits (CCPxM<3:0>). Whenever the ECCP module is turned off, or Capture mode is disabled, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared; therefore, the first capture may be from a non-zero prescaler. Example 19-1 provides the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the “false” interrupt.

EXAMPLE 19-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF   CCP1CON     ; Turn ECCP module off
MOVLW  NEW_CAPT_PS ; Load WREG with the
                   ; new prescaler mode
                   ; value and ECCP ON
MOVWF  CCP1CON     ; Load CCP1CON with
                   ; this value
```

FIGURE 19-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



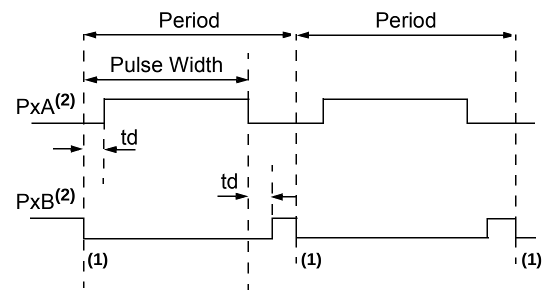
19.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the PxA pin, while the complementary PWM output signal is output on the PxB pin (see Figure 19-6). This mode can be used for half-bridge applications, as shown in Figure 19-7, or for full-bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in half-bridge power devices. The value of the PxDC<6:0> bits of the ECCPxDEL register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. For more details on the dead-band delay operations, see **Section 19.4.6 "Programmable Dead-Band Delay Mode"**.

Since the PxA and PxB outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure PxA and PxB as outputs.

FIGURE 19-6: EXAMPLE OF HALF-BRIDGE PWM OUTPUT



td = Dead-Band Delay

Note 1: At this time, the TMR2 register is equal to the PR2 register.

2: Output signals are shown as active-high.

FIGURE 19-7: EXAMPLE OF HALF-BRIDGE APPLICATIONS

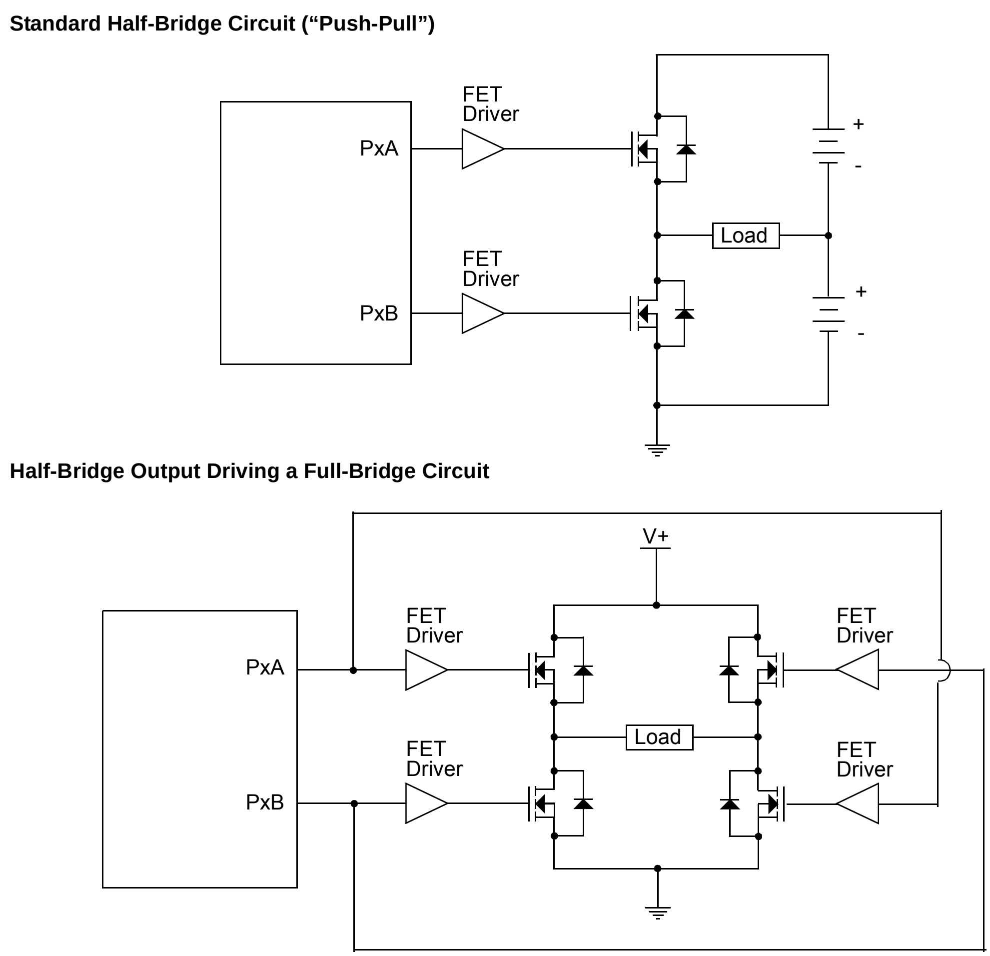
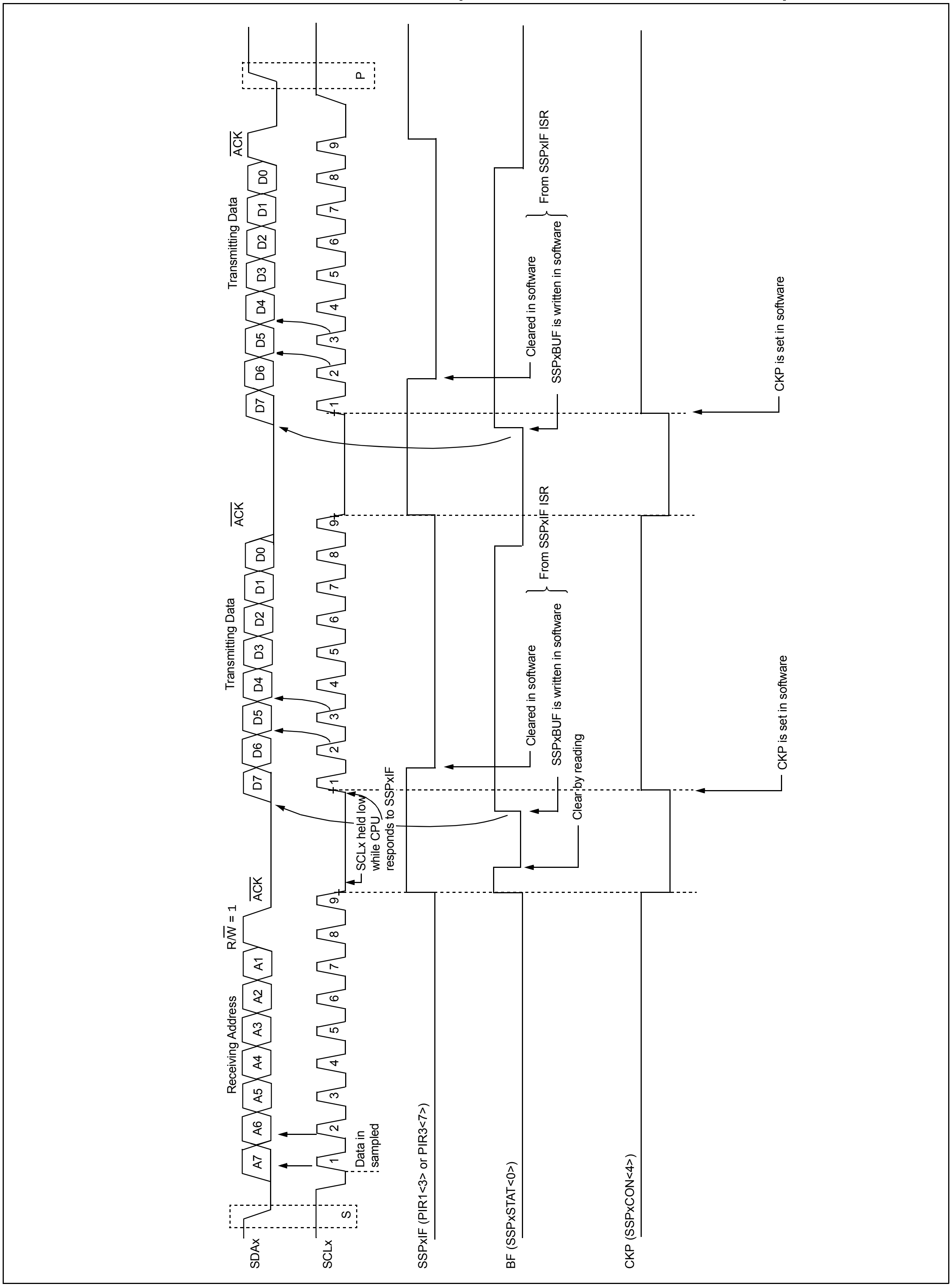


FIGURE 21-10: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)



22.2 EUSART Asynchronous Mode

The Asynchronous mode of operation is selected by clearing the SYNC bit (TXSTAx<4>). In this mode, the EUSART uses standard Non-Return-to-Zero (NRZ) format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is 8 bits. An on-chip, dedicated 8-bit/16-bit Baud Rate Generator can be used to derive standard baud rate frequencies from the oscillator.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent but use the same data format and baud rate. The Baud Rate Generator produces a clock, either x16 or x64 of the bit shift rate, depending on the BRGH and BRG16 bits (TXSTAx<2> and BAUDCONx<3>). Parity is not supported by the hardware but can be implemented in software and stored as the 9th data bit.

When operating in Asynchronous mode, the EUSART module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver
- Auto-Wake-up on Sync Break Character
- 12-Bit Break Character Transmit
- Auto-Baud Rate Detection

22.2.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 22-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREGx. The TXREGx register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. As soon as the Stop bit is transmitted, the TSR is loaded with new data from the TXREGx register (if available).

Once the TXREGx register transfers the data to the TSR register (occurs in one TCY), the TXREGx register is empty and the TXxIF flag bit is set. This interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXxIE. TXxIF will be set regardless of the state of TXxIE; it cannot be cleared in software. TXxIF is also not cleared immediately upon loading TXREGx, but becomes valid in the second instruction cycle following the load instruction. Polling TXxIF immediately following a load of TXREGx will return invalid results.

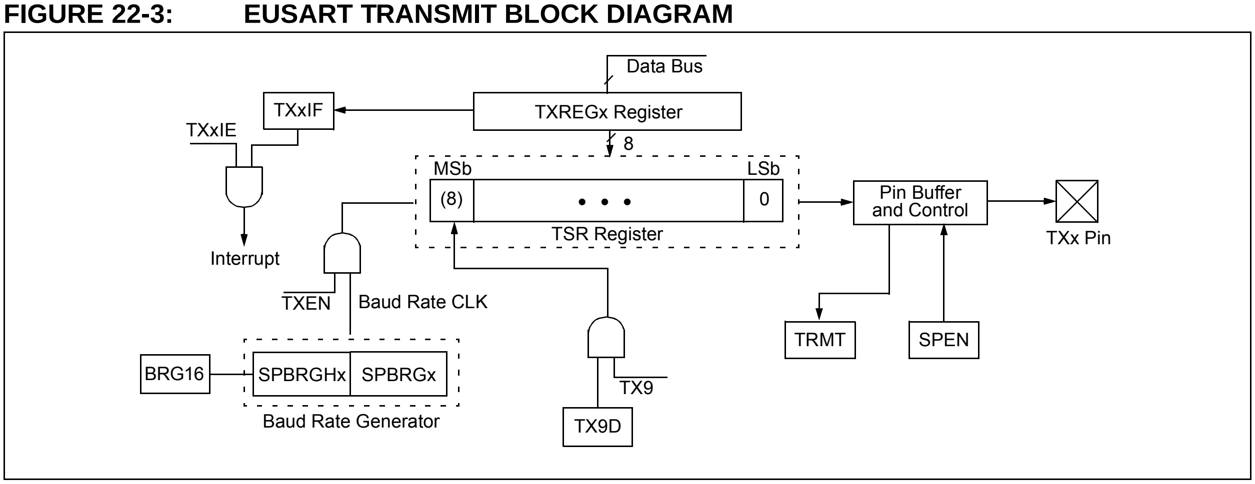
While TXxIF indicates the status of the TXREGx register; another bit, TRMT (TXSTAx<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit so the user has to poll this bit in order to determine if the TSR register is empty.

> **Note 1:** The TSR register is not mapped in data memory, so it is not available to the user.
>
> **2:** Flag bit, TXxIF, is set when enable bit, TXEN, is set.

To set up an Asynchronous Transmission:

1. Initialize the SPBRGHx:SPBRGx registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Enable the asynchronous serial port by clearing bit, SYNC, and setting bit, SPEN.
3. If interrupts are desired, set enable bit, TXxIE.
4. If 9-bit transmission is desired, set transmit bit, TX9; can be used as an address/data bit.
5. Enable the transmission by setting bit, TXEN, which will also set bit, TXxIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
7. Load data to the TXREGx register (starts transmission).
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 22-3: EUSART TRANSMIT BLOCK DIAGRAM



27.8 Measuring Temperature Using the CTMU Module

The CTMU, along with an internal diode, can be used to measure the temperature. The ADC can be connected to the internal diode and the CTMU module can source the current to the diode. The ADC reading will reflect the temperature. With the increase, the ADC readings will go low. This can be used for low-cost temperature measurement applications.

EXAMPLE 27-5: ROUTINE FOR TEMPERATURE MEASUREMENT USING INTERNAL DIODE

```
//Initialize CTMU
    CTMUICON=0x03;
    CTMUCONHbits.CTMUEN=1;
    CTMUCONLbits.EDG1STAT=1;
//Initialize ADC
    ADCON0=0xE5;                      //ADCON and connect to Internal diode
    ADCON1=0;
    ADCON2=0xBE;                      //Right justified

    ADCON0bits.GO=1;
    while(ADCON0bits.GO==1);
    Temp=ADRES;                       ;//read ADC results ( inversely proportional to temperature)
-----------------------------------------------------------------------------------------------
```

Note: The temperature diode is not calibrated; the user will have to calibrate the diode to their application.

REGISTER 28-12: CONFIG7L: CONFIGURATION REGISTER 7 LOW (BYTE ADDRESS 30000Ch)(3)

R/C-1	R/C-1	R/C-1	R/C-1	R/C-1	R/C-1	R/C-1	R/C-1
EBTR7(1)	EBTR6(1)	EBTR5(1)	EBTR4(1)	EBTR3	EBTR2	EBTR1	EBTR0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **EBTR7:** Table Read Protection bit(1)
1 = Block 7 is not protected from table reads executed in other blocks
0 = Block 7 is protected from table reads executed in other blocks

bit 6 **EBTR6:** Table Read Protection bit(1)
1 = Block 6 is not protected from table reads executed in other blocks
0 = Block 6 is protected from table reads executed in other blocks

bit 5 **EBTR5:** Table Read Protection bit(1)
1 = Block 5 is not protected from table reads executed in other blocks
0 = Block 5 is protected from table reads executed in other blocks

bit 4 **EBTR4:** Table Read Protection bit(1)
1 = Block 4 is not protected from table reads executed in other blocks
0 = Block 4 is protected from table reads executed in other blocks

bit 3 **EBTR3:** Table Read Protection bit
1 = Block 3 is not protected from table reads executed in other blocks
0 = Block 3 is protected from table reads executed in other blocks

bit 2 **EBTR2**: Table Read Protection bit
1 = Block 2 is not protected from table reads executed in other blocks
0 = Block 2 is protected from table reads executed in other blocks

bit 1 **EBTR1:** Table Read Protection bit
1 = Block 1 is not protected from table reads executed in other blocks
0 = Block 1 is protected from table reads executed in other blocks

bit 0 **EBTR0:** Table Read Protection bit
1 = Block 0 is not protected from table reads executed in other blocks
0 = Block 0 is protected from table reads executed in other blocks

Note 1: This bit is only available on PIC18F67K90 and PIC18F87K90.
2: This bit is only available on PIC18F66K90, PIC18F67K90, PIC18F86K90 and PIC18F87K90 devices.
3: For the memory size of the blocks, refer to Figure 28-6.

BNC **Branch if Not Carry**

Syntax:	BNC n
Operands:	-128 ≤ n ≤ 127
Operation:	if Carry bit is '0', (PC) + 2 + 2n → PC
Status Affected:	None
Encoding:	1110 0011 nnnn nnnn
Description:	If the Carry bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: `HERE BNC Jump`

Before Instruction
PC = address (HERE)
After Instruction
If Carry = 0;
PC = address (Jump)
If Carry = 1;
PC = address (HERE + 2)

BNN **Branch if Not Negative**

Syntax:	BNN n
Operands:	-128 ≤ n ≤ 127
Operation:	if Negative bit is '0', (PC) + 2 + 2n → PC
Status Affected:	None
Encoding:	1110 0111 nnnn nnnn
Description:	If the Negative bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a two-cycle instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: `HERE BNN Jump`

Before Instruction
PC = address (HERE)
After Instruction
If Negative = 0;
PC = address (Jump)
If Negative = 1;
PC = address (HERE + 2)

31.2 DC Characteristics: Power-Down and Supply Current PIC18F87K90 Family (Industrial/Extended) (Continued)

PIC18F87K90 Family		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Module Differential Currents (ΔIWDT, ΔIBOR, ΔIHLVD, ΔIOSCB, ΔIAD)						
D022 (ΔIWDT)	**Watchdog Timer**						
	All devices	0.3	1	μA	-40°C	VDD = 1.8V(4) Regulator Disabled	
		0.3	1	μA	+25°C		
		0.3	1	μA	+85°C		
		0.5	2	μA	+125°C		
	All devices	0.6	2	μA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		0.6	2	μA	+25°C		
		0.7	2	μA	+85°C		
		1	3	μA	+125°C		
	All devices	0.6	2	μA	-40°C	VDD = 5V(5) Regulator Enabled	
		0.6	2	μA	+25°C		
		0.7	2	μA	+85°C		
		1.5	4	μA	+125°C		
D022A (ΔIBOR) (ΔIBOR)	**Brown-out Reset**						
	All devices	4.6	19	μA	-40°C	VDD = 3.3V(4) Regulator Disabled	High-Power BOR
		4.5	20	μA	+25°C		
		4.7	20	μA	+85°C		
		18	40	μA	+125°C		
	All devices	4.2	20	μA	-40°C	VDD = 5V(5) Regulator Enabled	High-Power BOR
		4.3	20	μA	+25°C		
		4.4	20	μA	+85°C		
		20	40	μA	+125°C		
D022B (ΔIHLVD)	**High/Low-Voltage Detect**						
	All devices	3.8	9	μA	-40°C	VDD = 1.8V(4) Regulator Disabled	
		4.2	9	μA	+25°C		
		4.3	10	μA	+85°C		
		4.5	12	μA	+125°C		
	All devices	4.5	11	μA	-40°C	VDD = 3.3V(4) Regulator Disabled	
		4.8	12	μA	+25°C		
		4.8	12	μA	+85°C		
		5.0	14	μA	+125°C		
	All devices	4.9	13	μA	-40°C	VDD = 5V(5) Regulator Enabled	
		4.9	13	μA	+25°C		
		4.9	13	μA	+85°C		
		5.3	15	μA	+125°C		

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in a high-impedance state and tied to VDD or VSS, and all features that add delta current are disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: Voltage regulator disabled (ENVREG = 0, tied to VSS, $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 1).

5: Voltage regulator enabled (ENVREG = 1, tied to VDD, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0).

6: LCD glass is not connected; resistor current is not included.

7: 48 MHz maximum frequency at 125°C.

31.3 DC Characteristics: PIC18F87K90 Family (Industrial/Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		All I/O Ports:				
D030		with TTL Buffer	VSS	0.15 VDD	V	VDD < 4.5V
D031		with Schmitt Trigger Buffer	—	0.8	V	4.5 ≤ VDD ≤ 5.5V
		RC3, RC4	VSS	0.2 VDD	V	VDD < 4.5
		RD5, RD6	VSS	1.5	V	4.5 ≤ VDD ≤ 5.5V
D031A		RC3, RC4	VSS	0.3 VDD	V	I²C™ enabled
D031B		RD5, RD6	VSS	0.8	V	SMBus enabled
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		OSC1	VSS	0.2 VDD	V	LP, XT, HS, HSPLL modes
D033A		OSC1	VSS	0.2 VDD	V	EC, ECPLL modes
D034		SOSCI	VSS	0.3 VDD	V	
	VIH	**Input High Voltage**				
		I/O Ports:				
D040		with TTL Buffer	0.25 VDD	VDD	V	VDD < 4.5V
			2.0	VDD		4.5 ≤ VDD ≤ 5.5V
D041		with Schmitt Trigger Buffer	0.8 VDD	VDD	V	
		RC3, RC4	0.7 VDD	VDD	V	VDD < 4.5
		RD5, RD6	3V	5.5	V	4.5 ≤ VDD ≤ 5.5V
D041A		RC3, RC4	0.7 VDD	VDD	V	I²C enabled
D041B		RD5, RD6	2.1	VDD	V	SMBus enabled
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		OSC1	0.7 VDD	VDD	V	LP, XT, HS, HSPLL modes
D043A		OSC1	0.8 VDD	VDD	V	EC, ECPLL modes
D044		SOSCI	0.7 VDD	VDD	V	
	IIL	**Input Leakage Current**(1)				
D060		I/O Ports	±50	±200	nA	VSS ≤ VPIN ≤ VDD, Pin at High-Impedance
D061		$\overline{MCLR}$	—	±5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	±5	µA	VSS ≤ VPIN ≤ VDD
	IPU	**Weak Pull-up Current**				
D070	IPURB	PORTB Weak Pull-up Current	50	400	µA	VDD = 3.3V, VPIN = VSS

Note 1: Negative current is defined as current sourced by the pin.

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